



98

NEW RELEASES

Data Book

FEATURING

Precision Reset Controllers
Voltage Supervisory Circuits
Hot Swap Controllers
Data Conversion Products
Application Notes

1998 New Releases Data Book

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President's Message

Dear Prospective Customers,

In our 1998 Data Book, one can see that our product families have grown quickly in the last year. Our programmable analog technology has evolved into the optimum solution for delivering cost-effective analog functions to a variety of applications.

The Reset controller and Microcontroller Supervisor product line offers the best solutions available to control the system reset signals based upon the status of the system power supplies, additional system voltages, external reset conditions and system operational integrity.

Hot Swap controllers have been developed to support the rapidly growing requirement for "high-availability" systems in the Telecommunications and Data Communications markets.

The growing DACPOT™ Product family provides a cost effective solution to the replacement of potentiometers in a variety of control, consumer and communications applications.

New product families in development include Analog Monitor devices, higher resolution DACPOTs, Sensor Linearizers, and battery management devices. New product information is placed on the Summit Website as it becomes available.

As Summit Microelectronics has matured, we have implemented many programs to support our customer's business requirements. Summit is Y2K compliant and is expecting to be ISO 9000 certified in the third calendar quarter of 1998.

Summit's focus is to solve our customers applications problems with integrated solutions. By combining inputs from a variety of customers with similar application problems, we derive cost-effective standard products.

Our goal is to provide to our customers unparalleled support in product development, innovation, quality, reliability, pricing and commercial issues. It is through this close interaction with our customers that we are able to insure our mutual success. We are always available for your comments and questions and encourage your feedback. We would like to solve your analog applications problem.

Sincerely yours,

Rick Orlando

Rick Orlando

*President and Applications Engineer
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DATA BOOK NOTES

Data sheets for products in design development are designated by the words **Advance Information** in the masthead. For availability please contact your Summit Microelectronics representative.

Data sheets for products beyond the design stage but not fully characterized are designated by the word **Preliminary** in the masthead.

Data sheets for fully characterized products released to production will not have any additional wording in the masthead.

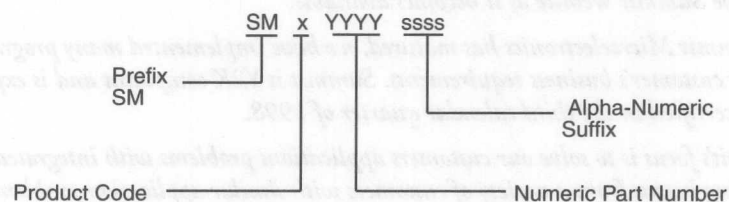
PART NUMBER CHANGES

The S24368 is renumbered and is now the SMD1102/03 Advance Information data sheet.

PART NUMBERING CONVENTION

Existing part numbers will not change.

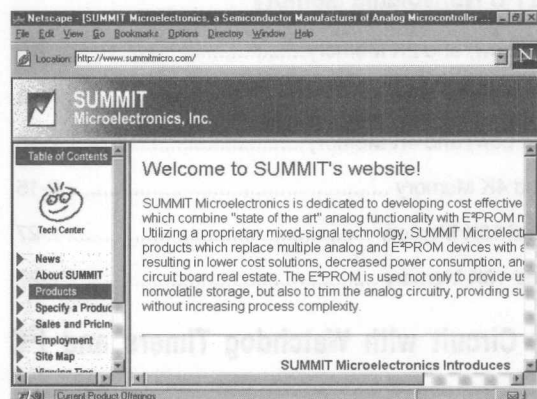
In the future new Summit products will follow the part numbering convention shown below.



D = Conversion Product
E = Enhanced Product Upgrade
H = Hot Swap
N = Nonvolatile Memory
P = Digital Potentiometer
R = Reference Voltage
S = Supervisory Circuit or Reset



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SECTION 1 **Hot Swap Controller**

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Hot Swap Voltage Controller



FEATURES

- Full Voltage Control for Hot Swap Applications
 - Card Insertion Detection
 - Platform Voltage Detection
 - Card Voltage Sequencing
 - 5 Volt, 12 Volt and 3.3 Volt
- 12 Volt FET Enable Outputs
 - Allows use of Low On-resistance N-Channel FETS
- Card Reset Generation Based on Out of Spec Voltages
 - Host Reset
- Programmable Slew Rate Control [250V/Sec Default Rate]
- Supports 5 Volt, 3.3 Volt and Mixed Voltage Cards
- Integrated 1K Bit E²PROM Memory
- Data Download™ Mode [Simplifies Downloading of Configuration Memory into Interface ASIC or MCU]

DESCRIPTION

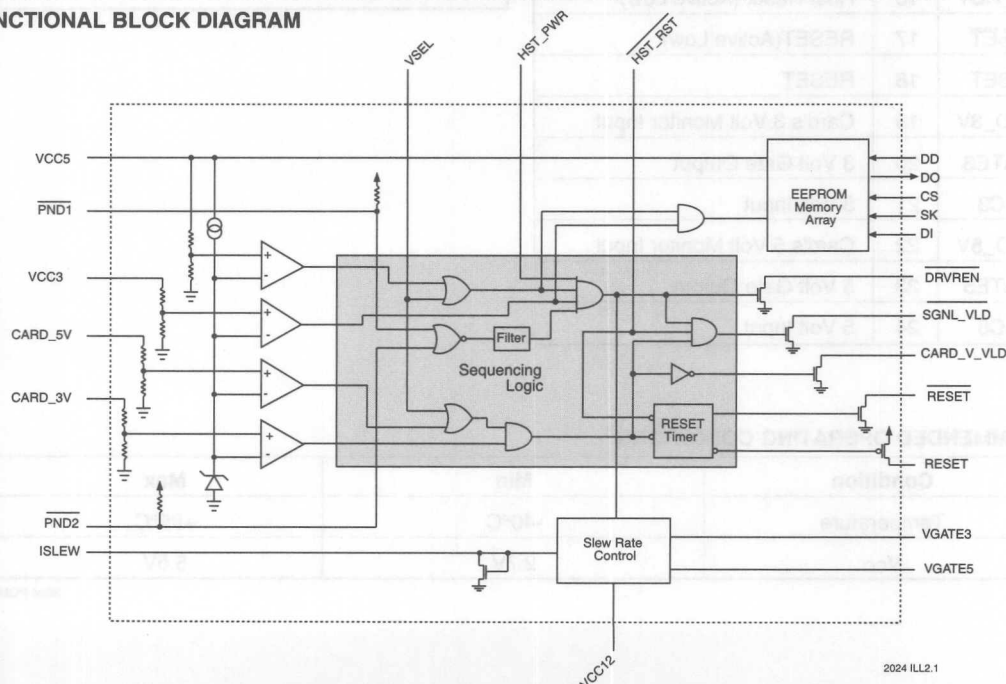
The S39421 is a fully integrated hot swap controller intended for use on add-in cards that may be inserted into or removed from powered-on host platforms. The S39421 performs a variety of tasks starting with the validation of proper card insertion and the presence of "in-spec" voltages at the host platform interface.

Once power is switched on, the S39421 continues to monitor the back-end power to the add-in card and the host power supply. If either the 5V or 3.3V supplies drop below Vtrip the S39421 will immediately assert the RESET outputs and power-down the add-in card.

In addition to the power control for the add-in card, the S39421 provides status signals that can be employed by the host and for the control of bus interface components.

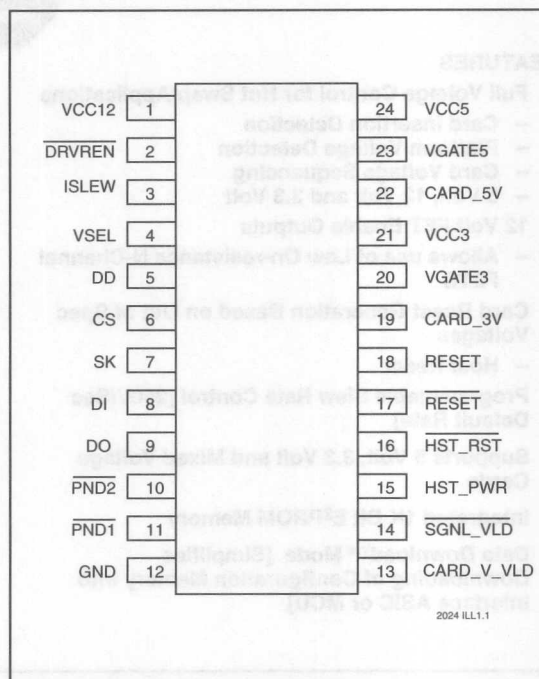
The on board E²PROM can be used as configuration memory for the individual card or as general purpose memory. The proprietary DataDownload mode provides a more direct interface to the E²PROM for simplified access by the add-in card's controller or ASIC.

FUNCTIONAL BLOCK DIAGRAM



**S39421****PIN CONFIGURATION**

Symbol	Pin	Description
VCC12	1	12 Volt Input
DRVREN	2	High Side Driver Enable (L)
ISLEW	3	Slew Rate Control
VSEL	4	Voltage Select
DD	5	Data Download Enable
CS	6	Microwire Chip Select
SK	7	Microwire Serial Clock
DI	8	Microwire Data In
DO	9	Microwire Data Out
PND2	10	Pin Detect 2 (Active Low)
PND1	11	Pin Detect 1 (Active Low)
GND	12	Ground
CARD_V_VLD	13	Card Voltage Valid
SGNL_VLD	14	Signals Valid (Active Low)
HST_PWR	15	Host Power Up Enable
HST_RST	16	Host Reset (Active Low)
RESET	17	RESET(Active Low)
RESET	18	RESET
CARD_3V	19	Card's 3 Volt Monitor Input
VGATE3	20	3 Volt Gate Output
VCC3	21	3 Volt Input
CARD_5V	22	Card's 5 Volt Monitor Input
VGATE5	23	5 Volt Gate Output
VCC5	24	5 Volt Input

**RECOMMENDED OPERATING CONDITIONS**

Condition	Min	Max
Temperature	-40°C	+85°C
V _{cc}	2.7V	5.5V

2024 PGM T1.1

**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on :	
VCC12	15V
VCC3	7V
CARD_5V	7V
CARD_3V	7V
DRVREN, SGNL_VLD, CARD_V_VLD & RESET	7V
RESET	V _{CC} +.7V
All Others	V _{CC} +.7V
Output Short Circuit Current	100mA
Lead Solder Temperature (10 secs)	300°C

COMMENT

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS (Over Recommended Operating Conditions)

Symbol	Parameter	Conditions	Min	Max	Units
I _{CC1}	Power Supply Current	Operating		150	μA
I _{CC2}	Power Supply Current	E ² PROM Access		3	mA
V _{TRIP5}	Host 5 Volt Sense Trip Level		4.5	4.75	V
V _{CARD5}	Backend 5 Volt Sense Trip Level		4.5	4.75	V
V _{TRIP3}	Host 3 Volt Sense Trip Level		2.8	3.0	V
V _{CARD3}	Backend 3 Volt Sense Trip Level		2.8	3.0	V
I _{LI}	Input Leakage Current			2	μA
I _{LO}	Output Leakage Current			10	μA
V _{IL}	Input Low Voltage		-0.1	0.8	V
V _{IH}	Input High Voltage		2	V _{CC} +1	V
V _{OL}	Output Low Voltage	V _{CC} = 5.0V, I _{OL} = 2.1mA		0.4	V
V _{OH}	Output High Voltage	V _{CC} = 5.0V, I _{OH} = -400μA	2.4		V
V _{OLRS}	RESET Output Low Voltage	I _{OL} = 1mA		0.4	V
V _{OHRS}	RESET Output High Voltage	I _{OH} = -400 mA	V _{CC} -.75V		V

2024 PGM T2.1

**MEMORY AC OPERATING CHARACTERISTICS (Over Recommended Operating Conditions)**

Symbol	Parameter	Conditions	Min	Max	Units
t _{CS}	CS Setup Time			50	ns
t _{CSH}	CS Hold Time			0	ns
t _{DIS}	DI Setup Time		100		ns
t _{DIH}	DI Hold Time		100		ns
t _{PD1}	Output Delay to 1			250	ns
t _{PD0}	Output Delay to 0			250	ns
t _{HZ}	Output Delay to Hi-Z			100	ns
t _{EW}	Program/Erase Time			10	ms
t _{CSMIN}	Minimum CS Low Time		250		ns
t _{SKHI}	Minimum SK Low Time		250		ns
t _{SV}	Output Delay to Status Valid			250	ns
SK _{MAX}	Maximum Clock Frequency			1	MHZ

2024 PGM T3.0

SEQUENCER AC OPERATING CHARACTERISTICS (Over Recommended Operating Conditions)

Symbol	Parameter	Notes	Min	Max	Units
T _{SLEW}	Slew Rate			250	V/Sec
T _{HSE}	High Side Enable Delay	Card Insertion Noise Filter	100	200	ms
V _{TRHST}	Trip Point Hysteresis		7		mV
t _{PURST}	Power-up Reset Timeout		100	200	ms
t _{RESET}	External Reset Timeout	HST_RST Release Delay	100	200	ms
t _{RPD}	V _{TRIP} to RESET output Delay			5	μs
V _{RVALID}	RESET Output Valid		1		V
t _{GLTICH}	Glitch Reject Pulse Width			40	ns

2024 PGM T4.1

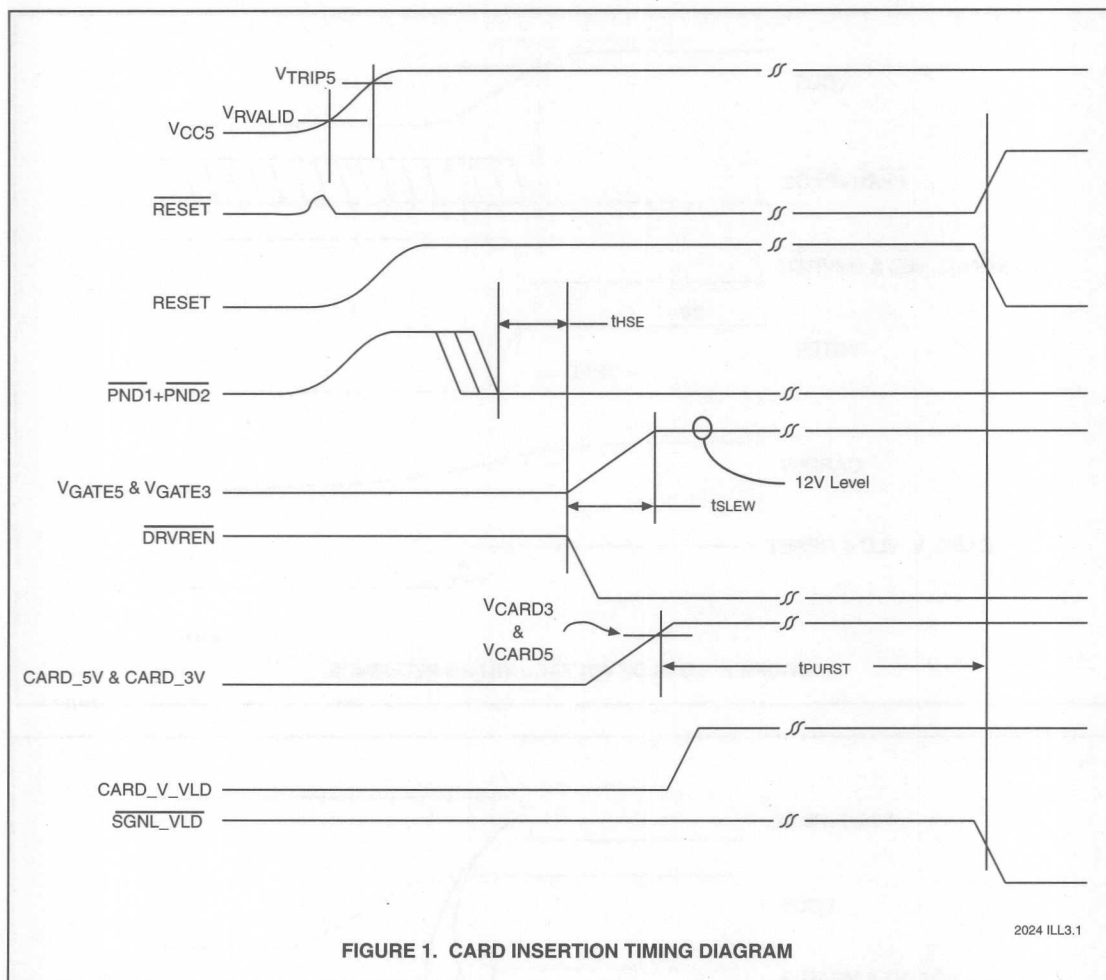
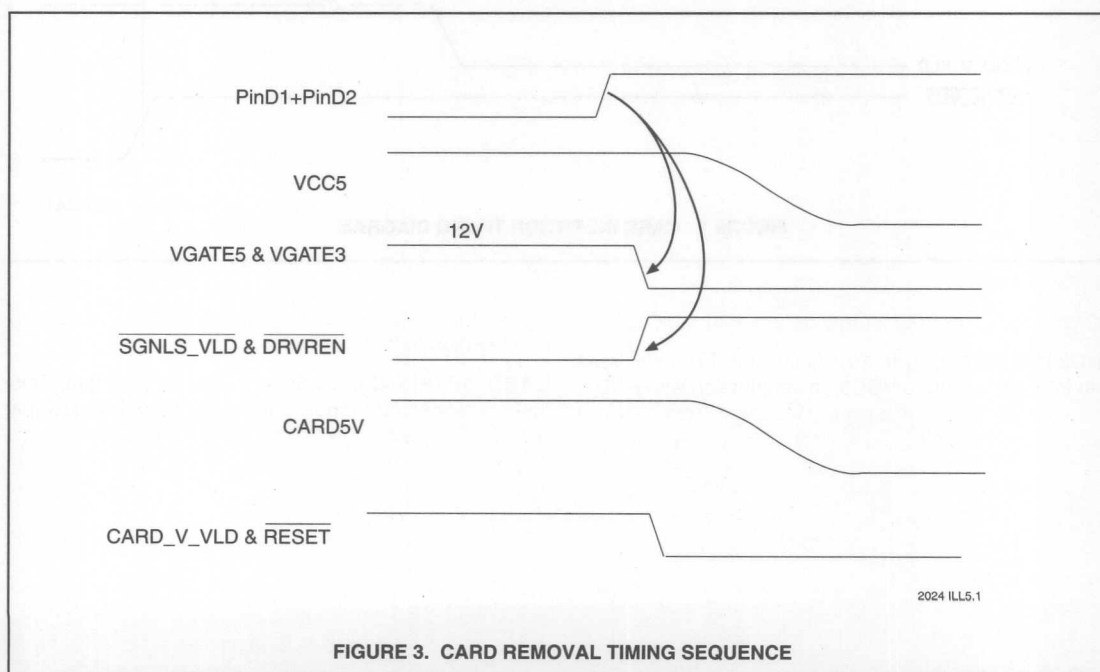
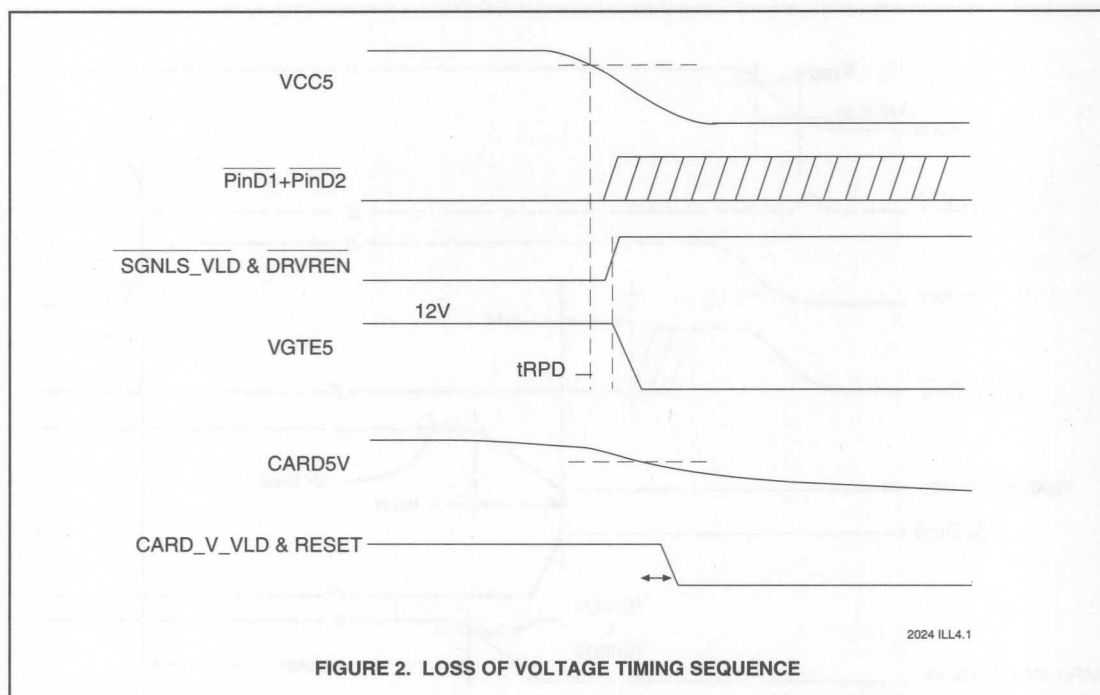


FIGURE 1. CARD INSERTION TIMING DIAGRAM



**PIN DESCRIPTIONS****PIN NAME [CompactPCI name] (pin #)**

VCC12 (Pin 1): Supplies the 12 volts required for powering the high-side drivers.

DRVREN (Pin 2): Open drain, active low output indicates the status of the 3 volt and 5 volt high side driver outputs (VGATE5 and VGATE3). This signal may also be used as a switching signal for the 12 volt supply.

ISLEW (Pin 3): Diode-connected NFET input may be used to adjust the 250V/s default slew rate of the high-side driver outputs. One quarter of the current injected into this pin will be mirrored into each of the high-side driver outputs.

VSEL (Pin 4): TTL level input used to determine which of the Host power supply inputs will be monitored for valid voltage and reset generation.

VSEL-Voltage Select	Host Voltage Monitored
Low	5 Volt or Mixed-Mode
High	3.3 Volt Only

DD (Pin 5): A high going edge on this input will place the embedded memory into Data Download mode. This mode allows the entire contents of the E²PROM array to be read out of the device by selecting the device (CS high) and providing clock cycles on the SK input. Data Download mode is exited when Chip Select is brought low.

CS (Pin 6): E²PROM memory chip select, active high.

SK (Pin 7): E²PROM memory serial clock input.

DI (Pin 8): E²PROM memory data input.

DO (Pin 9): E²PROM memory data output.

PND2 [BD_SEL2#] (Pin 10): Active low TTL level input with internal pull-up to VCC5. In conjunction with PND1, this signal indicates proper card insertion. This pin must be connected to ground on the host side of the connector. PND1 and PND2 must be placed on opposite corners of the connector and will preferably be staggered shorter than the power connector pins. Board insertion is assumed when PND1 and PND2 are low.

PND1 [BD_SEL1#] (Pin 11): Active low TTL level input with internal pull-up to VCC5. In conjunction with PND2, this signal indicates proper card insertion.

GND (Pin 12): Ground.

CARD_V_VLD (pin13): CARD_V_VLD is an open drain output, indicating the card side voltages are at or above V_{TRIP}.

SGNL_VLD (Pin 14): Signals valid (SGNL_VLD) is an open drain active low signal indicating the card side power is valid and that the reset signals have been released. This signal can be used by the host as an indication that the bus interface is active and all signals are valid.

HST_PWR (pin15): The host power (HST_PWR) input is an active high input. It provides the host system active control over the sequencing of the power up operation. When low, the S39421 will hold the add-in card in reset and block all power to the backend logic. When HST_PWR is high the power sequencing will begin immediately and the reset outputs will be driven active after t_{PURST}.

HST_RST [PCI_RST#] (Pin 16): TTL level input used as a reset input signal from the host interface. An active low level longer than 40 nsec will cause a reset sequence to be performed on the card. The power switching logic will not be affected.

RESET (Pin 17): RESET is an active low open-drain output. It should be tied high through a pull-up resistor connected to V_{CC}.

RESET (Pin 18): RESET is an active high open drain (PFET) output. It should be tied low through a pull-down resistor connected to ground.

CARD_3V (Pin 19): 3.3 volt card side supply input. This input is monitored for power integrity. If it falls below the 3.3V sense threshold, the PWR_VLD signal is de-asserted and a RESET sequence initiates.

VGATE3 (Pin 20): Slew rate limited high side driver output for the 3.3V external Power FET gate.

VCC3 (Pin 21): 3.3 volt host side supply input. This input is monitored for power integrity. If it falls below the 3.3V sense threshold, the SGNL_VLD signal is de-asserted and the high side drivers disabled.

CARD_5V (Pin 22): 5 volt card side supply input. This input is monitored for power integrity. If it falls below the 5V sense threshold and the VSEL input is low, the PWR_VLD signal is de-asserted and a RESET sequence initiates.

VGATE5 (Pin 23): Slew rate limited high side driver output for the 5V external Power FET gate.

VCC5 (Pin 24): Power to the S39421 and 5 volt host side supply input. This input is monitored for power integrity. If it falls below the 5V sense threshold and the VSEL input is low, the SGNL_VLD signal is de-asserted and the high side drivers disabled.



DEVICE OPERATION

Power-Up Sequence

A sequencing operation is initiated by the physical insertion of the card into the platform's connector. The S39421's VCC5 pin should be connected to the early power pins of the connector. As soon as power is applied, the S39421 will drive the reset outputs active and clamp the VGATE outputs to ground.

Proper card insertion is insured by detecting the presence of a low level on the pin detect (PND1, PND2) inputs, which should be located on opposite ends of the bus connector. These pin detect inputs have internal pull-up resistors and the connection on the host platform side must be connected directly to ground. [In a *CompactPCI* application these are the BD_SEL# signals]. The PND inputs have an internal noise filter nominally set at 150ms. Once the proper card insertion has been detected, the S39421 will check the status of the HST_PWR signal from the host.

Implementation of HST_PWR is optional; e.g. it can be used to power down individual cards on the bus via software control. If it is not used by the host system the input must be held high in order for the S39421 to enable power sequencing to the card.

Once these basic conditions are met the S39421 will begin the power-up portion of the sequence. First, the host platform supplies are checked for compliance. Based on the state of the VSEL input the S39421 will monitor the +5V and +3.3V supplies. If these are above the VTRIP thresholds the sequencing next begins the backend logic power-on operation.

The S39421 will drive the VGATE3 and VGATE5 outputs to the 12V rail to turn on the external 3 volt and 5 volt power FETs. The slew rate of these outputs defaults to 250V/s.

Different slew rates can be accommodated by either adding an additional capacitor between the FET gate and ground or by injecting current into the ISLEW input.

RESET CONTROL

The S39421 will now monitor the backend card voltages on pins CARD-5V and CARD_3V. When these inputs are above their respective VTRIP levels the S39421 will release PWR_VLD.

If the HST_RST [PCI_RST#] input is released (pulled high) the S39421 will begin timing out its reset function and release reset to the card after t_{PURST} . With the release of the reset outputs, the S39421 will drive the SGNL_VLD output.

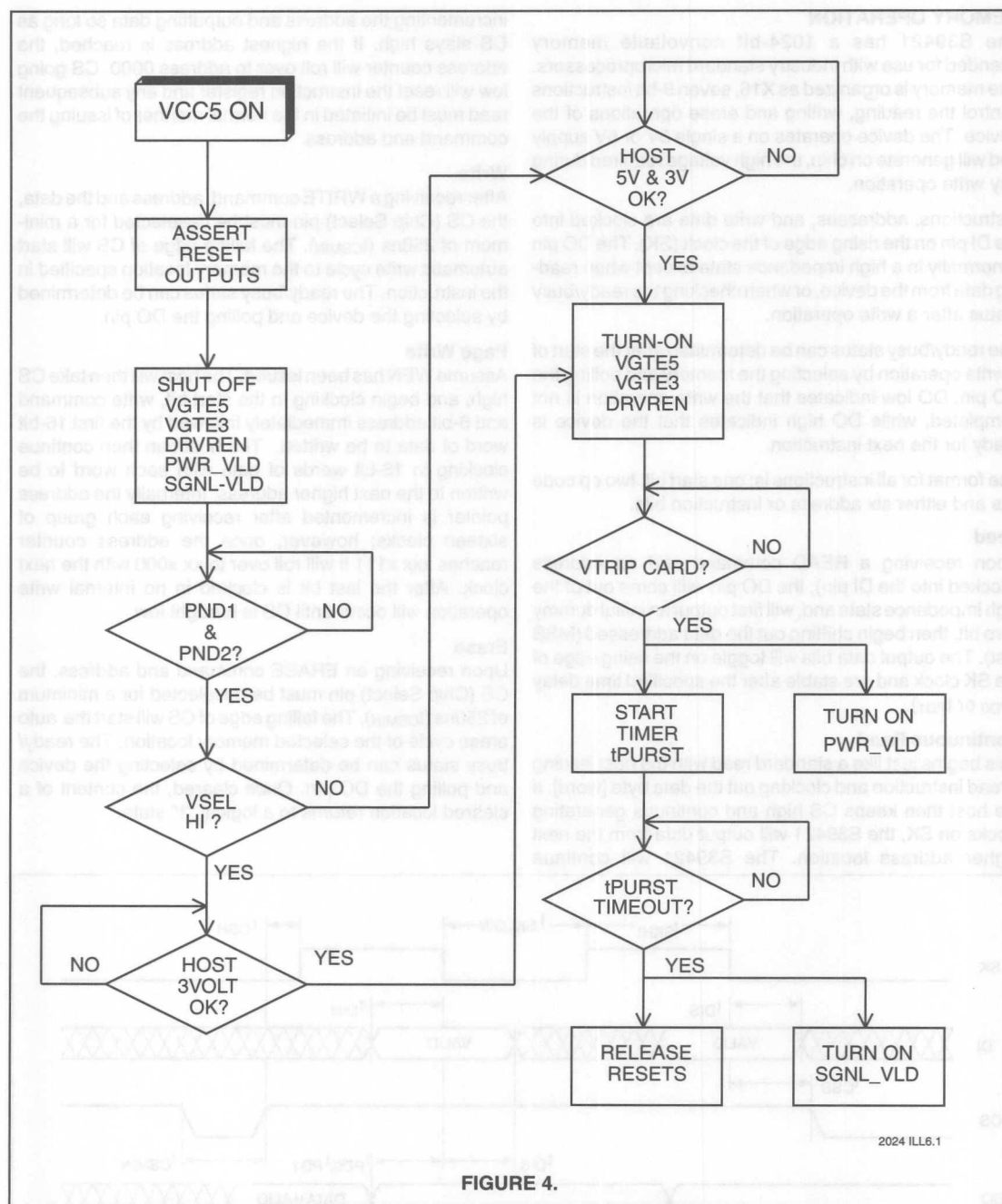
During normal operation, the supply voltages are continuously monitored. If the cardside supplies fall below the VTRIP levels the reset outputs will be driven active. If the host platform supplies fall below VTRIP, the S39421 will immediately assert the reset outputs and disable the highside drivers.

Power Configurations

The S39421 can be used in 5V-only, 3.3V-only and mixed voltage systems. For mixed voltage systems, simply connect the appropriate bus and card power inputs as indicated. The VSEL pin should be grounded.

For systems with a single power supply, connect VCC5 and VCC3 together to the platform host early power line (long pin power supply). Also connect CARD5V and CARD3V together to the cardside power output of the FET.

The state of VSEL determines the reset level that will be used to signal CARD_V_VLD. For 3.3V systems, tie VSEL to the supply; for 5V systems, tie VSEL to ground.



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FIGURE 4.

**MEMORY OPERATION**

The S39421 has a 1024-bit nonvolatile memory intended for use with industry standard microprocessors. The memory is organized as X16, seven 9-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the memory and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction.

The format for all instructions is: one start bit; two op code bits and either six address or instruction bits.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Continuous Read

This begins just like a standard read with the host issuing a read instruction and clocking out the data byte [word]. If the host then keeps CS high and continues generating clocks on SK, the S39421 will output data from the next higher address location. The S39421 will continue

incrementing the address and outputting data so long as CS stays high. If the highest address is reached, the address counter will roll over to address 0000. CS going low will reset the instruction register and any subsequent read must be initiated in the normal manner of issuing the command and address.

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start automatic write cycle to the memory location specified in the instruction. The ready/busy status can be determined by selecting the device and polling the DO pin.

Page Write

Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 6-bit address immediately followed by the first 16-bit word of data to be written. The host can then continue clocking in 16-bit words of data with each word to be written to the next higher address. Internally the address pointer is incremented after receiving each group of sixteen clocks; however, once the address counter reaches xxx x111 it will roll over to xx x000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

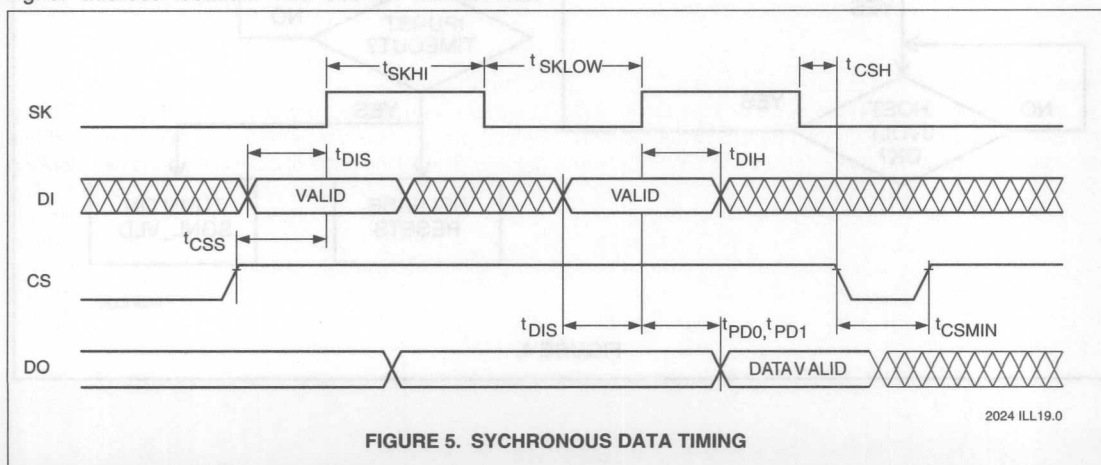
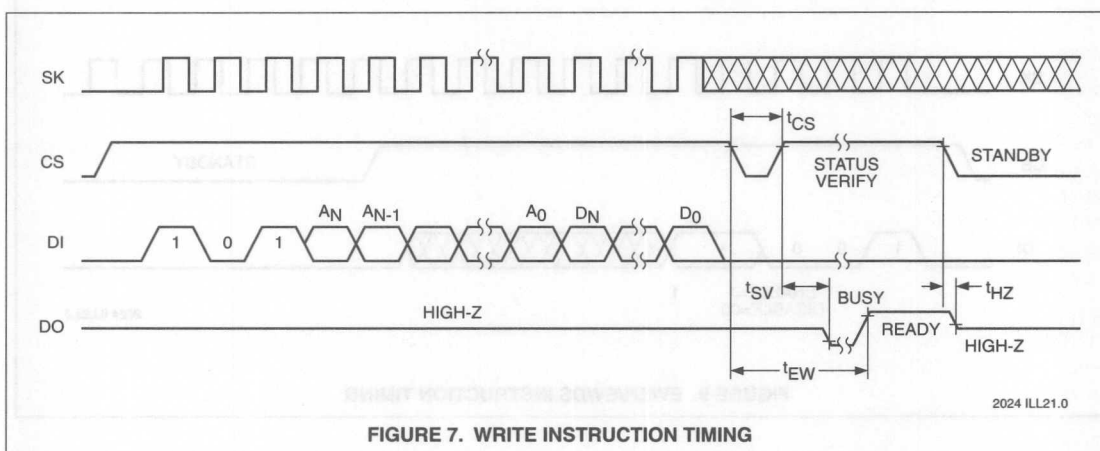
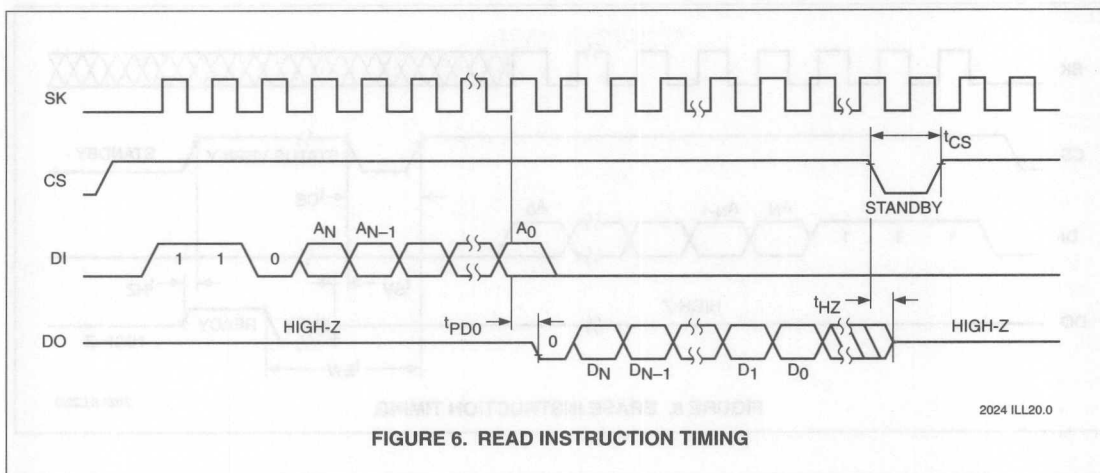


FIGURE 5. SYNCHRONOUS DATA TIMING

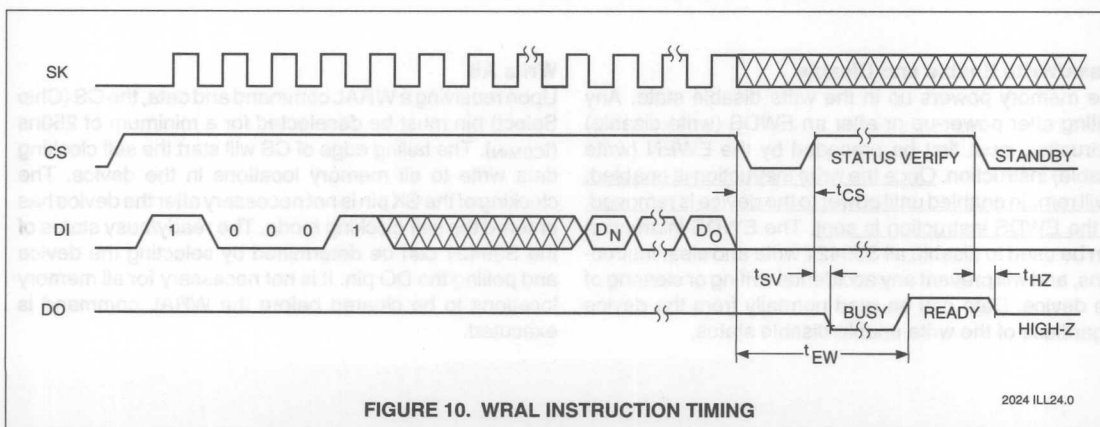
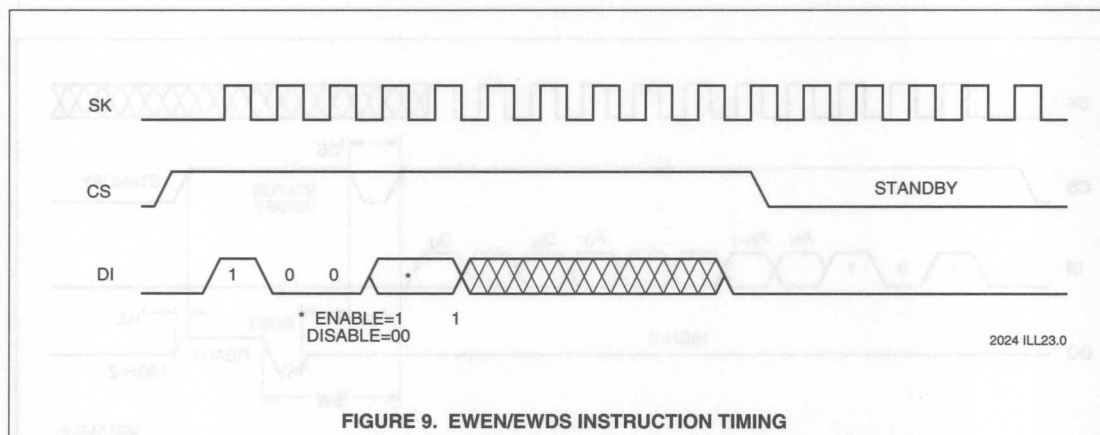
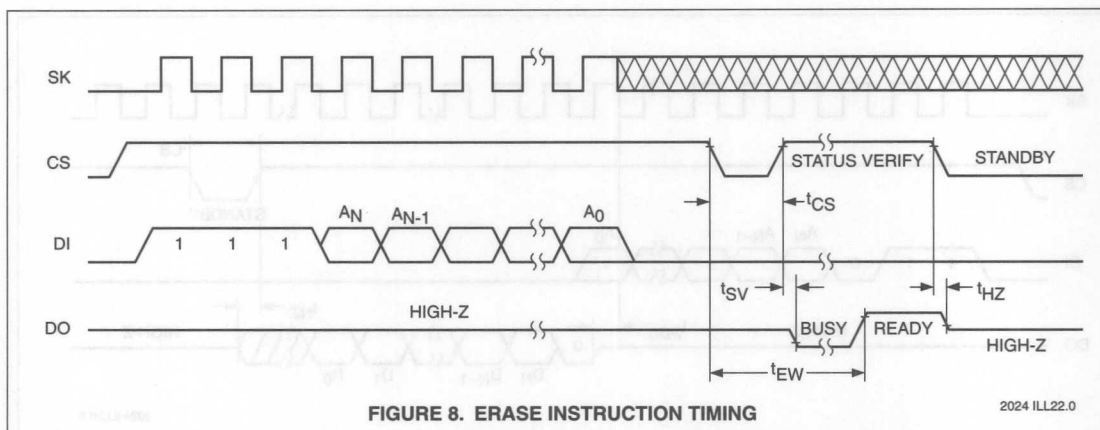


Erase/Write Enable and Disable

The memory powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all S39421 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S39421 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.



**INSTRUCTION SET**

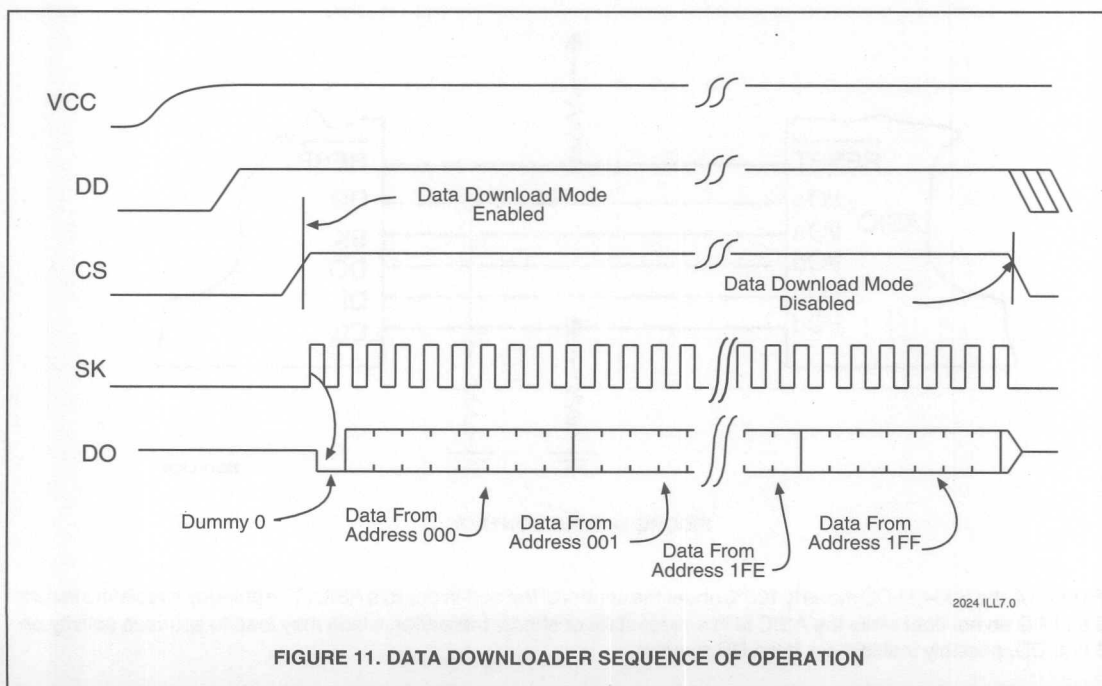
Instruction	Start Bit	Opcode	Address	Data	Comments
			x16	x16	
READ	1	10	x(A5–A0)		Read Address AN–A0
ERASE	1	11	x(A5–A0)		Clear Address AN–A0
WRITE	1	01	x(A5–A0)	D15–D0	Write Address AN–A0
EWEN	1	00	11xxxx		Write Enable
EWDS	1	00	00xxxx		Write Disable
WRAL	1	00	01xxxx	D15–D0	Write All Addresses

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Data Download Mode

The Data Download mode is an alternative method of accessing the E²PROM memory. Use of this mode allows downloading the entire contents of the memory without entering any commands. The DD mode is enabled after a low to high transition on the DD pin, while continuing to assert CS (this includes powering up the device with DD tied high). Also, as a condition to enter this mode, the device must not be in a state of reset. Once in Data Download mode, the device will wait until Chip Select is

driven active. At this point, the device will output a dummy '0' followed by the contents of location 0000. As long as the SK line is toggled the S39421 will continue to output the contents of sequential address locations. In this manner, the configuration data that is loaded into an interface device can be accessed in a simple manner without requiring the logic of the interface chip to generate the complex signals needed for the microwire interface. Data Download mode is exited upon the first high to low transition of the Chip Select input.





Data Download Control

There are a number of ways to implement the data download mode of operation. For applications that do not require use of this feature, simply ground the DD pin and disable the function altogether.

In Figure 13, DD is tied to V_{CC} through a pull-up resistor. This will allow only a single download after power on. The actual download function would not be enabled until t_{PURST} had expired and CS was brought high. As soon as CS is deselected the DD mode will be disabled. The primary disadvantage to this method is the lack of a reload after brownout. The DD mode may or may not be initiated depending on how low the power is cycled.

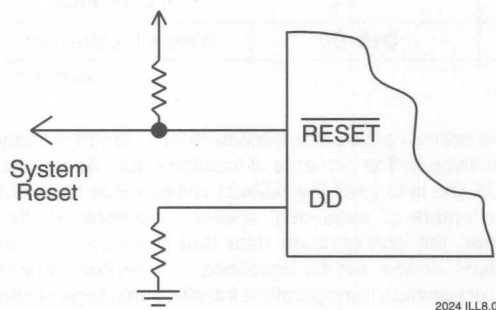


FIGURE 12. DD DISABLED

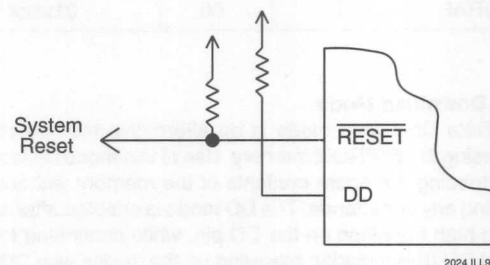


FIGURE 13. ONE TIME DOWNLOAD

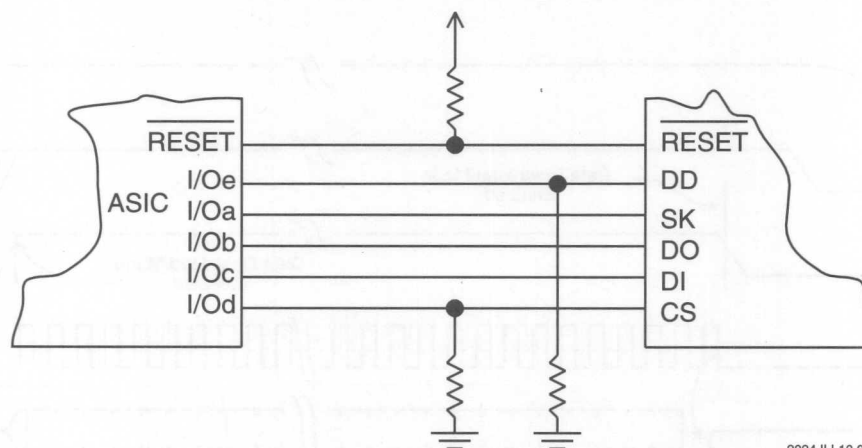
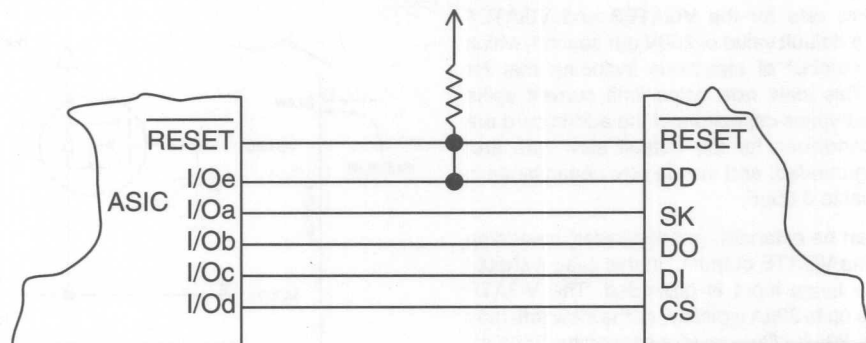


FIGURE 14. ASIC CONTROL

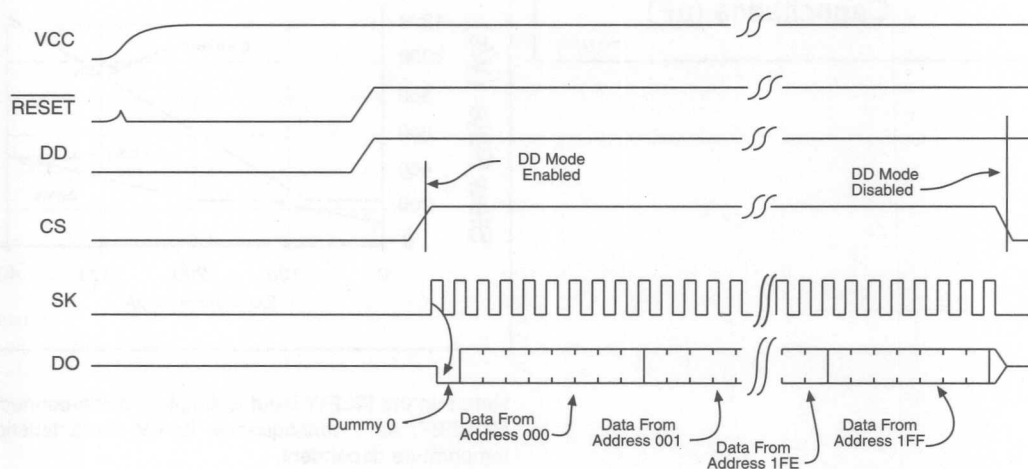
In Figure 14, the S39421 DD mode is 100% under the control of the add-in board's ASIC. The pull-down resistors insure CS and DD do not float while the ASIC is in a reset state or shortly thereafter, which may lead to spurious activity on CS and DD, possibly indicating a false DD request.



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FIGURE 15. DOWNLOAD ENABLED IN CONJUNCTION WITH RESET RELEASE

Figure 15 is a good implementation to use whenever there is a requirement to download data from the memory after any reset cycle. This provides control of the DD input function after power-on, brown-out or a system induced reset condition. In this way the data download function is ready under any circumstance an ASIC or MCU might need to reload initialization data.



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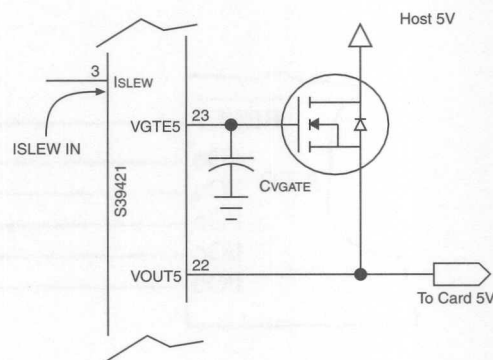
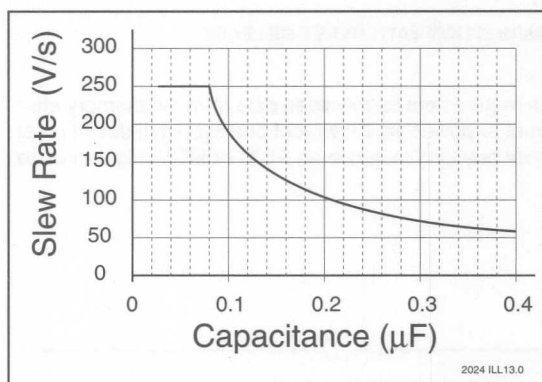
FIGURE 16. DD CIRCUIT 4 TIMING SEQUENCE DIAGRAM



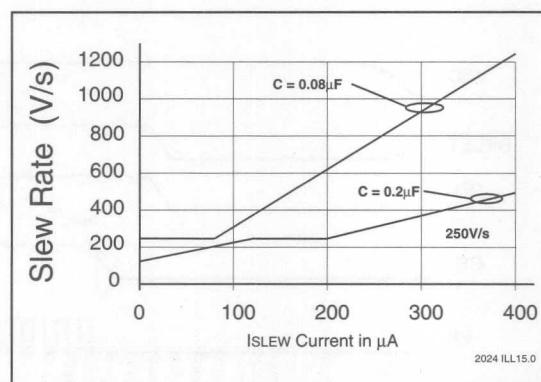
Slew Rate Control

The nominal slew rate for the VGATE3 and VGATE5 outputs is set at a default value of 250V per second, which conforms to a number of standards including that for Compact PCI. This slew rate helps limit current spike transients as the bypass capacitors of the add-in card are charged. The conditions for the default slew rate are: ISLEW input is grounded; and the C_{VGATE} capacitance is less than or equal to $0.08\mu\text{F}$.

The slew rate can be extended (made slower) by adding capacitance to the VGATE outputs. In this case it should be assumed the ISLEW input is grounded. The VGATE outputs can drive up to $20\mu\text{A}$ typically, so the slew rate may be calculated as $20\mu\text{A} \div C_{VGATE}$ (not exceeding 250V/s). Refer to Graph 1 shown below.

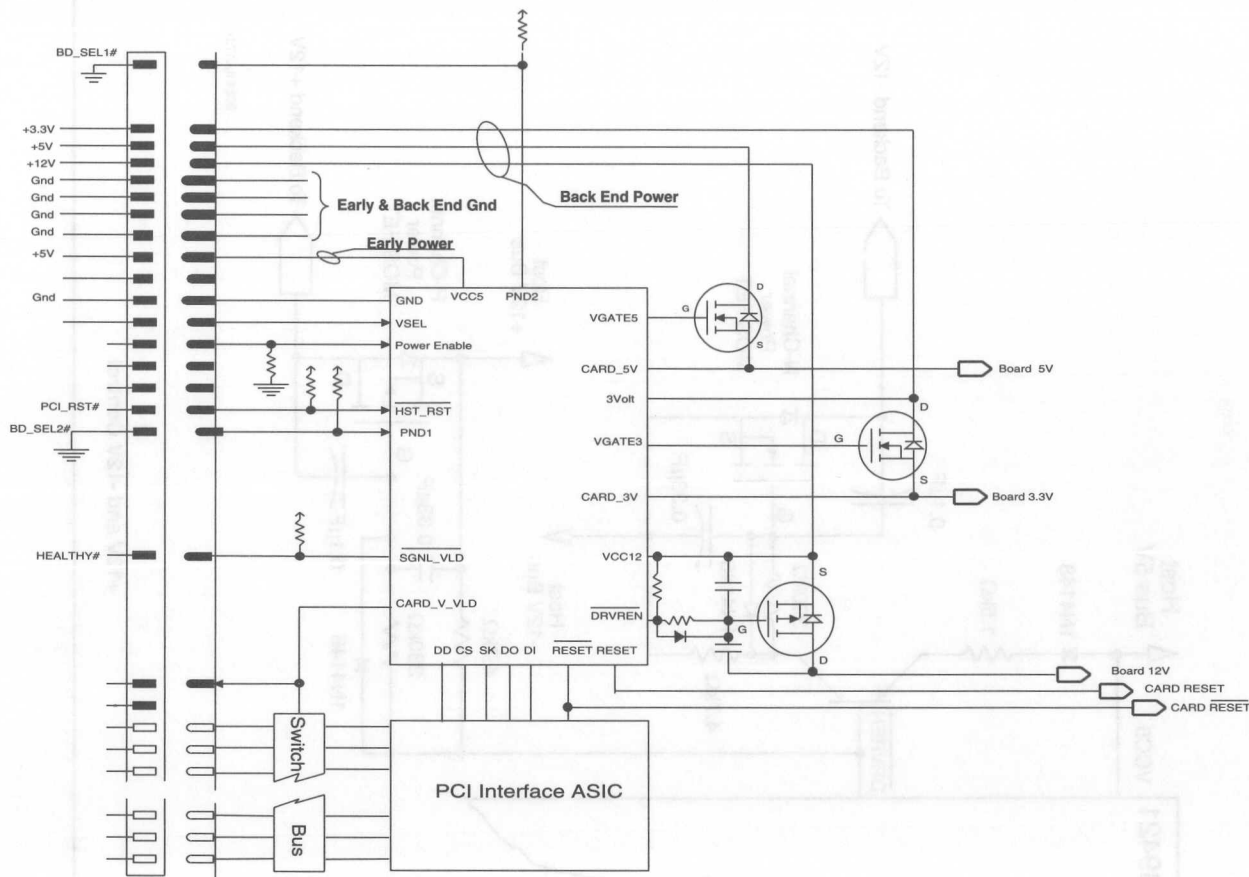


The slew rate can be increased (made faster) by injecting current into the ISLEW input. One quarter of the current injected into ISLEW will be mirrored out of the VGATE drivers. The resulting slew rate may be calculated as $\text{ISLEW} \div 4 \times C_{VGATE}$ (not less than 250V/s). Example slew rates are plotted to illustrate the effects of capacitance on the VGATE output in Graph 2. The reason for the flat portion of the graph is that the internal slew rate control operates in parallel to add as much as $20\mu\text{A}$ (typically) to help keep the SR at 250V/s.



Note that the ISLEW input is simply a diode-connected MOSFET. As a consequence, its I-V characteristic is temperature dependent.

TYPICAL PCI INTERFACE SCHEMATIC

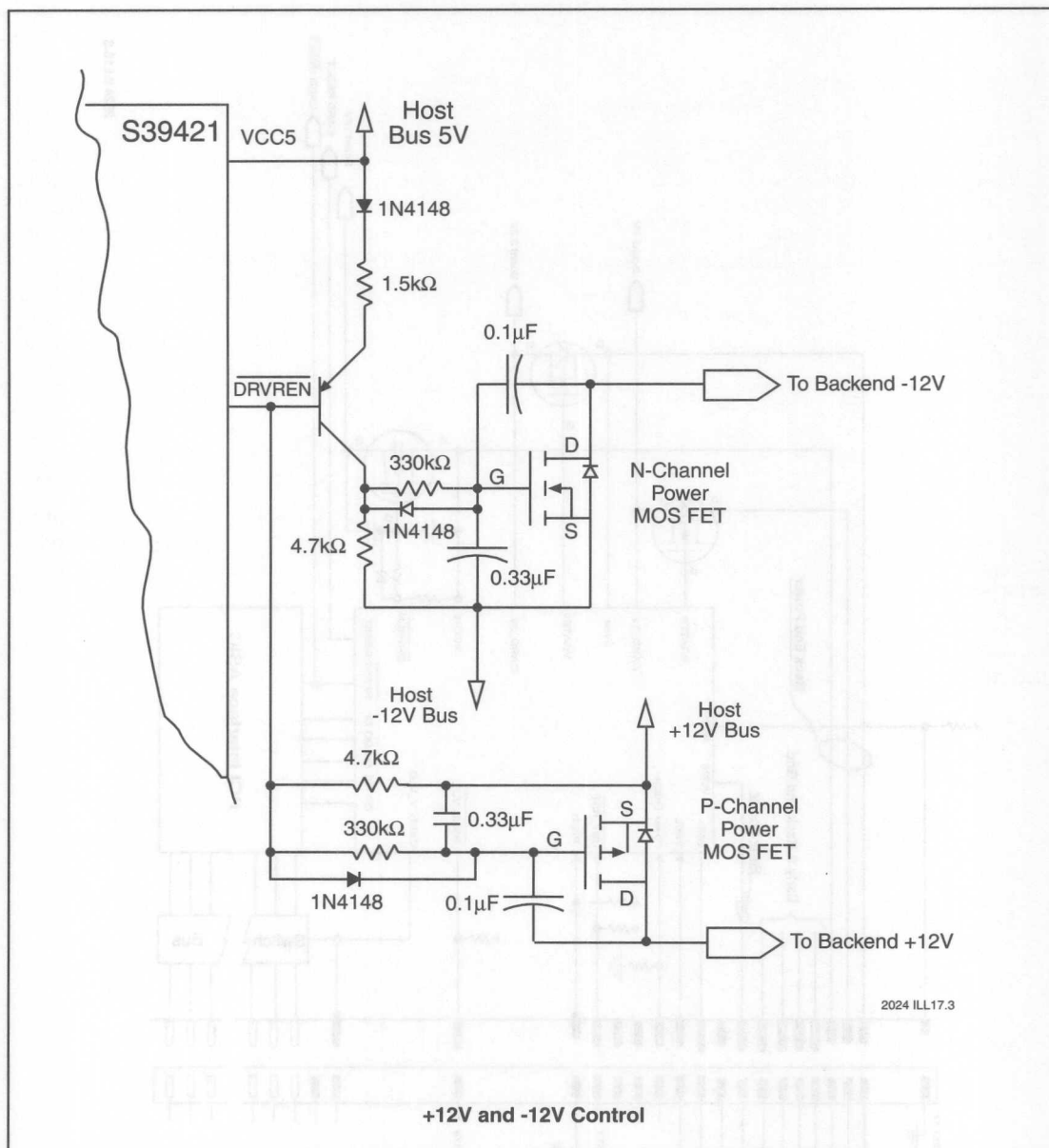


2024 ILL16.3



Applications
Aid

S39421





FEATURES

- Full Voltage Control for Hot Swap Applications
 - Card Insertion Detection
 - Platform Voltage Detection
 - Card Voltage Sequencing
 - 5 Volt, 12 Volt and 3.3 Volt
- 12 Volt FET Enable Outputs
 - Allows use of Low On-resistance N-Channel FETS
- Card Reset Generation Based on Out of Spec Voltages
 - Host Reset
- Programmable Slew Rate Control [250V/Sec Default Rate]
- Supports 5 Volt, 3.3 Volt and Mixed Voltage Cards
- Integrated 4K Bit E²PROM Memory
- Data Download™ Mode [Simplifies Downloading of Configuration Memory into Interface ASIC or MCU]

DESCRIPTION

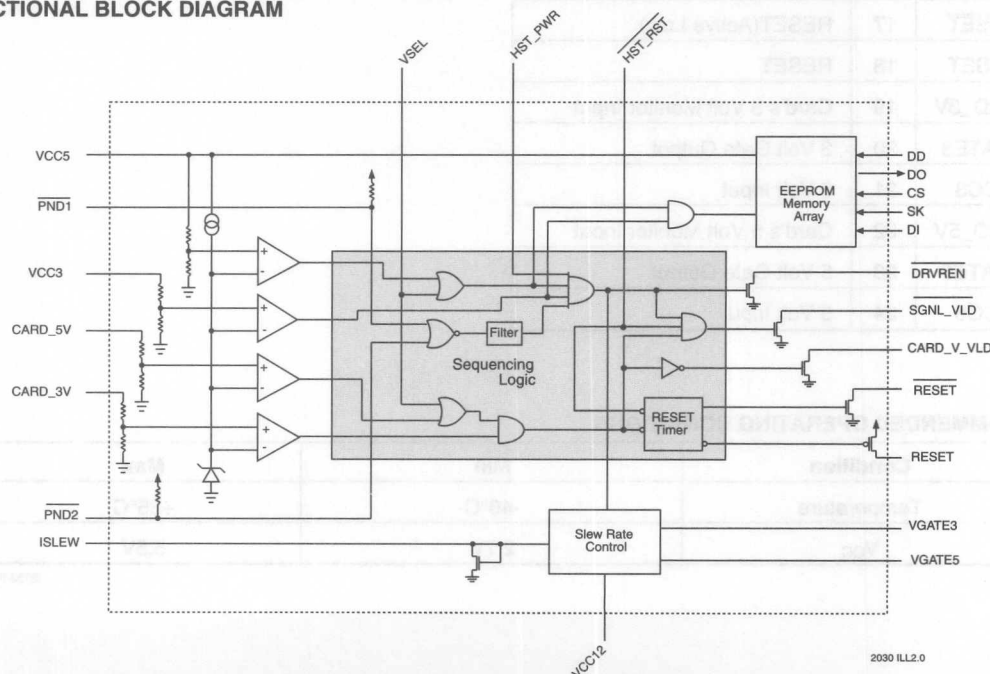
The S39424 is a fully integrated hot swap controller intended for use on add-in cards that may be inserted into or removed from powered-on host platforms. The S39424 performs a variety of tasks starting with the validation of proper card insertion and the presence of "in-spec" voltages at the host platform interface.

Once power is switched on, the S39424 continues to monitor the back-end power to the add-in card and the host power supply. If either the 5V or 3.3V supplies drop below V_{trip} the S39424 will immediately assert the RESET outputs and power-down the add-in card.

In addition to the power control for the add-in card, the S39424 provides status signals that can be employed by the host and for the control of bus interface components.

The on board E²PROM can be used as configuration memory for the individual card or as general purpose memory. The proprietary DataDownload mode provides a more direct interface to the E²PROM for simplified access by the add-in card's controller or ASIC.

FUNCTIONAL BLOCK DIAGRAM

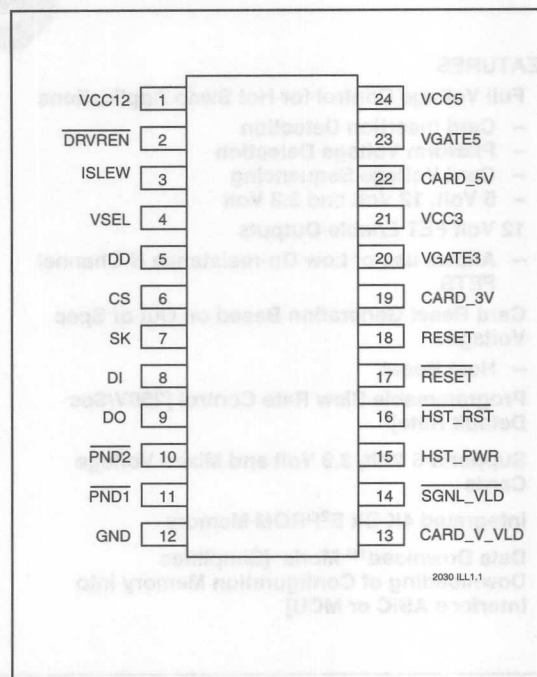


**S39424**

Preliminary

PIN CONFIGURATION

Symbol	Pin	Description
VCC12	1	12 Volt Input
DRVREN	2	High Side Driver Enable (L)
ISLEW	3	Slew Rate Control
VSEL	4	Voltage Select
DD	5	Data Download Enable
CS	6	Microwire Chip Select
SK	7	Microwire Serial Clock
DI	8	Microwire Data In
DO	9	Microwire Data Out
PND2	10	Pin Detect 2 (Active Low)
PND1	11	Pin Detect 1 (Active Low)
GND	12	Ground
CARD_V_VLD	13	Card Voltage Valid
SGNL_VLD	14	Signals Valid (Active Low)
HST_PWR	15	Host Power Up Enable
HST_RST	16	Host Reset (Active Low)
RESET	17	RESET(Active Low)
RESET	18	RESET
CARD_3V	19	Card's 3 Volt Monitor Input
VGATE3	20	3 Volt Gate Output
VCC3	21	3 Volt Input
CARD_5V	22	Card's 5 Volt Monitor Input
VGATE5	23	5 Volt Gate Output
VCC5	24	5 Volt Input

**RECOMMENDED OPERATING CONDITIONS**

Condition	Min	Max
Temperature	-40°C	+85°C
V _{CC}	2.7V	5.5V

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**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on :	
VCC12	15V
VCC3	7V
CARD_5V	7V
CARD_3V	7V
DRVREN, SGNL_VLD, CARD_V_VLD & RESET	7V
RESET	V _{CC} +.7V
All Others	V _{CC} +.7V
Output Short Circuit Current	100mA
Lead Solder Temperature (10 secs)	300°C

COMMENT

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

DC OPERATING CHARACTERISTICS (Over Recommended Operating Conditions)

Symbol	Parameter	Conditions	Min	Max	Units
I _{CC1}	Power Supply Current	Operating		150	μA
I _{CC2}	Power Supply Current	E ² PROM Access		3	mA
V _{TRIP5}	Host 5 Volt Sense Trip Level		4.5	4.75	V
V _{CARD5}	Backend 5 Volt Sense Trip Level		4.5	4.75	V
V _{TRIP3}	Host 3 Volt Sense Trip Level		2.8	3.0	V
V _{CARD3}	Backend 3 Volt Sense Trip Level		2.8	3.0	V
I _{LI}	Input Leakage Current			2	μA
I _{LO}	Output Leakage Current			10	μA
V _{IL}	Input Low Voltage		-0.1	0.8	V
V _{IH}	Input High Voltage		2	V _{CC} +1	V
V _{OL}	Output Low Voltage	V _{CC} = 5.0V, I _{OL} = 2.1mA		0.4	V
V _{OH}	Output High Voltage	V _{CC} = 5.0V, I _{OH} = -400μA	2.4		V
V _{OLRS}	RESET Output Low Voltage	I _{OL} = 1mA		0.4	V
V _{OHRS}	RESET Output High Voltage	I _{OH} = -400 mA	V _{CC} -.75V		V

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**S39424**

Preliminary

MEMORY AC OPERATING CHARACTERISTICS (Over Recommended Operating Conditions)

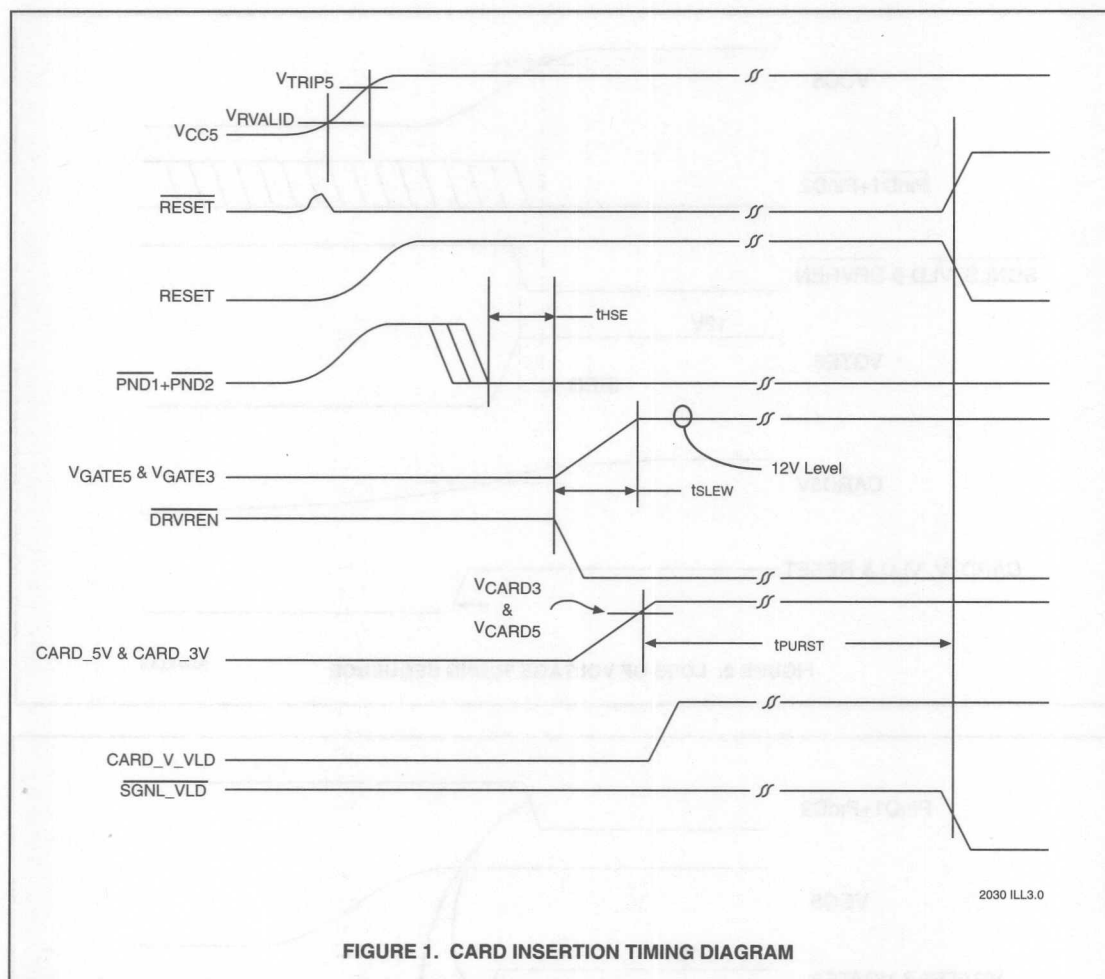
Symbol	Parameter	Conditions	Min	Max	Units
t _{CS}	CS Setup Time			50	ns
t _{CSH}	CS Hold Time			0	ns
t _{DIS}	DI Setup Time		100		ns
t _{DIH}	DI Hold Time		100		ns
t _{PD1}	Output Delay to 1			250	ns
t _{PD0}	Output Delay to 0			250	ns
t _{HZ}	Output Delay to Hi-Z			100	ns
t _{EW}	Program/Erase Time			10	ms
t _{CSMIN}	Minimum CS Low Time		250		ns
t _{SKHI}	Minimum SK Low Time		250		ns
t _{SV}	Output Delay to Status Valid			250	ns
SK _{MAX}	Maximum Clock Frequency			1	MHZ

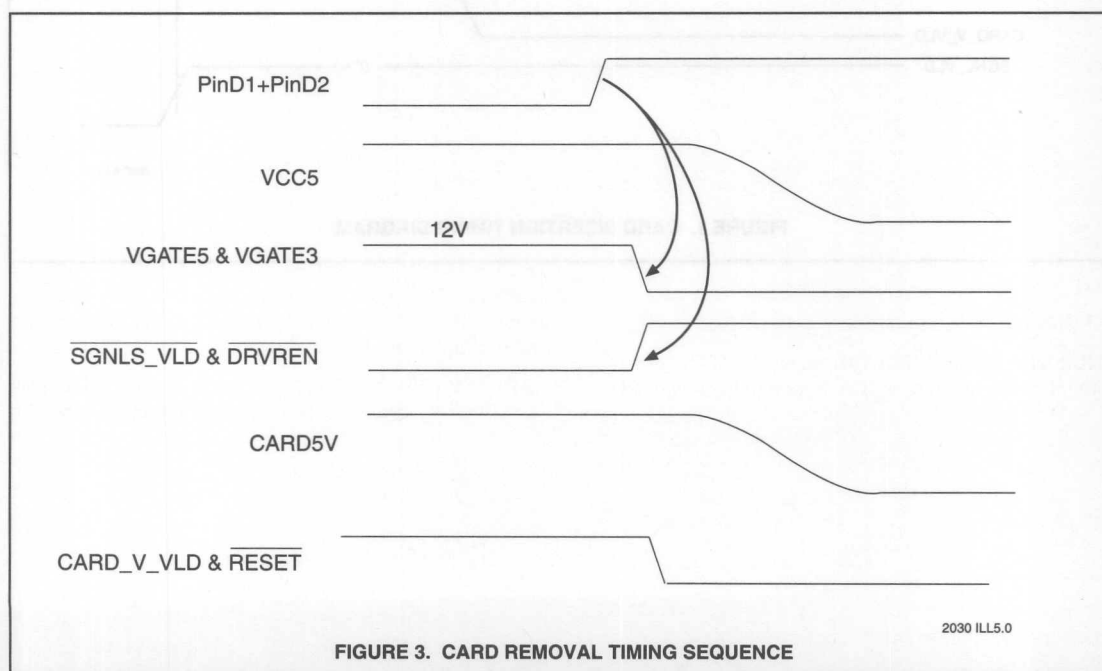
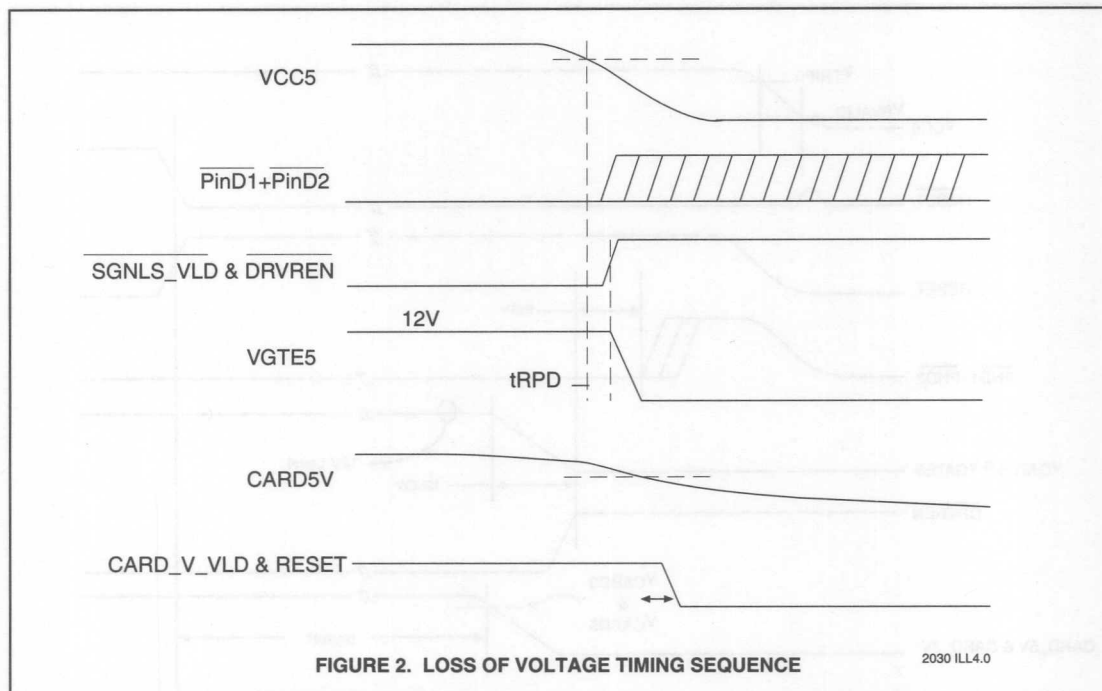
2030 PGM T3.0

SEQUENCER AC OPERATING CHARACTERISTICS (Over Recommended Operating Conditions)

Symbol	Parameter	Notes	Min	Max	Units
T _{SLEW}	Slew Rate			250	V/Sec
T _{HSE}	High Side Enable Delay	Card Insertion Noise Filter	100	200	ms
V _{TRHST}	Trip Point Hysteresis		7		mV
t _{PURST}	Power-up Reset Timeout		100	200	ms
t _{RESET}	External Reset Timeout	HST_RST Release Delay	100	200	ms
t _{RPD}	V _{TRIP} to RESET output Delay			5	μs
V _{RVALID}	RESET Output Valid		1		V
t _{GLTICH}	Glitch Reject Pulse Width			40	ns

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**FIGURE 1. CARD INSERTION TIMING DIAGRAM**



**PIN DESCRIPTIONS****PIN NAME [CompactPCI name] (pin #)**

VCC12 (Pin 1): Supplies the 12 volts required for powering the high-side drivers.

DRVREN (Pin 2): Open drain, active low output indicates the status of the 3 volt and 5 volt high side driver outputs (VGATE5 and VGATE3). This signal may also be used as a switching signal for the 12 volt supply.

ISLEW (Pin 3): Diode-connected NFET input may be used to adjust the 250V/s default slew rate of the high-side driver outputs. One quarter of the current injected into this pin will be mirrored into each of the high-side driver outputs.

VSEL (Pin 4): TTL level input used to determine which of the Host power supply inputs will be monitored for valid voltage and reset generation.

VSEL-Voltage Select	Host Voltage Monitored
Low	5 Volt or Mixed-Mode
High	3.3 Volt Only

DD (Pin 5): A high going edge on this input will place the embedded memory into Data Download mode. This mode allows the entire contents of the E²PROM array to be read out of the device by selecting the device (CS high) and providing clock cycles on the SK input. Data Download mode is exited when Chip Select is brought low.

CS (Pin 6): E²PROM memory chip select, active high.

SK (Pin 7): E²PROM memory serial clock input.

DI (Pin 8): E²PROM memory data input.

DO (Pin 9): E²PROM memory data output.

PND2 [BD_SEL2#] (Pin 10): Active low TTL level input with internal pull-up to VCC5. In conjunction with PND1, this signal indicates proper card insertion. This pin must be connected to ground on the host side of the connector. PND1 and PND2 must be placed on opposite corners of the connector and will preferably be staggered shorter than the power connector pins. Board insertion is assumed when PND1 and PND2 are low.

PND1 [BD_SEL1#] (Pin 11): Active low TTL level input with internal pull-up to VCC5. In conjunction with PND2, this signal indicates proper card insertion.

GND (Pin 12): Ground.

CARD_V_VLD (pin13): CARD_V_VLD is an open drain output, indicating the card side voltages are at or above V_{TRIP}.

SGNL_VLD (Pin 14): Signals valid (SGNL_VLD) is an open drain active low signal indicating the card side power is valid and that the reset signals have been released. This signal can be used by the host as an indication that the bus interface is active and all signals are valid.

HST_PWR (pin15): The host power (HST_PWR) input is an active high input. It provides the host system active control over the sequencing of the power up operation. When low, the S39424 will hold the add-in card in reset and block all power to the backend logic. When HST_PWR is high the power sequencing will begin immediately and the reset outputs will be driven active after t_{PURST}.

HST_RST [PCI_RST#] (Pin 16): TTL level input used as a reset input signal from the host interface. An active low level longer than 40 nsec will cause a reset sequence to be performed on the card. The power switching logic will not be affected.

RESET (Pin 17): RESET is an active low open-drain output. It should be tied high through a pull-up resistor connected to V_{CC}.

RESET (Pin 18): RESET is an active high open drain (PFET) output. It should be tied low through a pull-down resistor connected to ground.

CARD_3V (Pin 19): 3.3 volt card side supply input. This input is monitored for power integrity. If it falls below the 3.3V sense threshold, the PWR_VLD signal is de-asserted and a RESET sequence initiates.

VGATE3 (Pin 20): Slew rate limited high side driver output for the 3.3V external Power FET gate.

VCC3 (Pin 21): 3.3 volt host side supply input. This input is monitored for power integrity. If it falls below the 3.3V sense threshold, the SGNL_VLD signal is de-asserted and the high side drivers disabled.

CARD_5V (Pin 22): 5 volt card side supply input. This input is monitored for power integrity. If it falls below the 5V sense threshold and the VSEL input is low, the PWR_VLD signal is de-asserted and a RESET sequence initiates.

VGATE5 (Pin 23): Slew rate limited high side driver output for the 5V external Power FET gate.

VCC5 (Pin 24): Power to the S39424 and 5 volt host side supply input. This input is monitored for power integrity. If it falls below the 5V sense threshold and the VSEL input is low, the SGNL_VLD signal is de-asserted and the high side drivers disabled.

**DEVICE OPERATION****Power-Up Sequence**

A sequencing operation is initiated by the physical insertion of the card into the platform's connector. The S39424's VCC5 pin should be connected to the early power pins of the connector. As soon as power is applied, the S39424 will drive the reset outputs active and clamp the VGATE outputs to ground.

Proper card insertion is insured by detecting the presence of a low level on the pin detect (PND1, PND2) inputs, which should be located on opposite ends of the bus connector. These pin detect inputs have internal pull-up resistors and the connection on the host platform side must be connected directly to ground. [In a *CompactPCI* application these are the BD_SEL# signals]. The PND inputs have an internal noise filter nominally set at 150ms. Once the proper card insertion has been detected, the S39424 will check the status of the HST_PWR signal from the host.

Implementation of HST_PWR is optional; e.g. it can be used to power down individual cards on the bus via software control. If it is not used by the host system the input must be held high in order for the S39424 to enable power sequencing to the card.

Once these basic conditions are met the S39424 will begin the power-up portion of the sequence. First, the host platform supplies are checked for compliance. Based on the state of the VSEL input the S39424 will monitor the +5V and +3.3V supplies. If these are above the VTRIP thresholds the sequencing next begins the backend logic power-on operation.

The S39424 will drive the VGATE3 and VGATE5 outputs to the 12V rail to turn on the external 3 volt and 5 volt power FETs. The slew rate of these outputs defaults to 250V/s.

Different slew rates can be accommodated by either adding an additional capacitor between the FET gate and ground or by injecting current into the ISLEW input.

RESET CONTROL

The S39424 will now monitor the backend card voltages on pins CARD_5V and CARD_3V. When these inputs are above their respective VTRIP levels the S39424 will release PWR_VLD.

If the HST_RST [PCI_RST#] input is released (pulled high) the S39424 will begin timing out its reset function and release reset to the card after t_{PRST}. With the release of the reset outputs, the S39424 will drive the SGNL_VLD output.

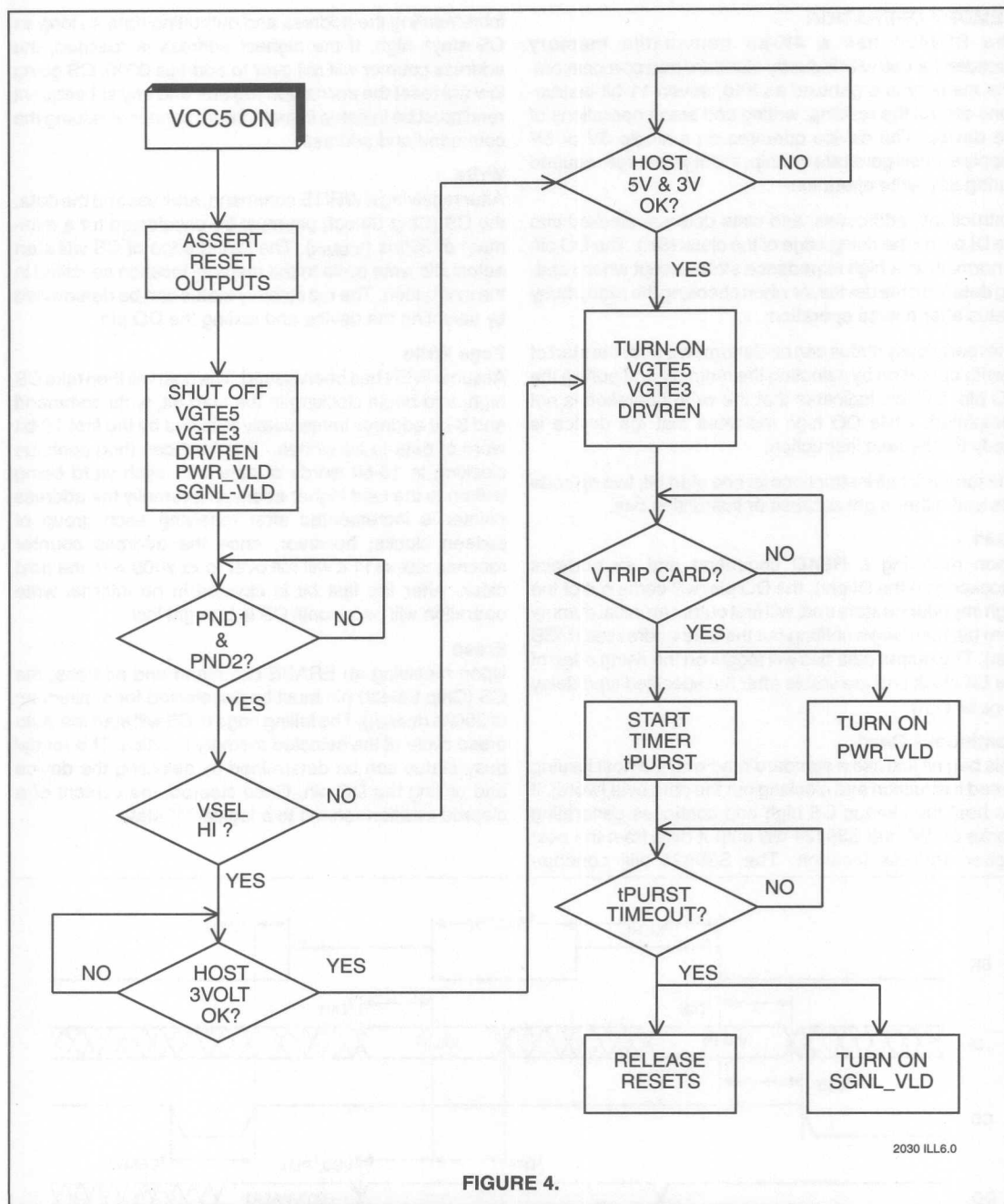
During normal operation, the supply voltages are continuously monitored. If the cardside supplies fall below the VTRIP levels the reset outputs will be driven active. If the host platform supplies fall below VTRIP, the S39424 will immediately assert the reset outputs and disable the highside drivers.

Power Configurations

The S39424 can be used in 5V-only, 3.3V-only and mixed voltage systems. For mixed voltage systems, simply connect the appropriate bus and card power inputs as indicated. The VSEL pin should be grounded.

For systems with a single power supply, connect VCC5 and VCC3 together to the platform host early power line (long pin power supply). Also connect CARD5V and CARD3V together to the cardside power output of the FET.

The state of VSEL determines the reset level that will be used to signal CARD_V_VLD. For 3.3V systems, tie VSEL to the supply; for 5V systems, tie VSEL to ground.



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FIGURE 4.

**MEMORY OPERATION**

The S39424 has a 4K-bit nonvolatile memory intended for use with industry standard microprocessors. The memory is organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the memory and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction.

The format for all instructions is: one start bit; two op code bits and either eight address or instruction bits.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Continuous Read

This begins just like a standard read with the host issuing a read instruction and clocking out the data byte [word]. If the host then keeps CS high and continues generating clocks on SK, the S39424 will output data from the next higher address location. The S39424 will continue

incrementing the address and outputting data so long as CS stays high. If the highest address is reached, the address counter will roll over to address 0000. CS going low will reset the instruction register and any subsequent read must be initiated in the normal manner of issuing the command and address.

Write

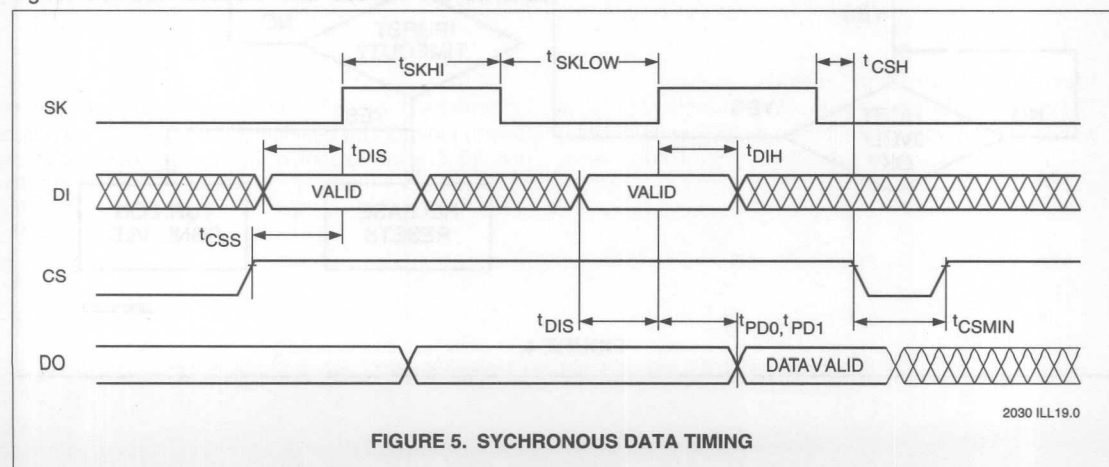
After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start automatic write cycle to the memory location specified in the instruction. The ready/busy status can be determined by selecting the device and polling the DO pin.

Page Write

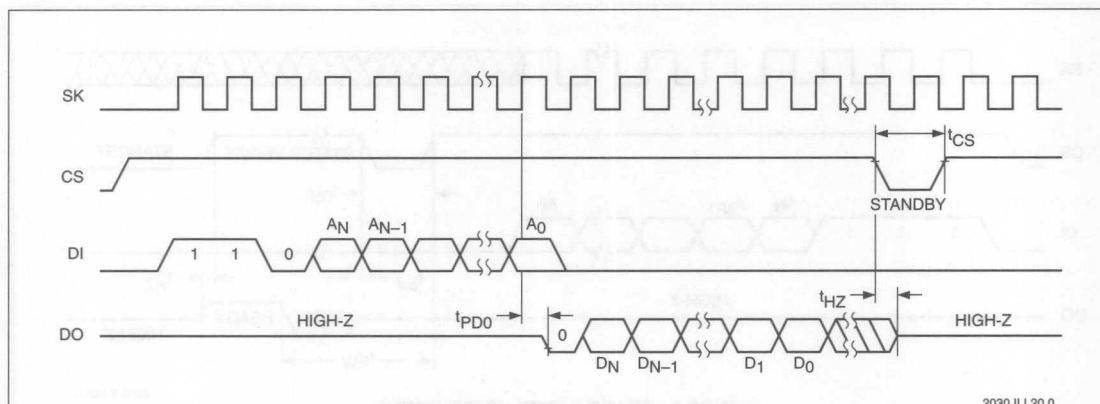
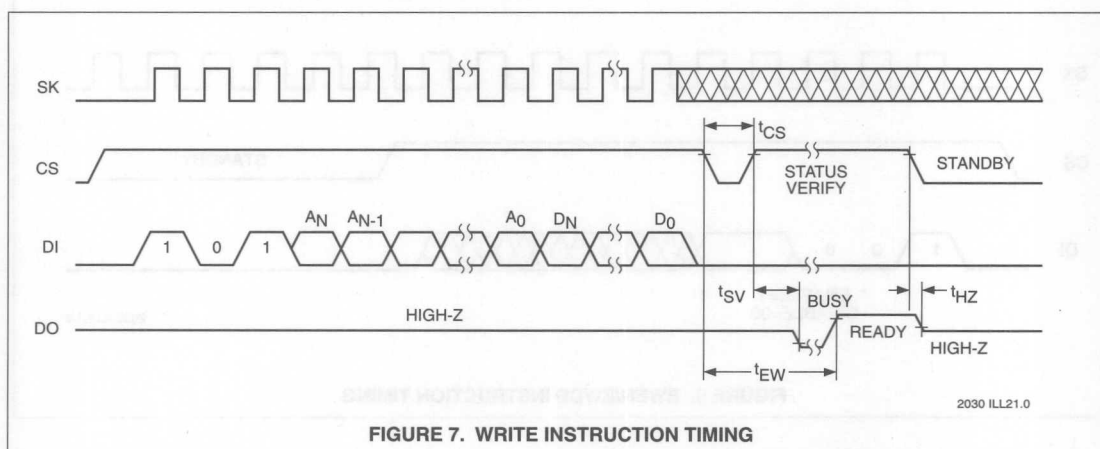
Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 8-bit address immediately followed by the first 16-bit word of data to be written. The host can then continue clocking in 16-bit words of data with each word being written to the next higher address. Internally the address pointer is incremented after receiving each group of sixteen clocks; however, once the address counter reaches xxx x111 it will roll over to xx x000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

**FIGURE 5. SYNCHRONOUS DATA TIMING**

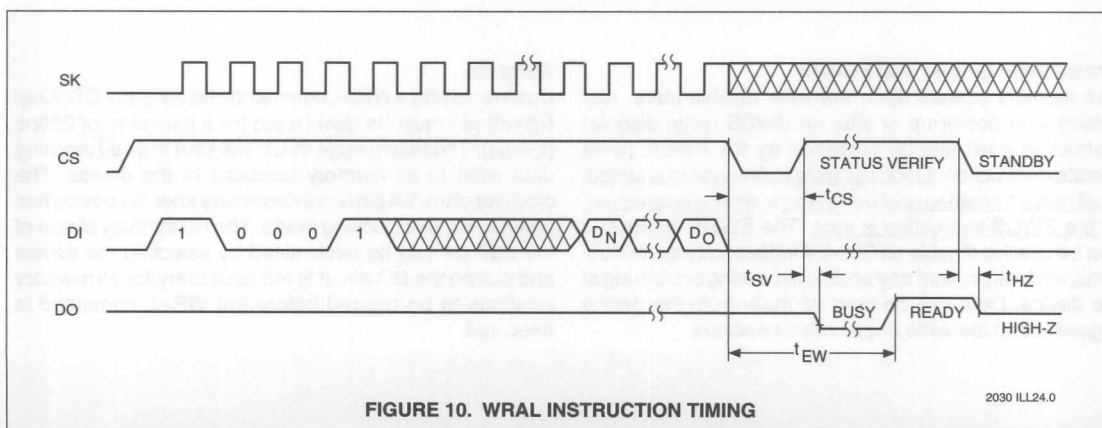
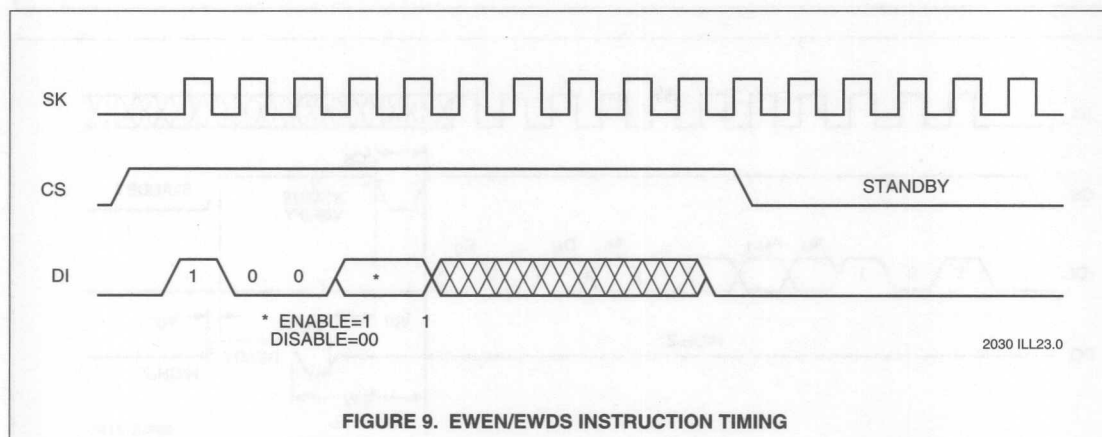
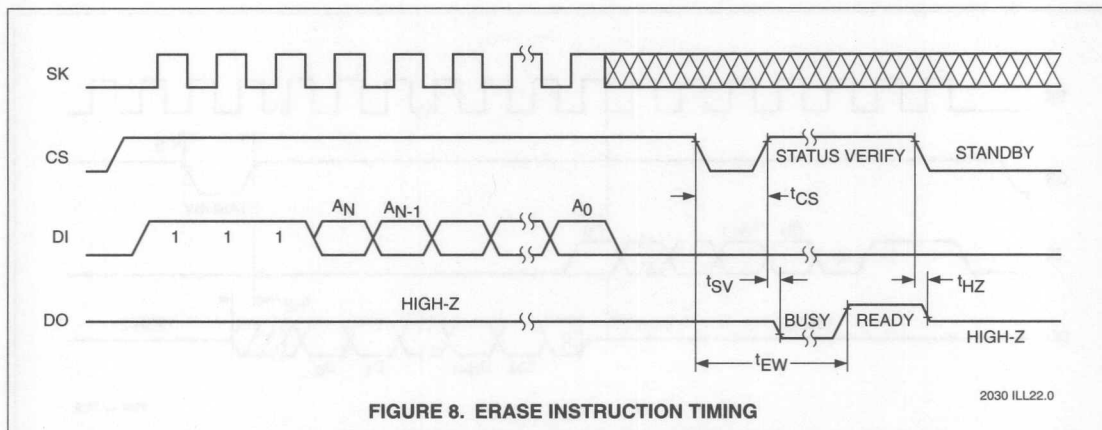
2030 ILL19.0

**FIGURE 6. READ INSTRUCTION TIMING****FIGURE 7. WRITE INSTRUCTION TIMING****Erase/Write Enable and Disable**

The memory powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all S39424 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S39424 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.



**INSTRUCTION SET**

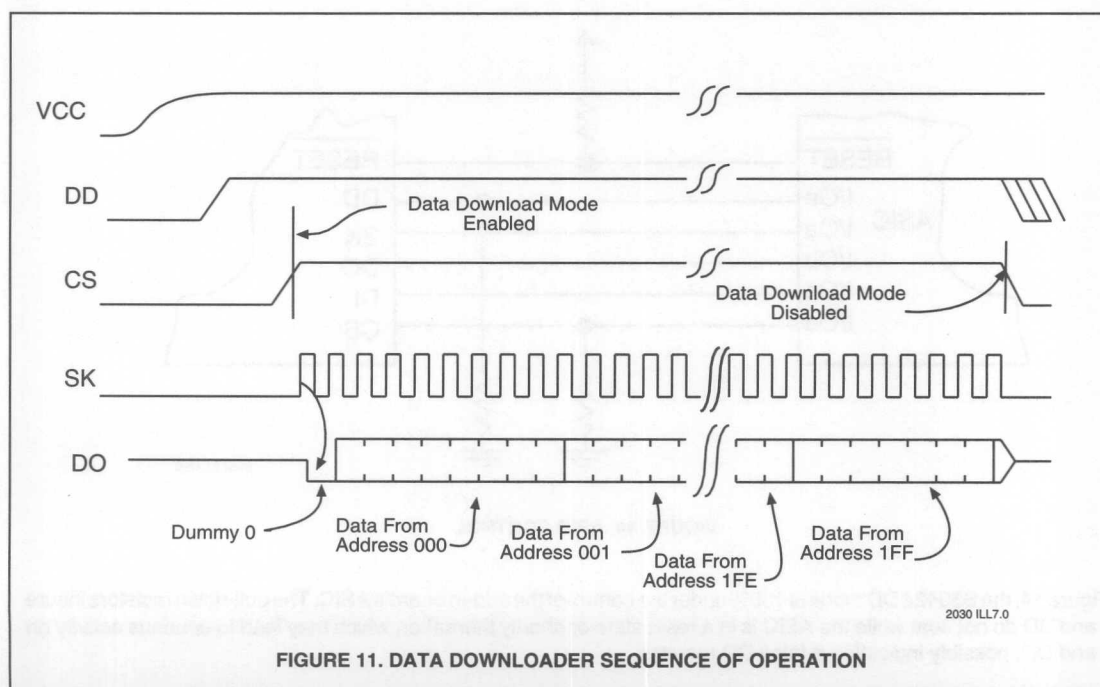
Instruction	Start Bit	Opcode	Address	Data	Comments
			x16	x16	
READ	1	10	x(A7-A0)		Read Address AN-A0
ERASE	1	11	x(A7-A0)		Clear Address AN-A0
WRITE	1	01	x(A7-A0)	D15-D0	Write Address AN-A0
EWEN	1	00	11xxxxxx		Write Enable
EWDS	1	00	00xxxxxx		Write Disable
WRAL	1	00	01xxxxxx	D15-D0	Write All Addresses

2030 PGM T5.0

Data Download Mode

The Data Download mode is an alternative method of accessing the E²PROM memory. Use of this mode allows downloading the entire contents of the memory without entering any commands. The DD mode is enabled after a low to high transition on the DD pin, while continuing to assert DD (this includes powering up the device with DD tied high). Also, as a condition to enter this mode, the device must not be in a state of reset. Once in Data Download mode, the device will wait until Chip Select is

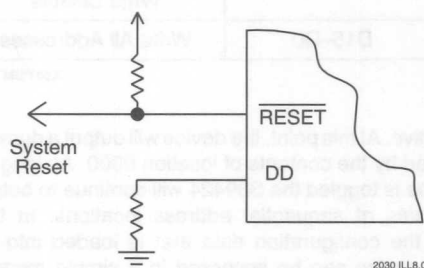
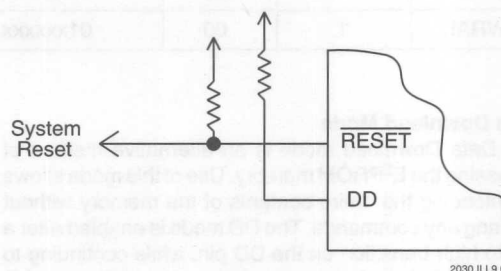
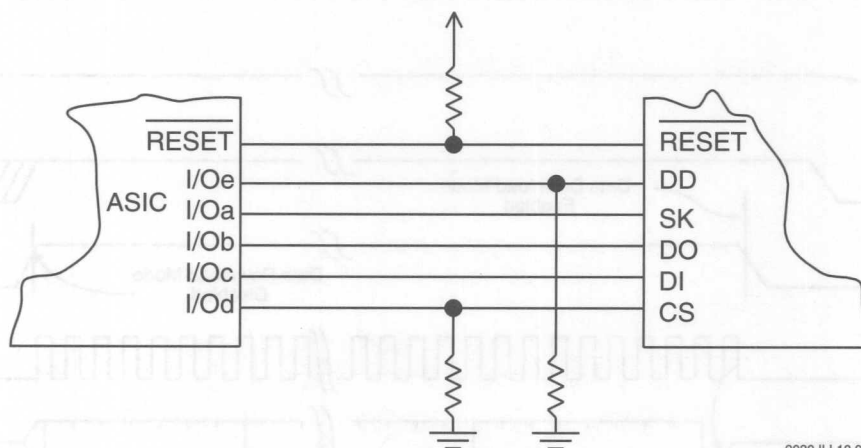
driven active. At this point, the device will output a dummy '0' followed by the contents of location 0000. As long as the SK line is toggled the S39424 will continue to output the contents of sequential address locations. In this manner, the configuration data that is loaded into an interface device can be accessed in a simple manner without requiring the logic of the interface chip to generate the complex signals needed for the microwire interface. Data Download mode is exited upon the first high to low transition of the Chip Select input.



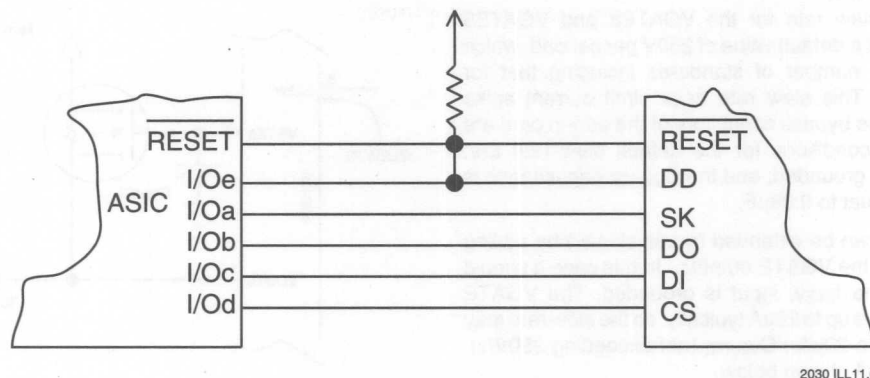
**Data Download Control**

There are a number of ways to implement the data download mode of operation. For applications that do not require use of this feature, simply ground the DD pin and disable the function altogether.

In Figure 13, DD is tied to V_{CC} through a pull-up resistor. This will allow only a single download after power on. The actual download function would not be enabled until t_{PURST} had expired and CS was brought high. As soon as CS is deselected the DD mode will be disabled. The primary disadvantage to this method is the lack of a reload after brownout. The DD mode may or may not be initiated depending on how low the power is cycled.

**FIGURE 12. DD DISABLED****FIGURE 13. ONE TIME DOWNLOAD****FIGURE 14. ASIC CONTROL**

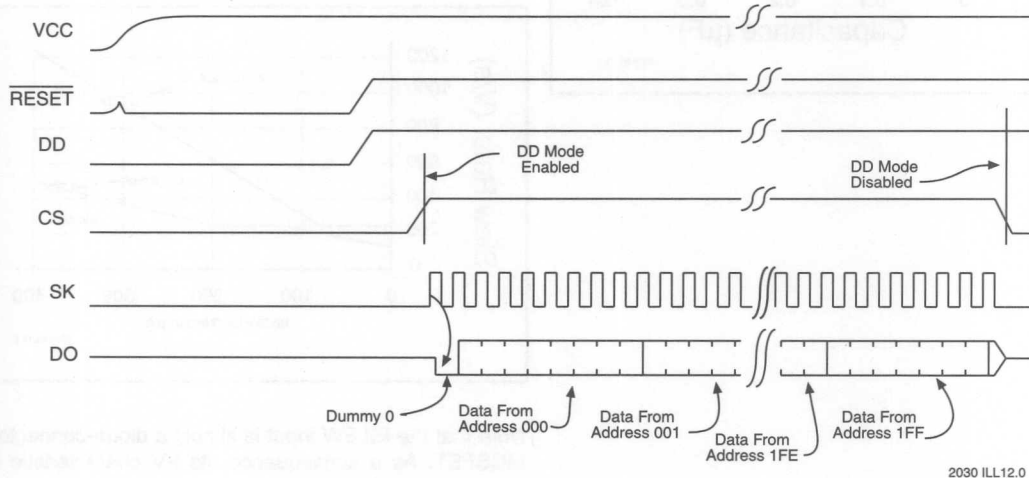
In Figure 14, the S39424 DD mode is 100% under the control of the add-in board's ASIC. The pull-down resistors insure CS and DD do not float while the ASIC is in a reset state or shortly thereafter, which may lead to spurious activity on CS and DD, possibly indicating a false DD request.



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FIGURE 15. DOWNLOAD ENABLED IN CONJUNCTION WITH RESET RELEASE

Figure 15 is a good implementation to use whenever there is a requirement to download data from the memory after any reset cycle. This provides control of the DD input function after power-on, brown-out or a system induced reset condition. In this way the data download function is ready under any circumstance an ASIC or MCU might need to reload initialization data.



2030 ILL12.0

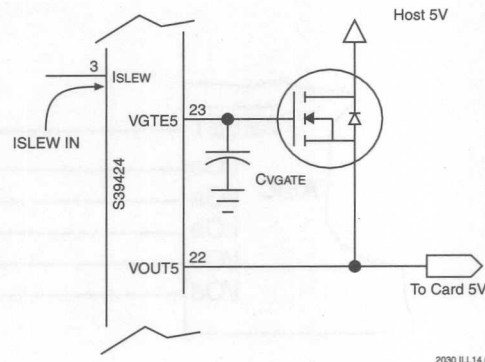
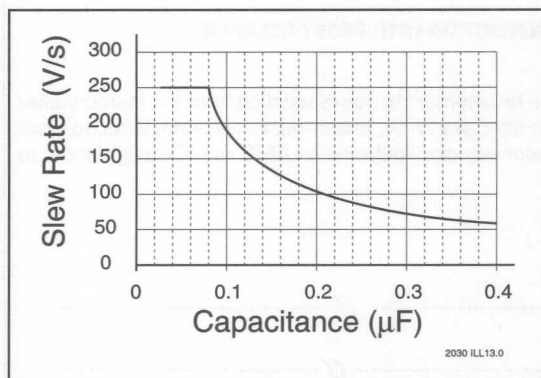
FIGURE 16. DD CIRCUIT 4 TIMING SEQUENCE DIAGRAM



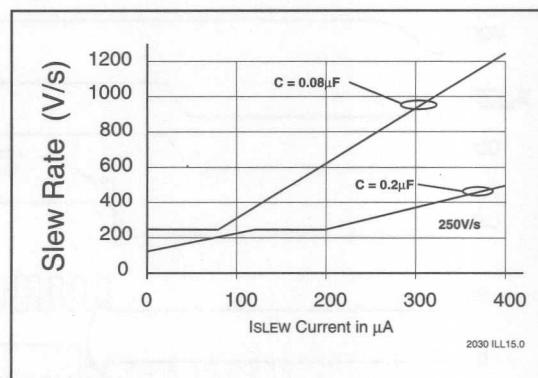
Slew Rate Control

The nominal slew rate for the VGATE3 and VGATE5 outputs is set at a default value of 250V per second, which conforms to a number of standards including that for Compact PCI. This slew rate helps limit current spike transients as the bypass capacitors of the add-in card are charged. The conditions for the default slew rate are: ISLEW input is grounded; and the C_{VGATE} capacitance is less than or equal to $0.08\mu\text{F}$.

The slew rate can be extended (made slower) by adding capacitance to the VGATE outputs. In this case it should be assumed the ISLEW input is grounded. The VGATE outputs can drive up to $20\mu\text{A}$ typically, so the slew rate may be calculated as $20\mu\text{A} \div C_{VGATE}$ (not exceeding 250V/s). Refer to Graph 1 shown below.

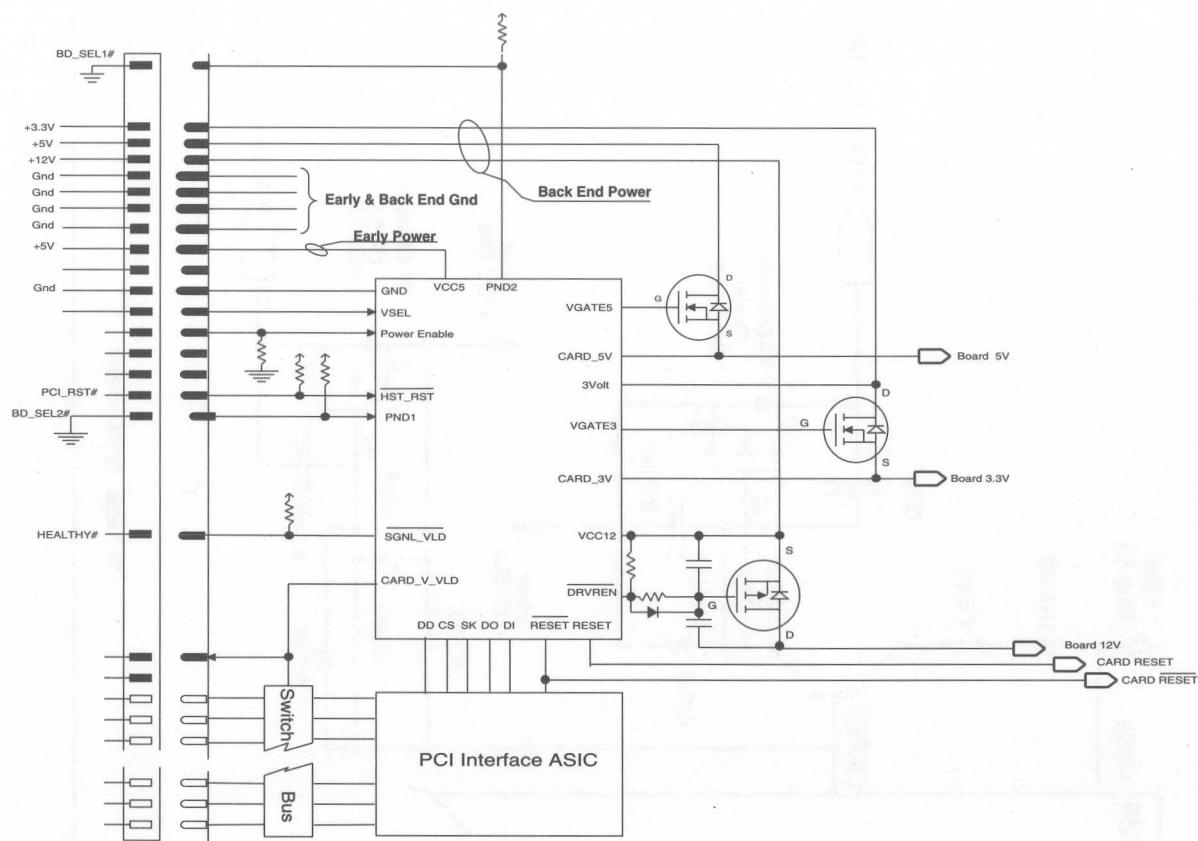


The slew rate can be increased (made faster) by injecting current into the ISLEW input. One quarter of the current injected into ISLEW will be mirrored out of the VGATE drivers. The resulting slew rate may be calculated as $\text{ISLEW} \div 4 \times C_{VGATE}$ (not less than 250V/s). Example slew rates are plotted to illustrate the effects of capacitance on the VGATE output in Graph 2. The reason for the flat portion of the graph is that the internal slew rate control operates in parallel to add as much as $20\mu\text{A}$ (typically) to help keep the SR at 250V/s.



Note that the ISLEW input is simply a diode-connected MOSFET. As a consequence, its I-V characteristic is temperature dependent.

TYPICAL PCI INTERFACE SCHEMATIC



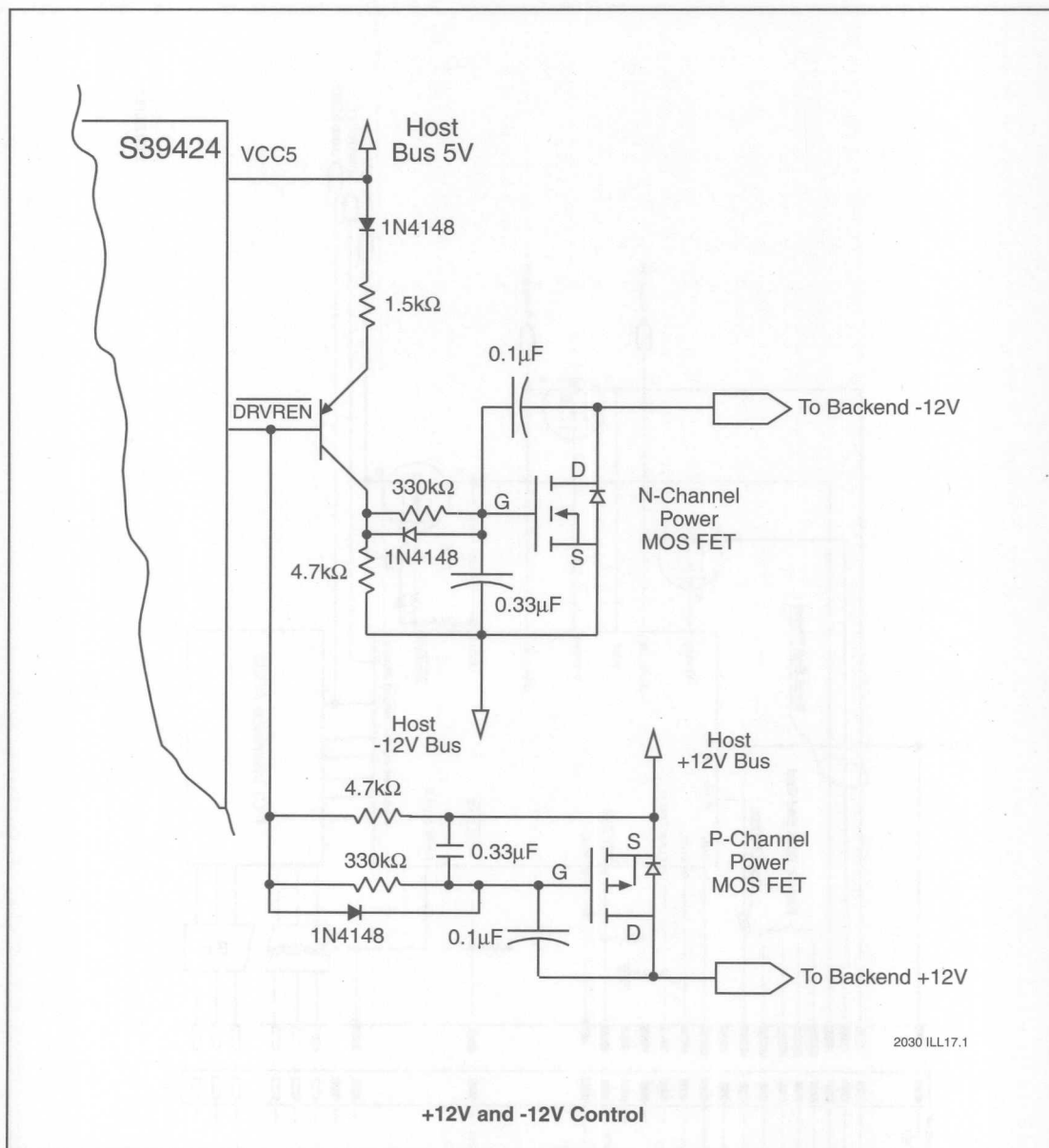
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Applications
Aid

S39424

Preliminary



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SECTION 2 **Precision Reset Controllers With a I²C Nonvolatile Memory**

S24022	Dual Reset I/Os (Active High and Low) and 2K Memory	2-3
S24023	Single Reset I/O (Active Low) and 2K Memory	2-3
S24042	Dual Reset I/Os (Active High and Low) and 4K Memory	2-15
S24043	Single Reset I/O (Active Low) and 4K Memory	2-15
S24162	Single Reset I/O (Active High) and 16K Memory	2-27
S24163	Single Reset I/O (Active Low) and 16K Memory	2-27



SECTION 2

- 2-1 2-1
- 2-2 2-2
- 2-3 2-3
- 2-4 2-4
- 2-5 2-5
- 2-6 2-6
- 2-7 2-7
- 2-8 2-8

**Precision RESET Controller and 2K I²C Memory
With Both RESET and ~~RESET~~ Outputs**

3 and 5 Volt Systems

FEATURES

- **Precision Supply Voltage Monitor**
 - Dual reset outputs for complex microcontroller systems
 - Integrated memory write lockout
- **Guaranteed RESET (RESET) assertion to V_{CC}=1V**
- **Power-Fail Accuracy Guaranteed**
- **No External Components**
- **3 and 5 Volt system versions**
- **Low Power CMOS**
 - Active current less than 3mA
 - Standby current less than 25μA
- **Memory Internally Organized 256 X 8**
 - Two Wire Serial Interface (I²C™)
 - Bidirectional data transfer protocol
 - Standard 100KHz and Fast 400KHz

High Reliability

- Endurance: 1,000,000 erase/write cycles
- Data retention: 100 years

8-Pin PDIP or SOIC Packages

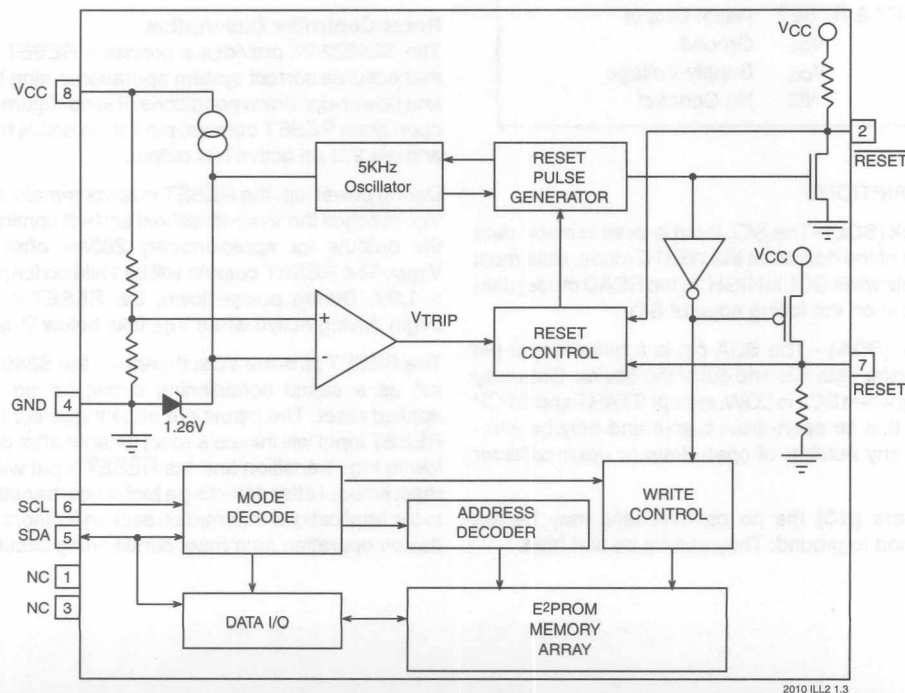
OVERVIEW

The S24022 and S24023 are power supervisory devices with 2,048 bits of serial E²PROM. They are fabricated using SUMMIT's advanced CMOS E²PROM technology and are suitable for both 3 and 5 volt systems.

The memory is internally organized as 256 x 8. It features the I²C serial interface and software protocol allowing operation on a simple two-wire bus.

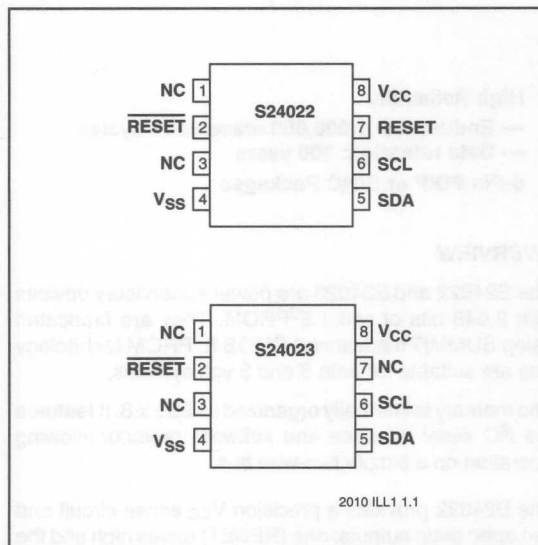
The S24022 provides a precision V_{CC} sense circuit and two open drain outputs: one (RESET) drives high and the other (~~RESET~~) drives low whenever V_{CC} falls below V_{TRIP}. The S24023 is identical to the S24022 with the exception being RESET is not bonded out on pin 7.

BLOCK DIAGRAM





PIN CONFIGURATIONS



PIN NAMES

SDA	Serial Data I/O
SCL	Serial Clock Input
RESET & $\overline{\text{RESET}}$	Reset Output
Vss	Ground
Vcc	Supply Voltage
NC	No Connect

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

No Connects (NC) the no connect pins may be left floating or tied to ground. They cannot be tied high.

RESET - $\overline{\text{RESET}}$ is an active low open drain output. It is driven low whenever V_{CC} is below V_{TRIP} . RESET is also an input and can be used to debounce a switch input or perform signal conditioning. The $\overline{\text{RESET}}$ pin does have an internal pull-up and should be left unconnected if the signal is not used in the system. However, when the pin is tied to a system RESET line an external pull-up resistor should be employed.

RESET - RESET is an active high open drain output. It is driven high whenever V_{CC} is below V_{TRIP} . RESET is also an input and can be used to debounce a switch input or perform signal conditioning. The RESET pin does have an internal pull-down and should be left unconnected if the signal is not used in the system. However, when the pin is tied to a system reset line an external pull-down resistor should be employed.

ENDURANCE AND DATA RETENTION

The S24022/23 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

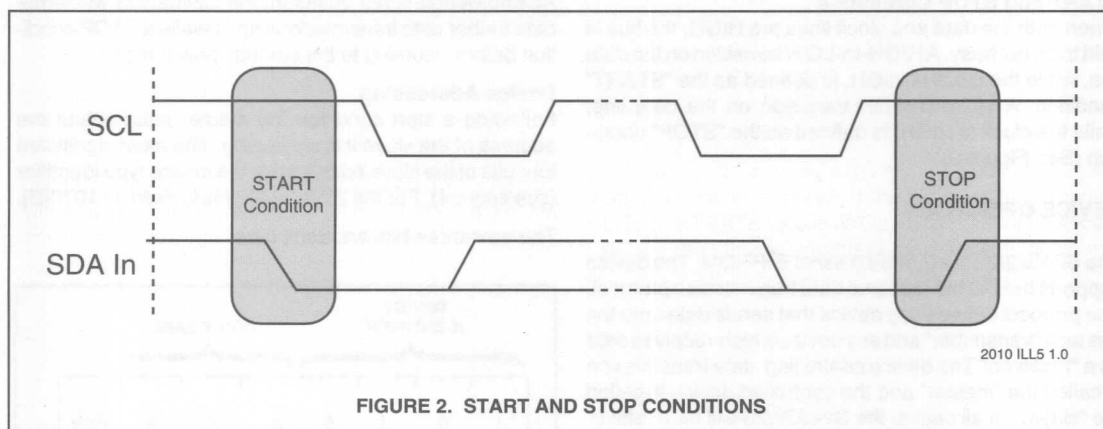
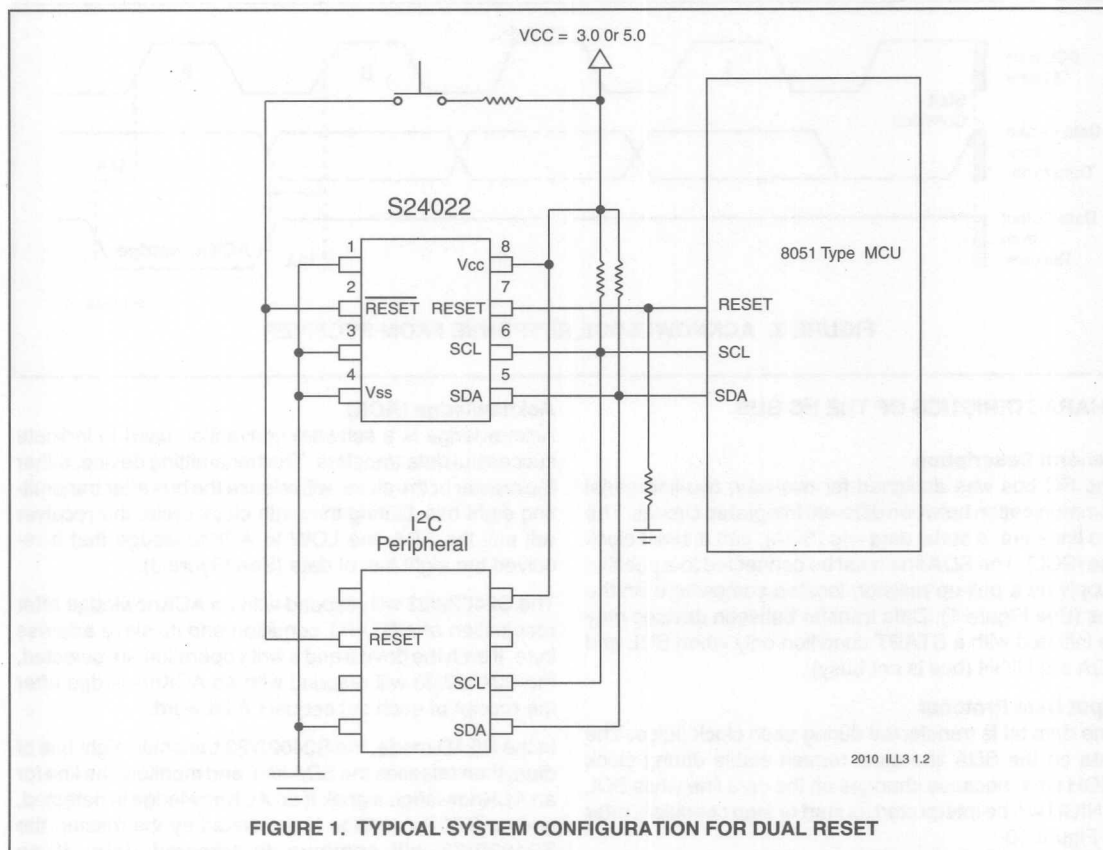
APPLICATIONS

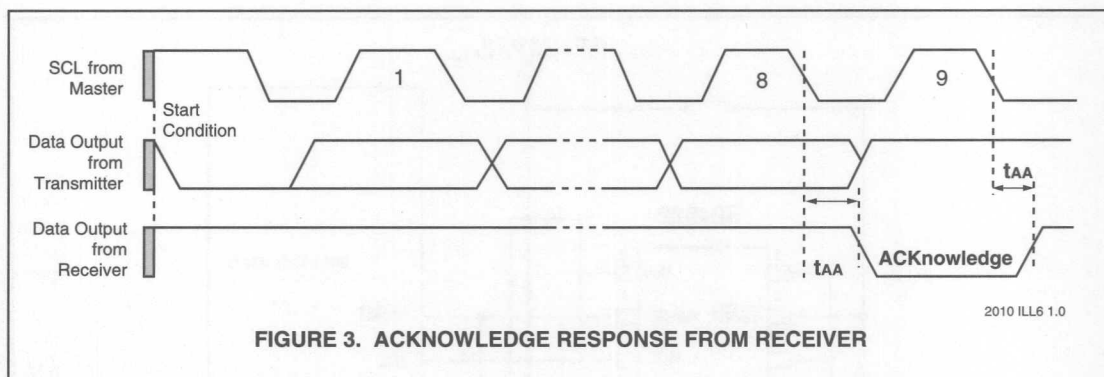
Reset Controller Description

The S24022/23 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output.

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP} . The RESET outputs will be valid so long as V_{CC} is $> 1.0V$. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP} .

The RESET pins are I/Os; therefore, the S24022/23 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a reset conditioning circuit.





CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition, refer to Figure 10.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 2).

DEVICE OPERATION

The S24022/23 is a 2,048-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S24022/23 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 3).

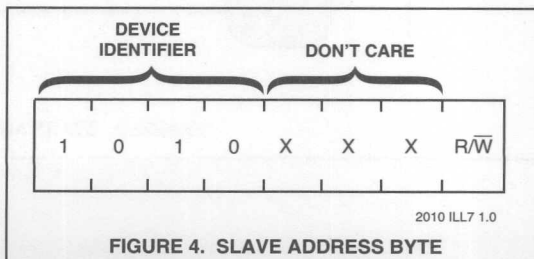
The S24022/23 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S24022/23 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S24022/23 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S24022/23 will continue to transmit data. If an ACKnowledge is not detected, the S24022/23 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 4). For the S24022/23 this is fixed as 1010[B].

The next three bits are don't care.





Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The S24022/23 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

After the slave address is sent (to identify the slave device, and a read or write operation), a second byte is transmitted which contains the 8 bit address of any one of the 256 words in the array.

Upon receipt of the word address, the S24022/23 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S24022/23 begins the internal write cycle.

While the internal write cycle is in progress, the S24022/23 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S24022/23 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more bytes of data. After the receipt of each byte, the S24022/23 will respond with an ACKnowledge.

The S24022/23 automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 5 for the address, ACKnowledge and data transfer sequence.

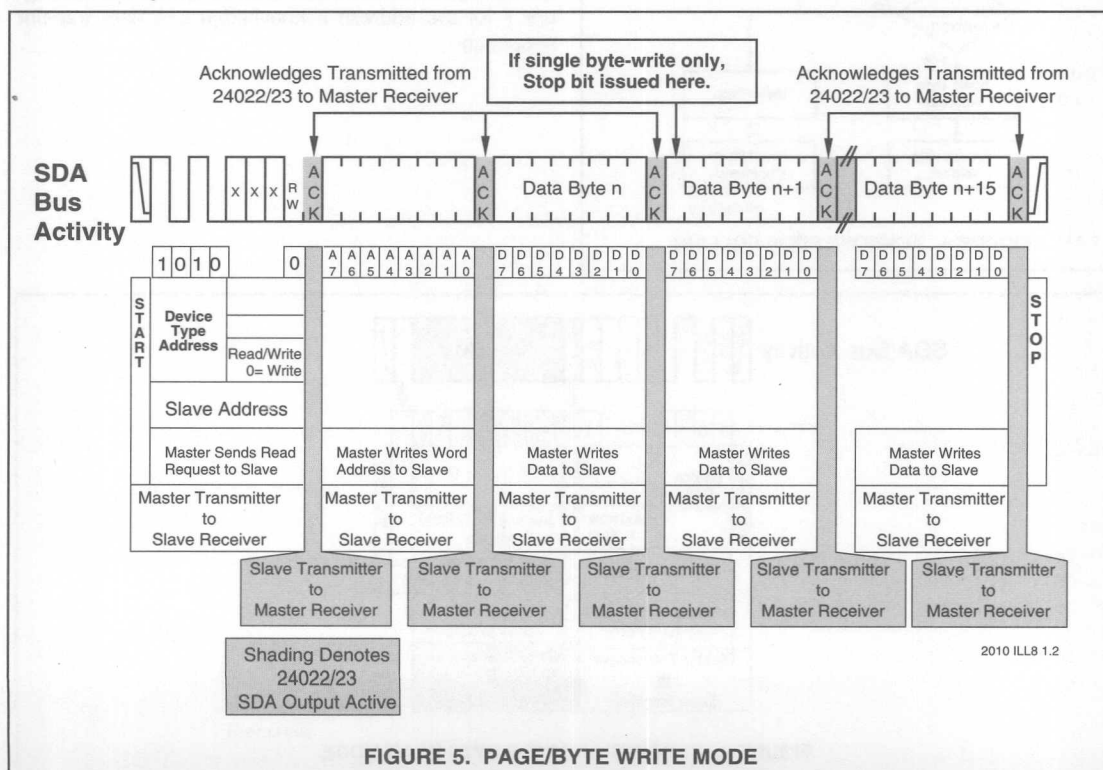
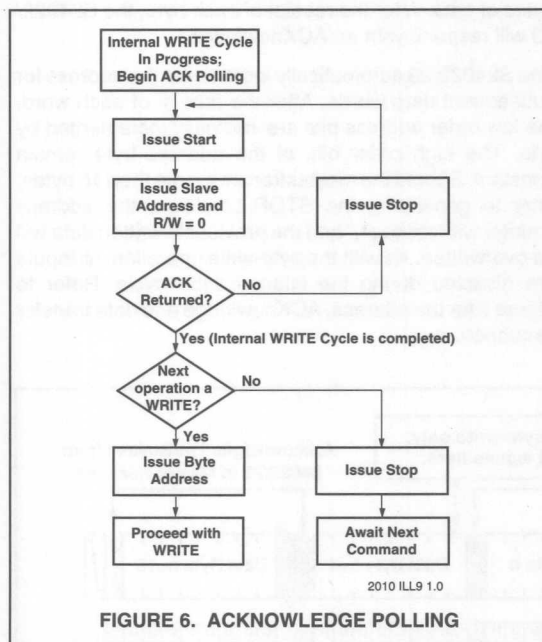


FIGURE 5. PAGE/BYTE WRITE MODE

**Acknowledge Polling**

When the S24022/23 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 6).

**READ OPERATIONS**

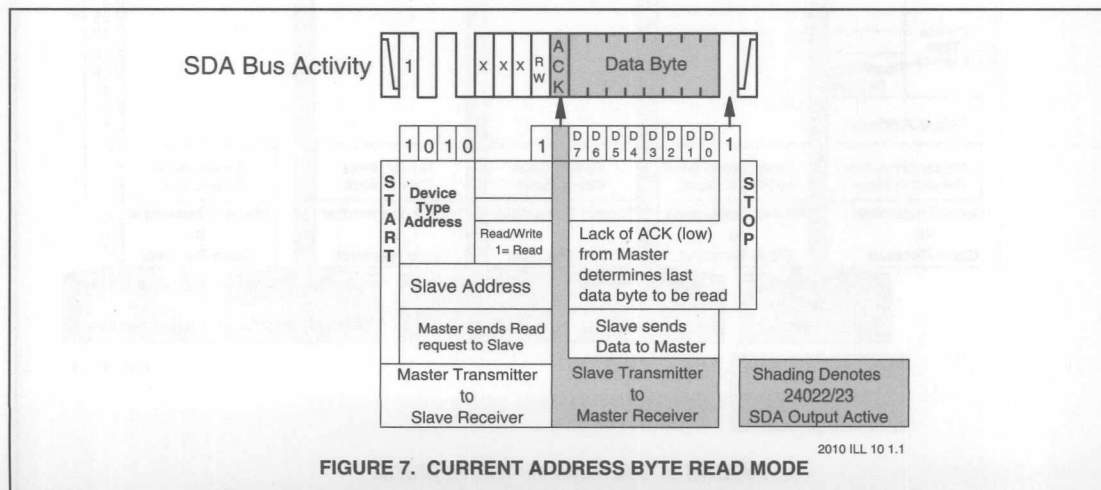
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S24022/23 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the S24022/23 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S24022/23 discontinues data transmission. See Figure 7 for the address acknowledge and data transfer sequence.

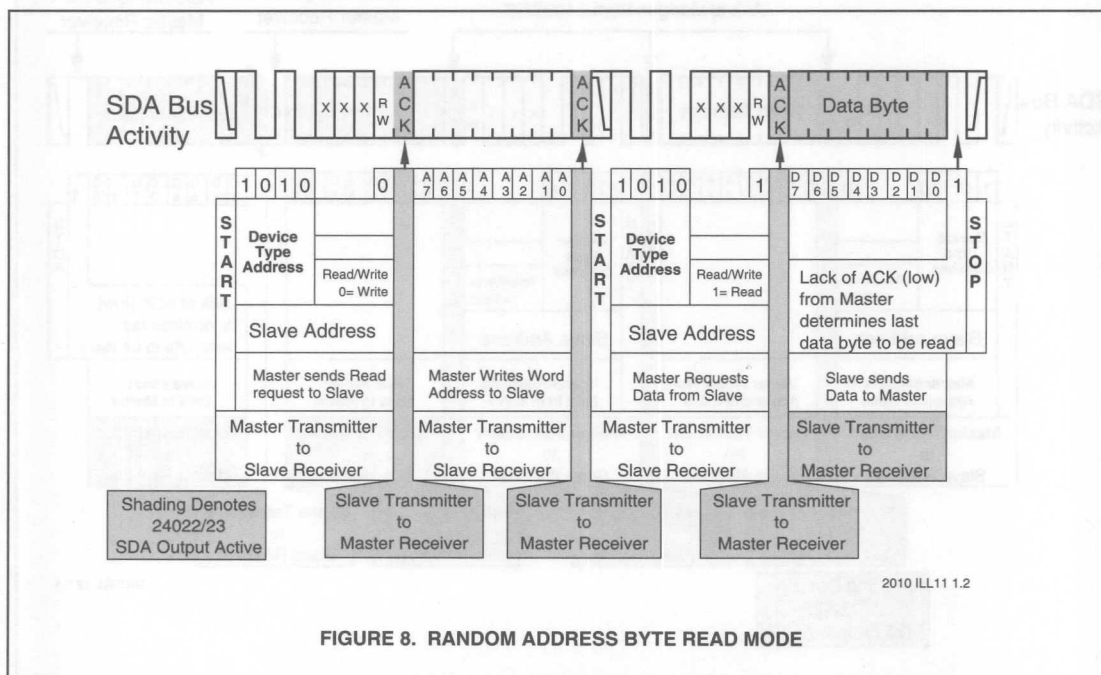




Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S24022/23 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S24022/23 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S24022/23 discontinues data transmission and reverts to its standby power mode. See Figure 8 for the address, acknowledge and data transfer sequence.

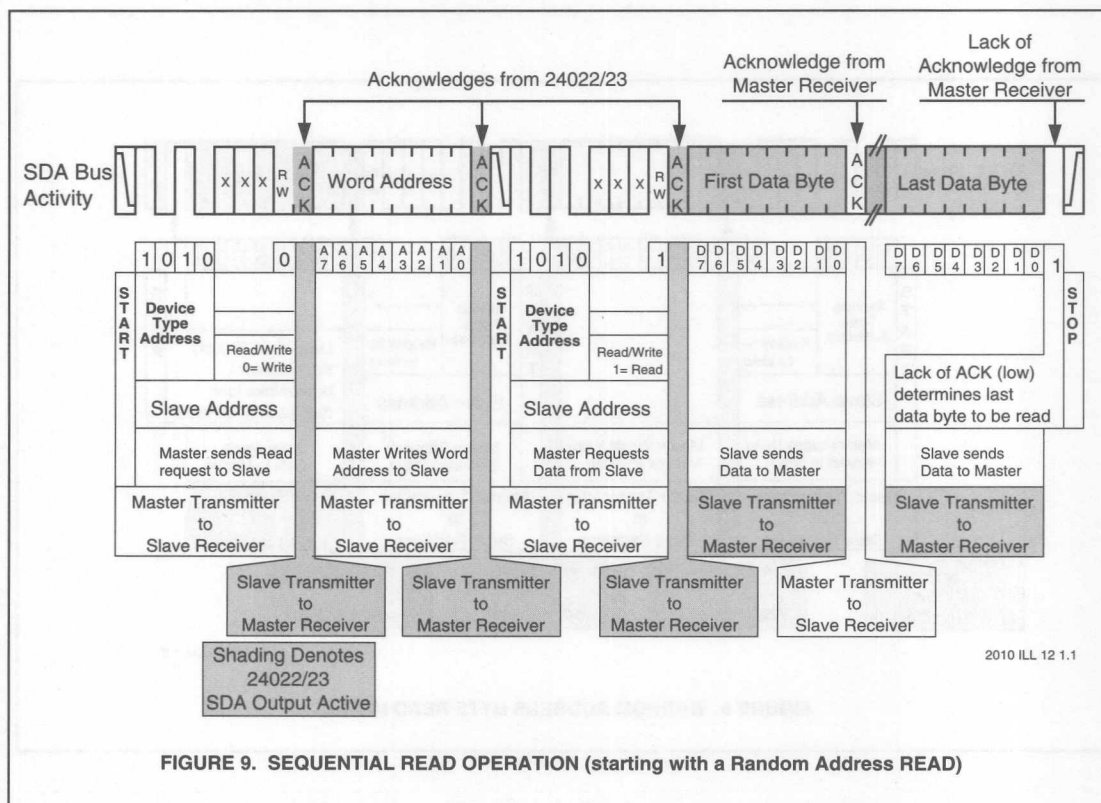




Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S24022/23. The S24022/23 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 9 for the address, acknowledge and data transfer sequence.



**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA	$0.7 \times V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$ SDA		0.4	V

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AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

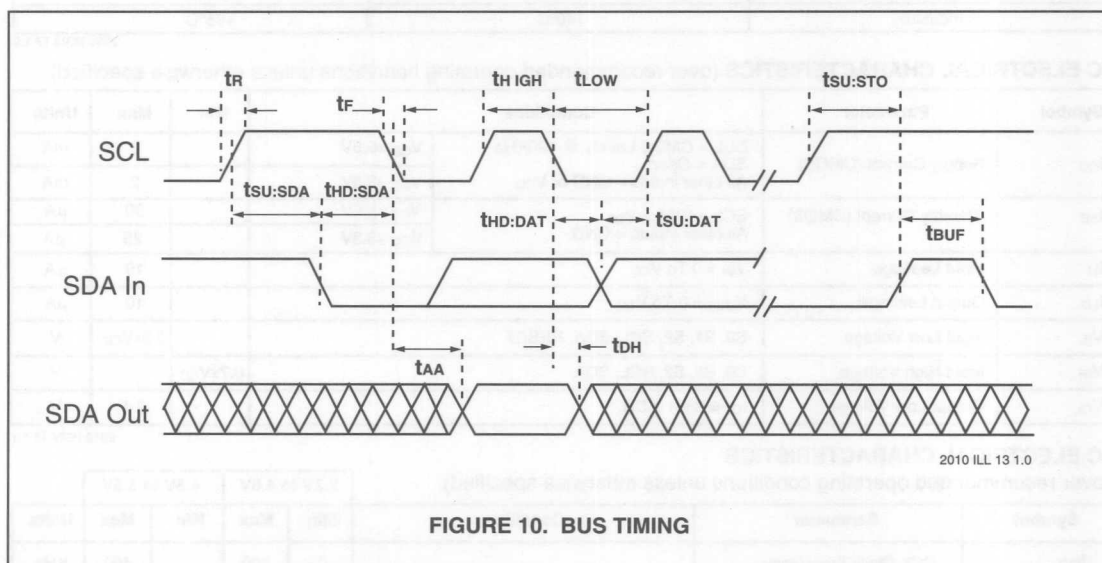
Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

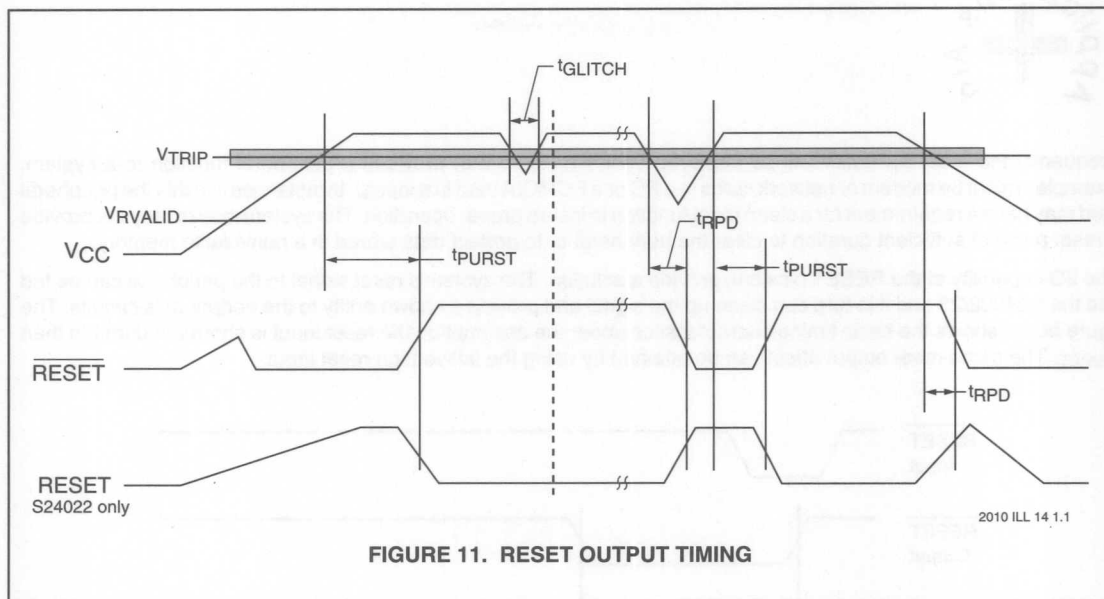
2010 PGM T2 1.0

**CAPACITANCE** $T_A = 25^\circ\text{C}$, $f = 100\text{KHz}$

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

2010 PGM T3 1.0



**RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS** $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

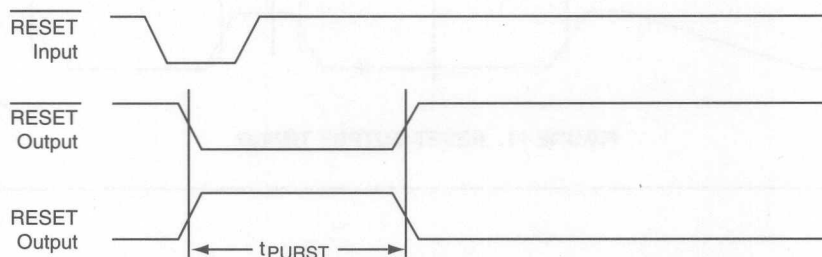
Symbol	Parameter	S24022/23-2.7		S24022/23-A		S24022/23-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
tPURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
tRPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage $I_{OL} = 1\text{mA}$		0.4		0.4		0.4	V
VOHRS	RESET Output High Voltage $I_{OH} = 800\text{ }\mu\text{A}$	$V_{CC} - .75$		$V_{CC} - .75$		$V_{CC} - .75$		V

2010 PGM T6 1.1



Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S24022/23 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



2010 ILL 16 1.0

When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 1.2V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 3.0V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 3.6V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 4.5V, I_{OL}=750\mu A$			0.3	V
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.4	V
		$V_{CC} = 1.2V, I_{OL}=150\mu A$			0.4	V
		$V_{CC} = 3.0V, I_{OL}=750\mu A$			0.4	V
		$V_{CC} = 3.6V, I_{OL}=1mA$			0.4	V
		$V_{CC} = 4.5V, I_{OL}=1mA$			0.4	V
RESET Output Voltage	V_{OH}	$V_{CC} = 1.0V, I_{OH}=400\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 1.2V, I_{OH}=800\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 3.0V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 3.6V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 4.5V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V

2010 PGM T5 1.0

**Precision RESET Controller and 4K I²C Memory
With Both RESET and RESET Outputs**

3 and 5 Volt Systems

FEATURES

- Precision Supply Voltage Monitor
 - Dual reset outputs for complex microcontroller systems
 - Integrated memory write lockout
- Guaranteed RESET (RESET) assertion to $V_{CC}=1V$
- Power-Fail Accuracy Guaranteed
- No External Components
- 3 and 5 Volt system versions
- Low Power CMOS
 - Active current less than 3mA
 - Standby current less than 25 μ A
- Memory Internally Organized 512 X 8
 - Two Wire Serial Interface (I²C™)
 - Bidirectional data transfer protocol
 - Standard 100KHz and Fast 400KHz

- High Reliability
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: 100 years
- 8-Pin PDIP or SOIC Packages

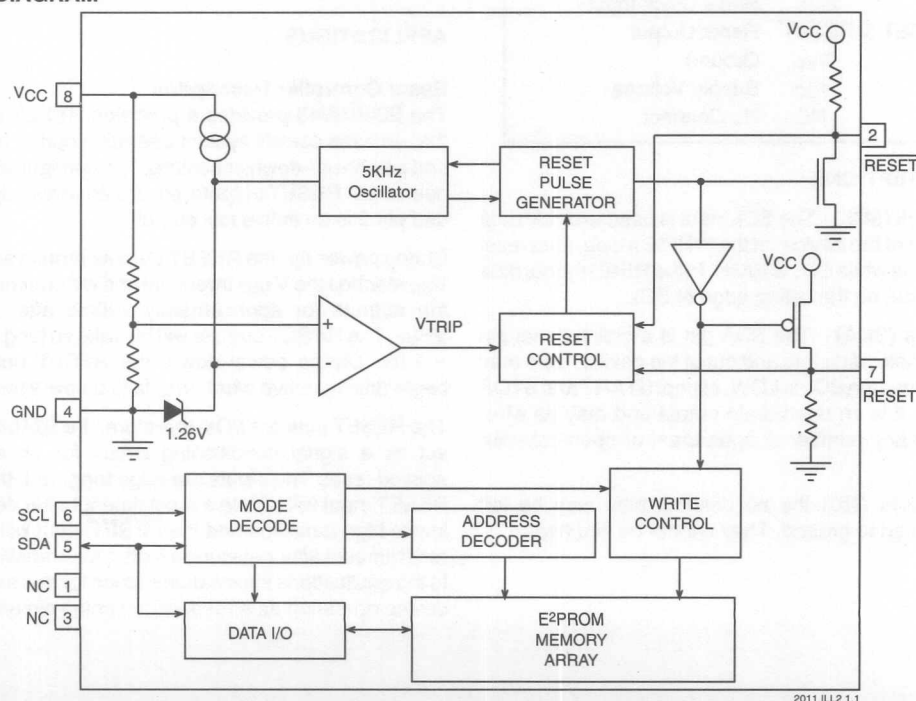
OVERVIEW

The S24042 and S24043 are power supervisory devices with 4,096 bits of serial E²PROM. They are fabricated using SUMMIT's advanced CMOS E²PROM technology and are suitable for both 3 and 5 volt systems.

The memory is internally organized as 512 x 8. It features the I²C serial interface and software protocol allowing operation on a simple two-wire bus.

The S24042 provides a precision V_{CC} sense circuit and two open drain outputs: one (RESET) drives high and the other (RESET) drives low whenever V_{CC} falls below V_{TRIP} . The S24043 is identical to the S24042 with the exception being RESET is not bonded out on pin 7.

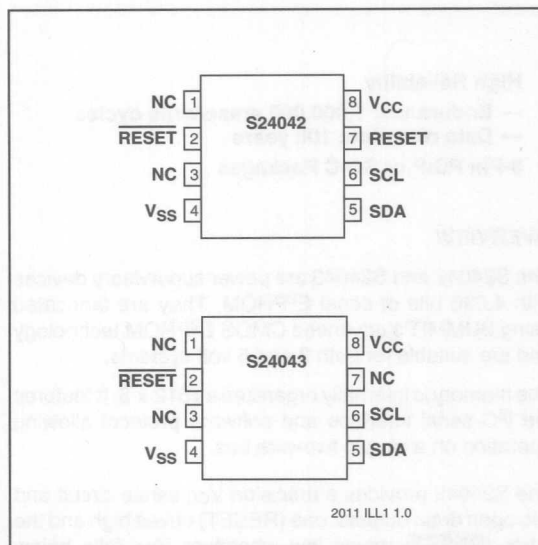
BLOCK DIAGRAM



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PIN CONFIGURATIONS



PIN NAMES

SDA	Serial Data I/O
SCL	Serial Clock Input
RESET & $\overline{\text{RESET}}$	Reset Output
Vss	Ground
Vcc	Supply Voltage
NC	No Connect

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

No Connects (NC) the no connect pins may be left floating or tied to ground. They cannot be tied high.

RESET - $\overline{\text{RESET}}$ is an active low open drain output. It is driven low whenever V_{CC} is below V_{TRIP} . $\overline{\text{RESET}}$ is also an input and can be used to debounce a switch input or perform signal conditioning. The $\overline{\text{RESET}}$ pin does have an internal pull-up and should be left unconnected if the signal is not used in the system. However, when the pin is tied to a system $\overline{\text{RESET}}$ line an external pull-up resistor should be employed.

RESET - RESET is an active high open drain output. It is driven high whenever V_{CC} is below V_{TRIP} . RESET is also an input and can be used to debounce a switch input or perform signal conditioning. The RESET pin does have an internal pull-down and should be left unconnected if the signal is not used in the system. However, when the pin is tied to a system reset line an external pull-down resistor should be employed.

ENDURANCE AND DATA RETENTION

The S24042/43 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

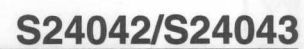
APPLICATIONS

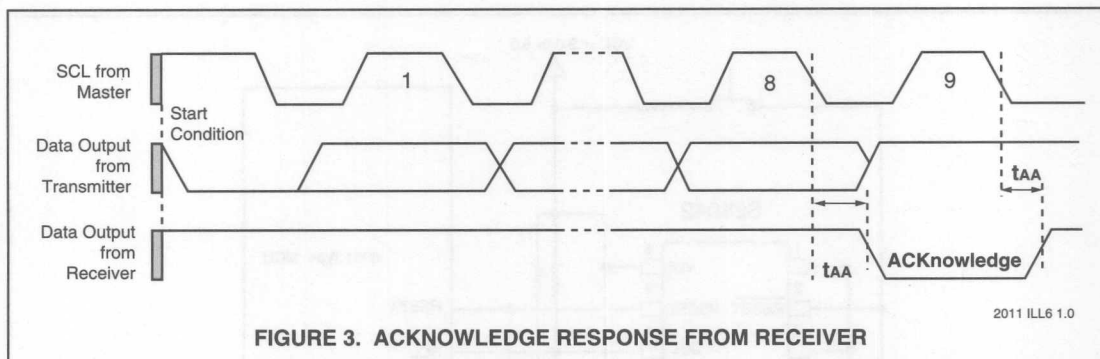
Reset Controller Description

The S24042/43 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output.

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP} . The RESET outputs will be valid so long as V_{CC} is $> 1.0V$. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP} .

The RESET pins are I/Os; therefore, the S24042/43 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a low to high transition and the RESET input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a reset conditioning circuit.





CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition, refer to Figure 10.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 2).

DEVICE OPERATION

The S24042/43 is a 4,096-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S24042/43 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 3).

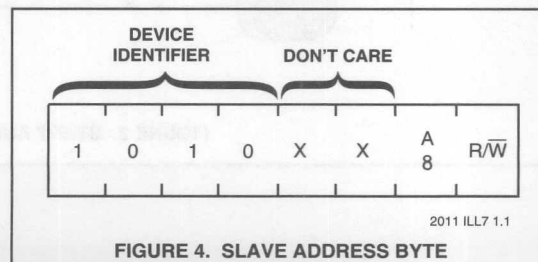
The S24042/43 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S24042/43 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S24042/43 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S24042/43 will continue to transmit data. If an ACKnowledge is not detected, the S24042/43 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 4). For the S24042/43 this is fixed as 1010[B].

The next two bits are don't care. The next bit is the high order address bit A₈.





Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The S24042/43 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

Upon receipt of the slave address and word address, the S24042/43 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S24042/43 begins the internal write cycle.

While the internal write cycle is in progress, the S24042/43 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S24042/43 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more bytes of data. After the receipt of each byte, the S24042/43 will respond with an ACKnowledge.

The S24042/43 automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 5 for the address, ACKnowledge and data transfer sequence.

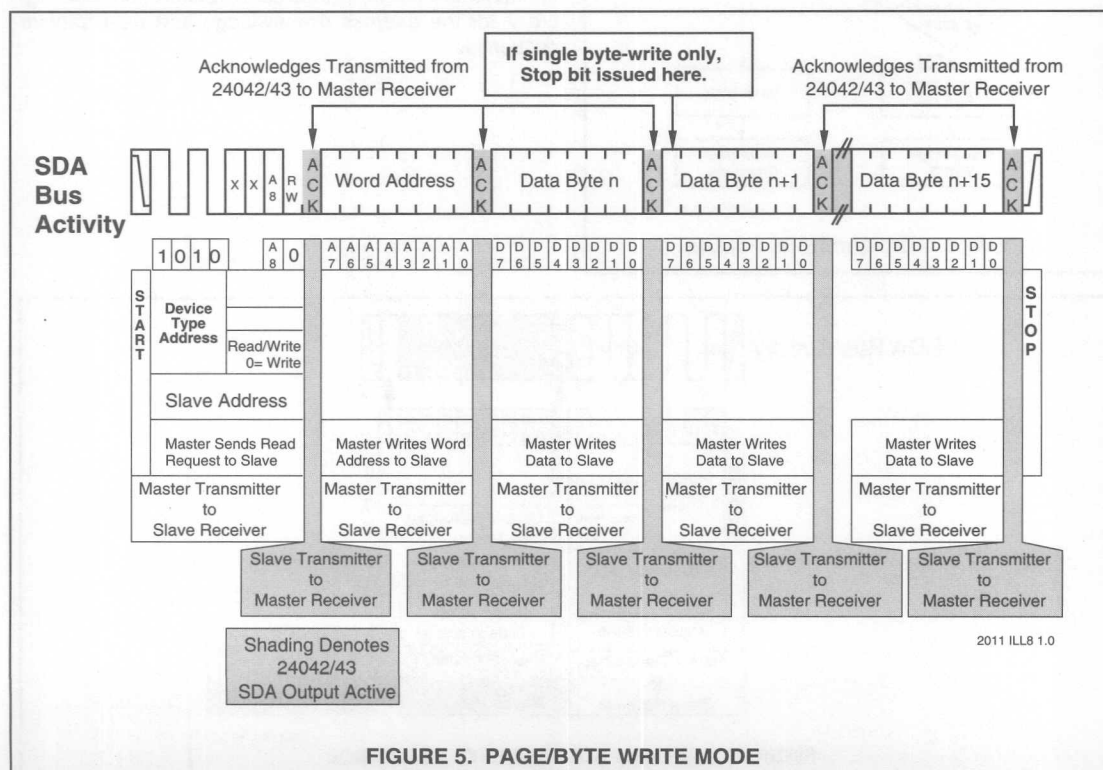


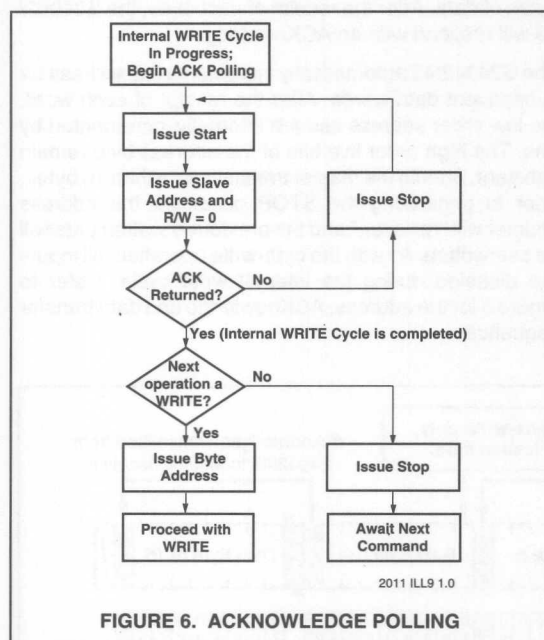
FIGURE 5. PAGE/BYTE WRITE MODE



Acknowledge Polling

When the S24042/43 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 6).



READ OPERATIONS

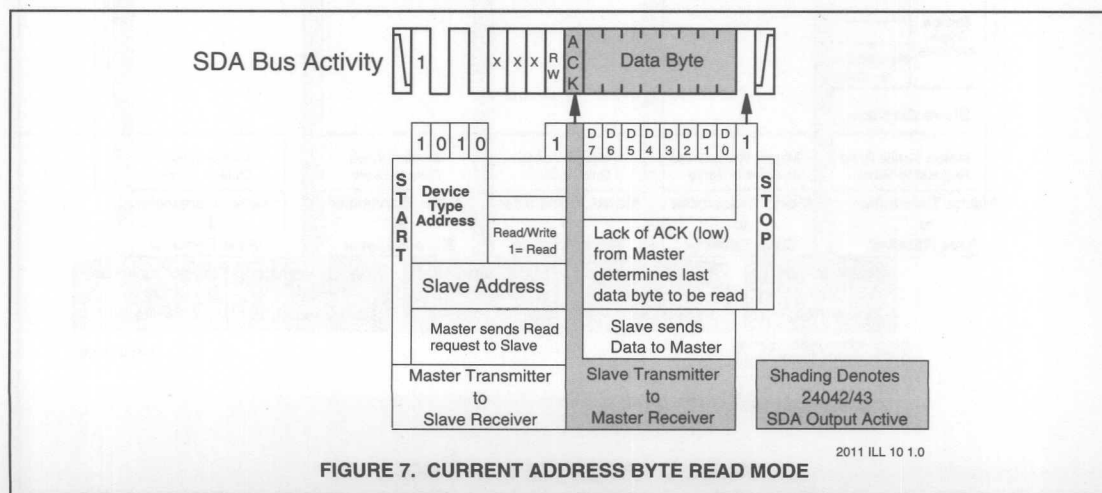
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S24042/43 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n , the next read operation would access data from address location $n+1$ and increment the current address pointer. When the S24042/43 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location $n+1$.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S24042/43 discontinues data transmission. See Figure 7 for the address acknowledge and data transfer sequence.

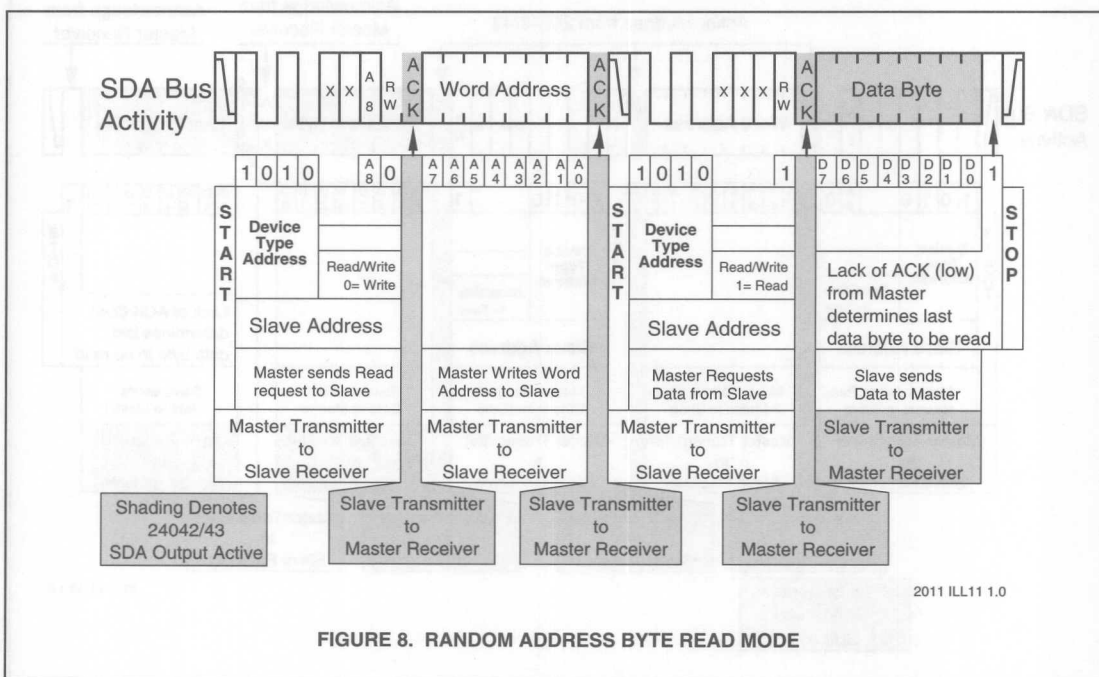




Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S24042/43 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S24042/43 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S24042/43 discontinues data transmission and reverts to its standby power mode. See Figure 8 for the address, acknowledge and data transfer sequence.





Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S24042/43. The S24042/43 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 9 for the address, acknowledge and data transfer sequence.

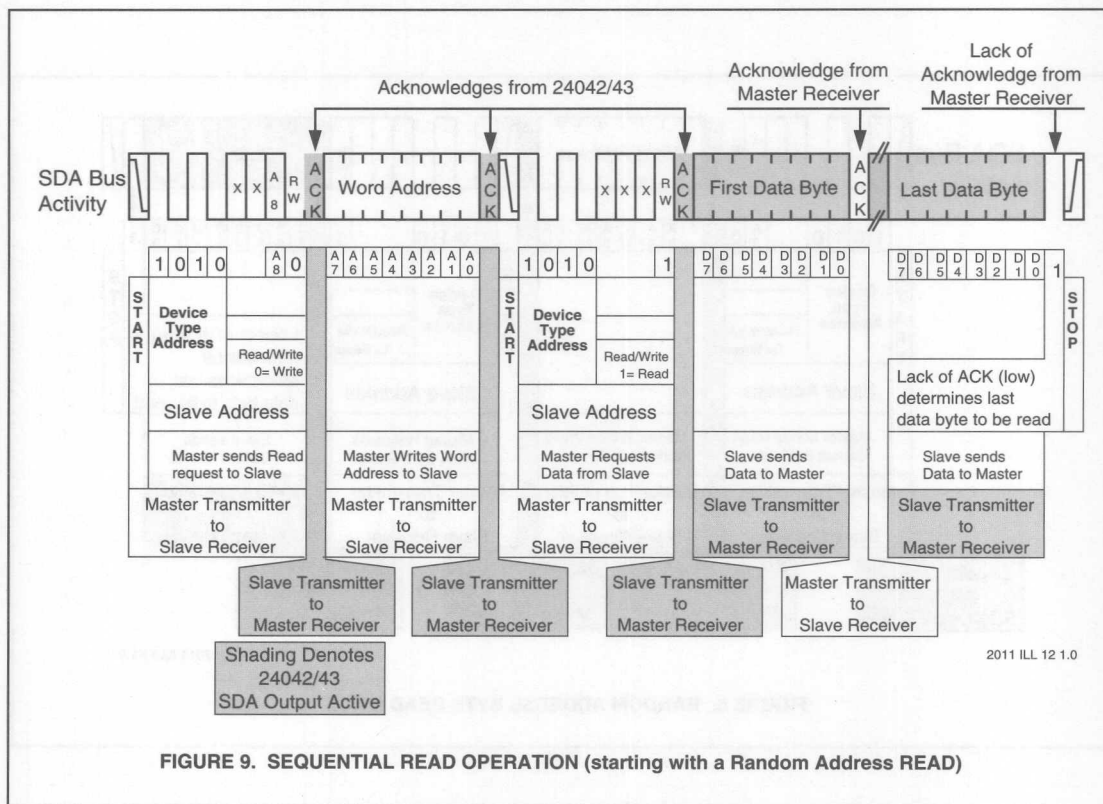


FIGURE 9. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SS}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA	$0.7 \times V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$ SDA		0.4	V

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AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

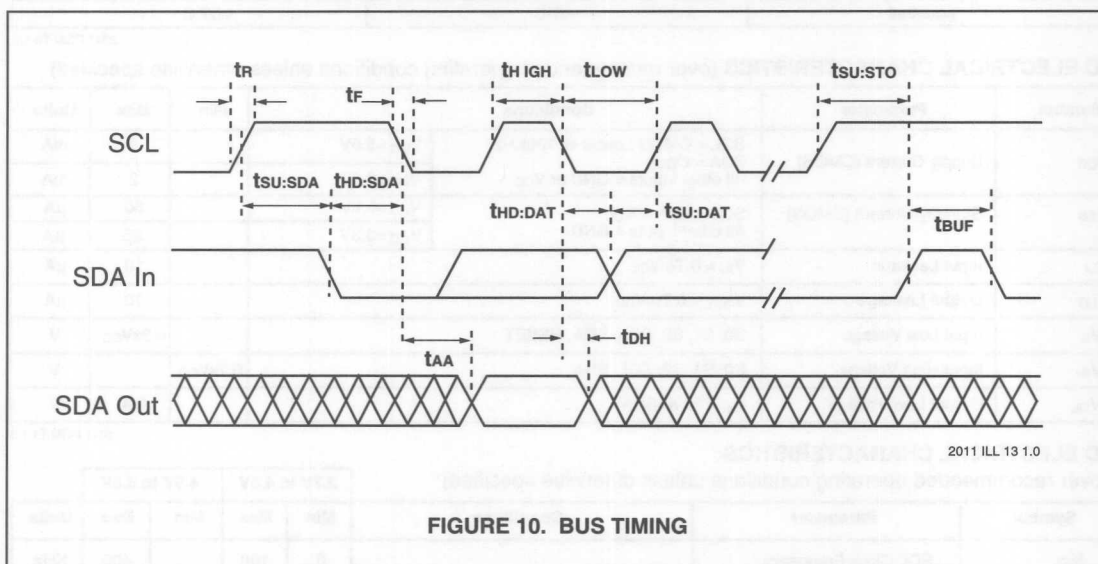
Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

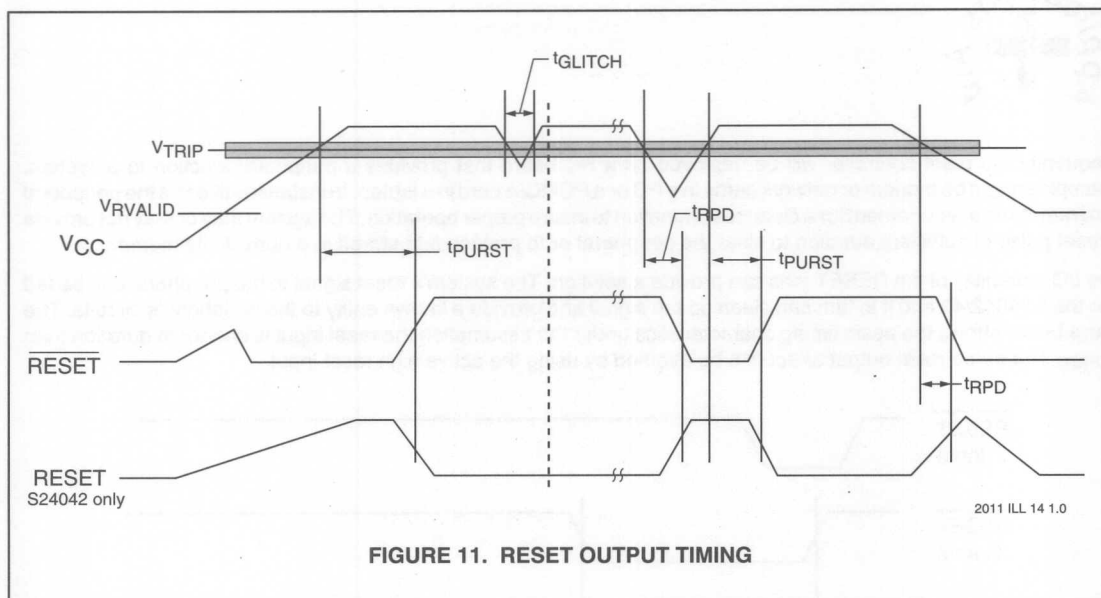
2011 PGM T2 1.0

**CAPACITANCE** $T_A = 25^\circ\text{C}$, $f = 100\text{KHz}$

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

2011 PGM T3 1.0



**RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS**

TA = -40°C to +85°C

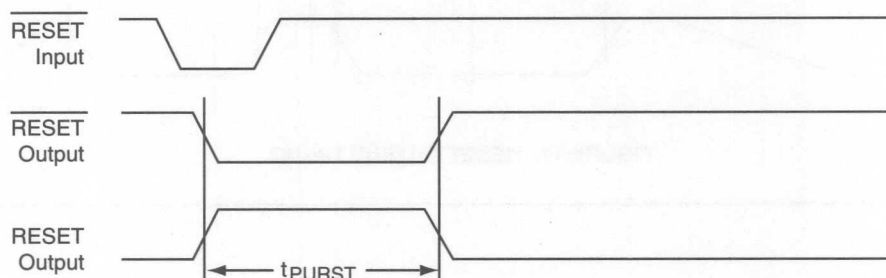
Symbol	Parameter	S24042/43-2.7		S24042/43-A		S24042/43-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
tpURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
trPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage IO _L = 1mA		0.4		0.4		0.4	V
VOHRS	RESET Output High Voltage IO _H = 800 μA	VCC-75		VCC-75		VCC-75		V

2011 PGM T6 1.1



Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S24042/43 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



2011 ILL 16 1.0

When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 1.2V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 3.0V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 3.6V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 4.5V, I_{OL}=750\mu A$			0.3	V
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.4	V
		$V_{CC} = 1.2V, I_{OL}=150\mu A$			0.4	V
		$V_{CC} = 3.0V, I_{OL}=750\mu A$			0.4	V
		$V_{CC} = 3.6V, I_{OL}=1mA$			0.4	V
		$V_{CC} = 4.5V, I_{OL}=1mA$			0.4	V
RESET Output Voltage	V_{OH}	$V_{CC} = 1.0V, I_{OH}=400\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 1.2V, I_{OH}=800\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 3.0V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 3.6V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 4.5V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V

2011 PGM T5 1.0

FEATURES

- **Precision Supply Voltage Monitor**
 - 162 Active High
 - 163 Active Low
 - Integrated memory write lockout
- **Guaranteed RESET ($\overline{\text{RESET}}$) assertion to $V_{CC}=1V$**
- **Power-Fail Accuracy Guaranteed**
- **No External Components**
- **3 and 5 Volt system versions**
- **Low Power CMOS**
 - Active current less than 3mA
 - Standby current less than 25 μ A
- **Memory Internally Organized 2k X 8**
 - Two Wire Serial Interface (I²C™)
 - Bidirectional data transfer protocol
 - Standard 100KHz and Fast 400KHz

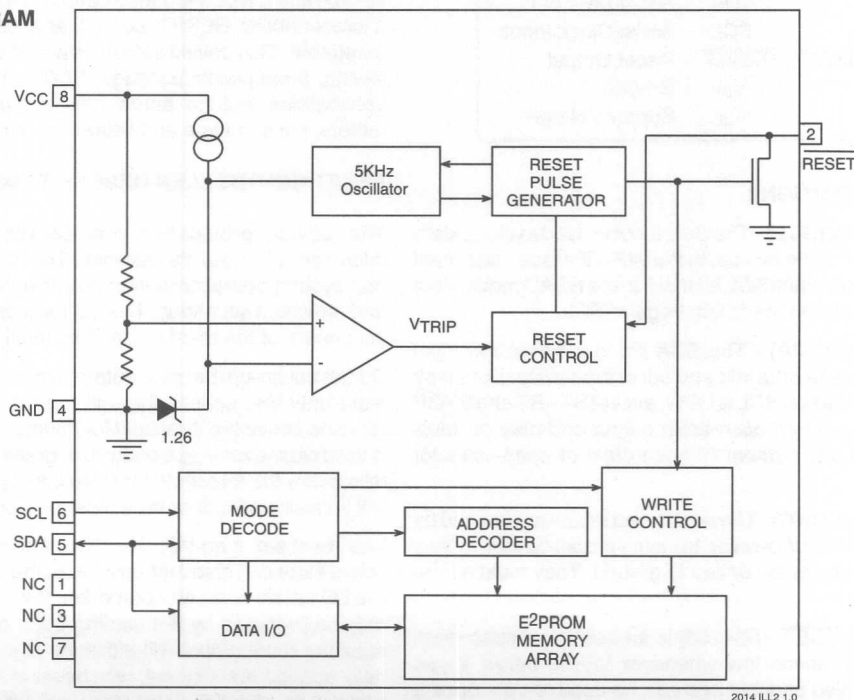
High Reliability

- Endurance: 1,000,000 erase/write cycles
- Data retention: 100 years

8-Pin PDIP or SOIC Packages
OVERVIEW

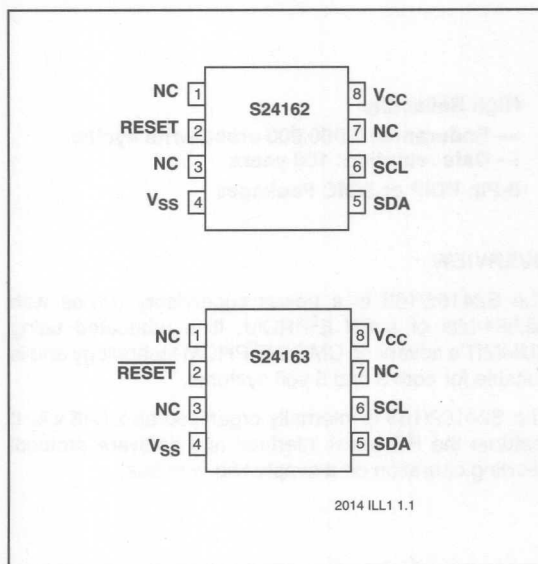
The S24162/163 is a power supervisory device with 16,384-bits of serial E²PROM. It is fabricated using SUMMIT's advanced CMOS E²PROM technology and is suitable for both 3 and 5 volt systems.

The S24162/163 is internally organized as 2,048 x 8. It features the I²C serial interface and software protocol allowing operation on a simple two-wire bus.

BLOCK DIAGRAM




PIN CONFIGURATIONS



PIN NAMES

NC	No Connect
SDA	Serial Data I/O
SCL	Serial Clock Input
(RESET) RESET	Reset Output
VSS	Ground
VCC	Supply Voltage

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

No Connects (NC) - The no connect inputs are unused by the S24162/163; however, to insure proper operation they can be unconnected or tied to ground. They must not be tied to VCC.

RESET - RESET (S24163) is an active low open drain output. It is driven low whenever VCC is below VTRIP. RESET is also an input and can be used to debounce a

switch input or perform signal conditioning. The RESET pin does have an internal pull-up and should be left unconnected if the signal is not used in the system. However, when the pin is tied to a system RESET line an external pull-up resistor should be employed.

RESET - RESET (S24162) is an active high open drain output. It is driven high whenever VCC is below VTRIP. RESET is also an input and can be used to debounce a switch input or perform signal conditioning. The RESET pin does have an internal pull-down and should be left unconnected if the signal is not used in the system. However, when the pin is tied to a system reset line an external pull-down resistor should be employed.

ENDURANCE AND DATA RETENTION

The S24162/163 is designed for applications requiring up to 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

APPLICATIONS

The S24162/163 is ideal for applications requiring low voltage and low power consumption. This device provides microcontroller RESET control and can be manually resettable. This device also uses a cost effective, space-saving, 8-pin plastic package, SOIC and PDIP. Typical applications include alarm devices, electronic locks, meters, keys, pagers and cellular phones.

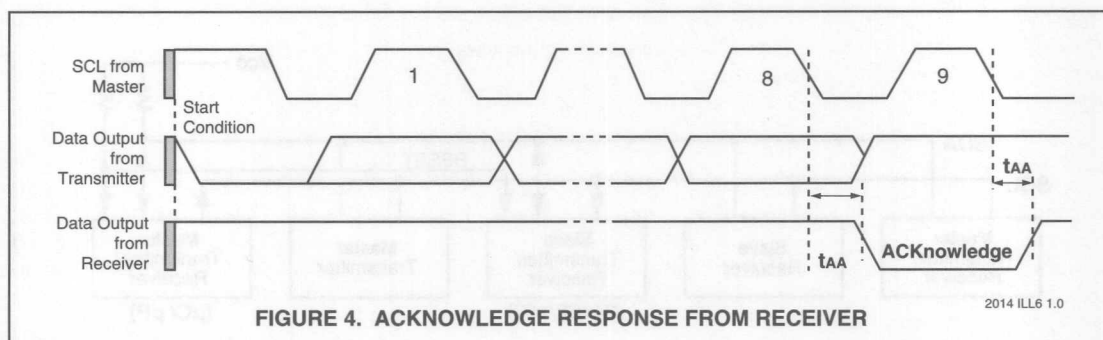
RESET CONTROLLER DESCRIPTION

The device provides a precise reset output to a microcontroller and it's associated circuitry ensuring correct system operation during power-up/down conditions and brownout situations. The output is open drain, allowing control of the reset function by multiple devices.

During power-up the reset output remains in a fixed active state until VCC passes through the reset threshold and remains above the threshold for 200ms. The reset output is valid whenever VCC is equal to or greater than 1V. If VCC falls below the threshold for more than tGLITCH the device will immediately generate a reset and drive the output.

The reset pin is an I/O; therefore, forcing the pin to the active state can also manually reset the device. Because the I/O needs to be an open drain, the internal timer can only be triggered by the leading edge of the input. The resulting reset output will either be tPURST, or the externally applied reset signal, whichever is longer. This can provide an affective debounce or reset signal extender solution.





CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition (See Figure 2).

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 3).

DEVICE OPERATION

The S24162/163 is a 16,384-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S24162/163 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either

the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to Acknowledge that it received the eight bits of data (See Figure 4).

The S24162/163 will respond with an Acknowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S24162/163 will respond with an Acknowledge after the receipt of each subsequent 8-bit word.

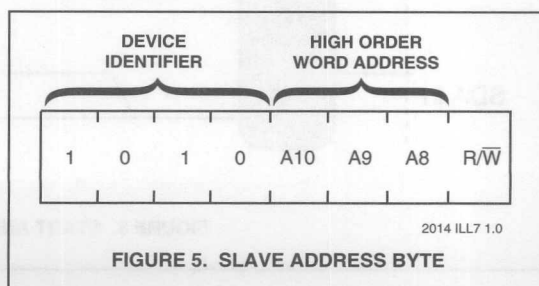
In the READ mode, the S24162/163 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no STOP condition is generated by the master, the S24162/163 will continue to transmit data. If an Acknowledge is not detected, the S24162/163 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 5). For the S24162/163 this is fixed as 1010[B].

Word Address

The next three bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the 2,048 X 8 array.





Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The S24162/163 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 2,048 words in the array.

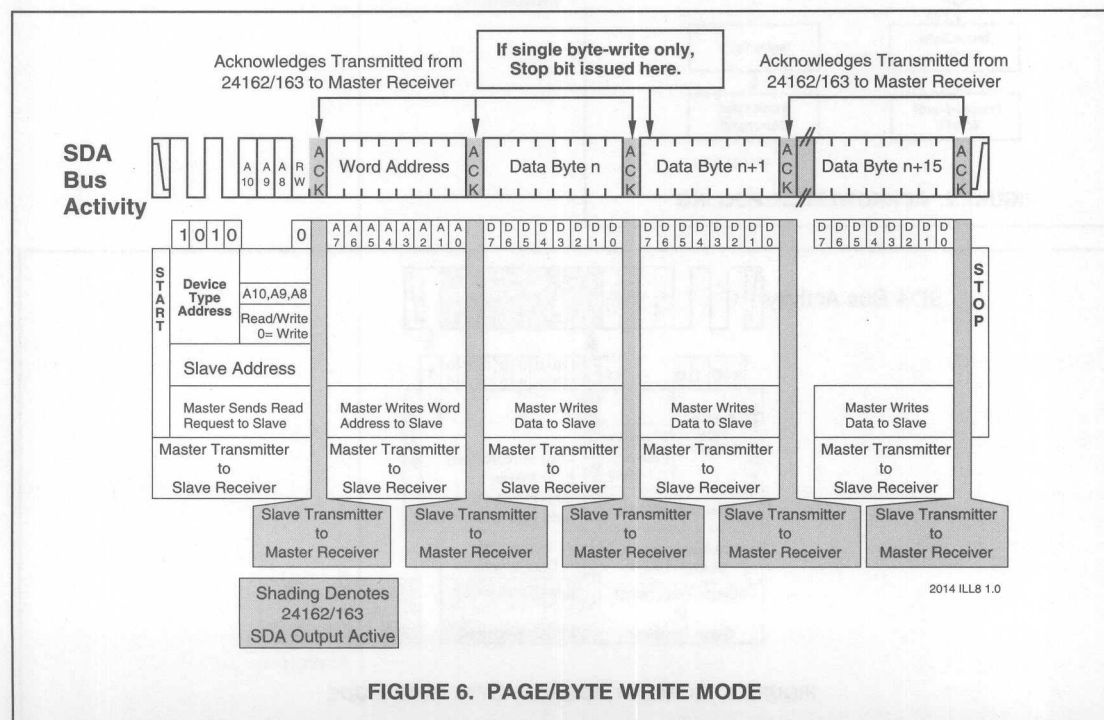
Upon receipt of the word address, the S24162/163 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S24162/163 begins the internal write cycle.

While the internal write cycle is in progress, the S24162/163 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S24162/163 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S24162/163 will respond with an ACKnowledge.

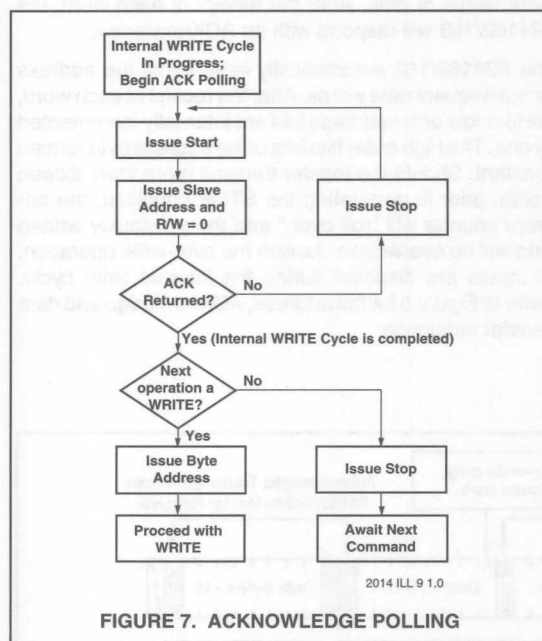
The S24162/163 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.



**Acknowledge Polling**

When the S24162/163 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).

**READ OPERATIONS**

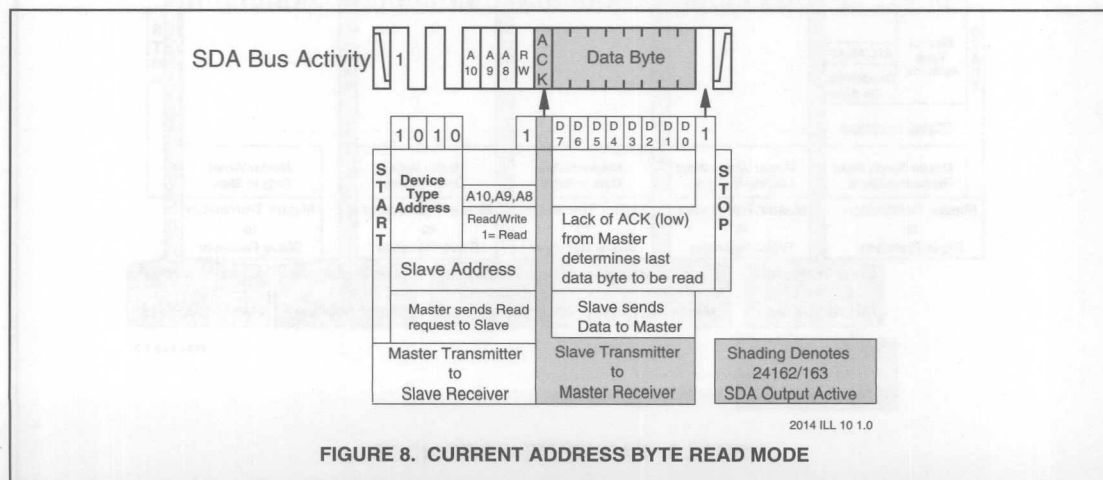
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S24162/163 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n , the next read operation would access data from address location $n+1$ and increment the current address pointer. When the S24162/163 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location $n+1$.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S24162/163 discontinues data transmission. See Figure 8 for the address acknowledge and data transfer sequence.





Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S24162/163 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S24162/163 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S24162/163 discontinues data transmission and reverts to its standby power mode. See Figure 9 for the address, acknowledge and data transfer sequence.

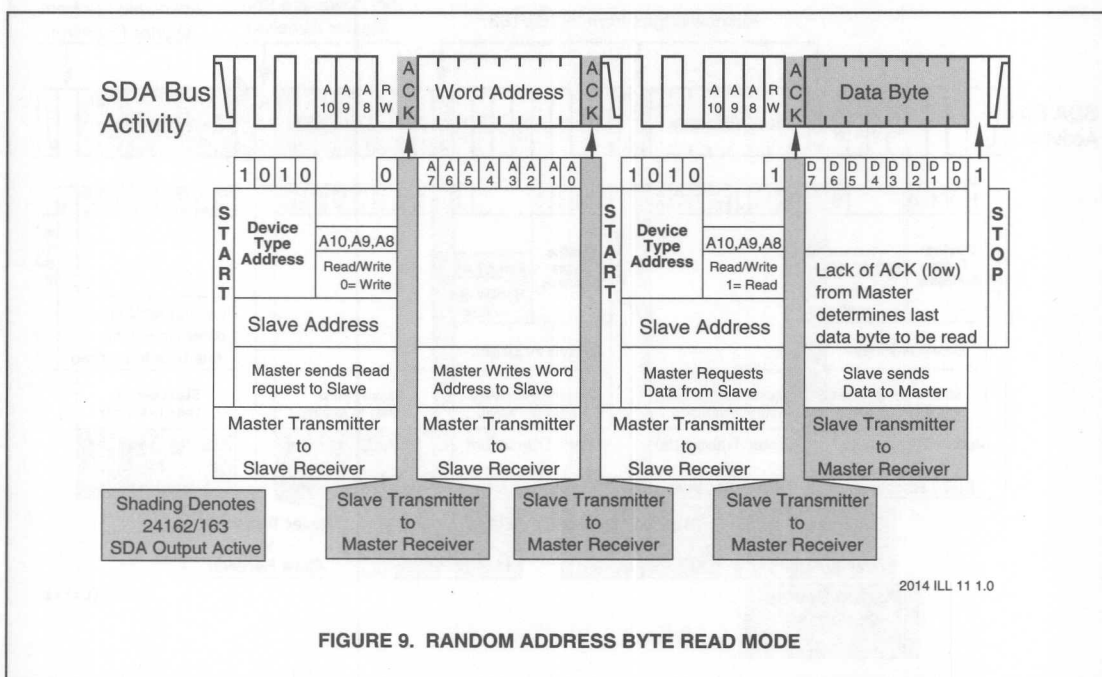


FIGURE 9. RANDOM ADDRESS BYTE READ MODE



Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S24162/163. The S24162/163 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 10 for the address, acknowledge and data transfer sequence.

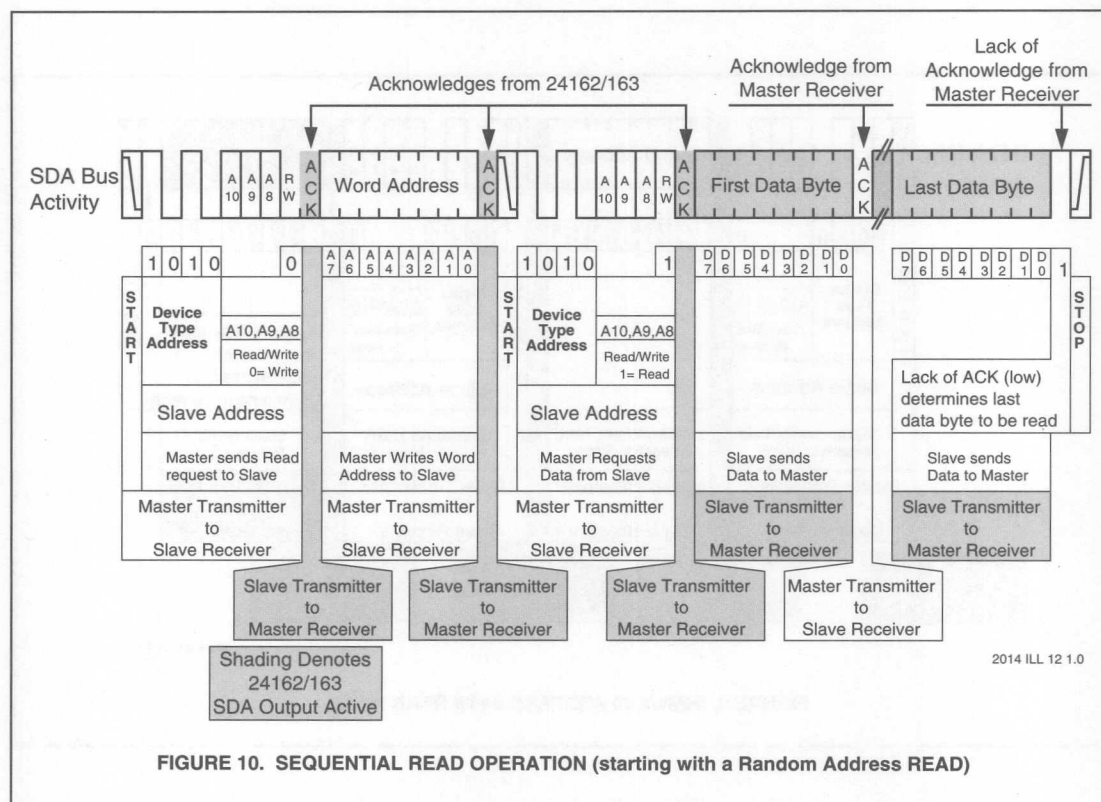


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

S24162/163, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$

S24162/163-3, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7V$ to $5.5V$

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA	$0.7 \times V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$		0.4	V

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AC ELECTRICAL CHARACTERISTICS

S24162/163, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$

S24162/163-3, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7V$ to $5.5V$

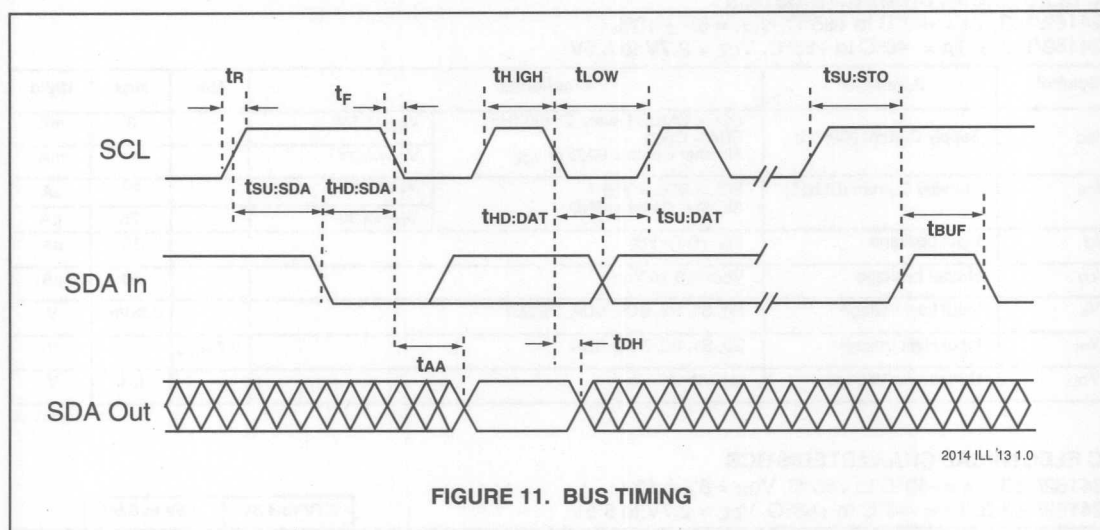
Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

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**CAPACITANCE** $T_A = 25^{\circ}\text{C}$, $f = 100\text{kHz}$

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

2014 PGM T3 1.0

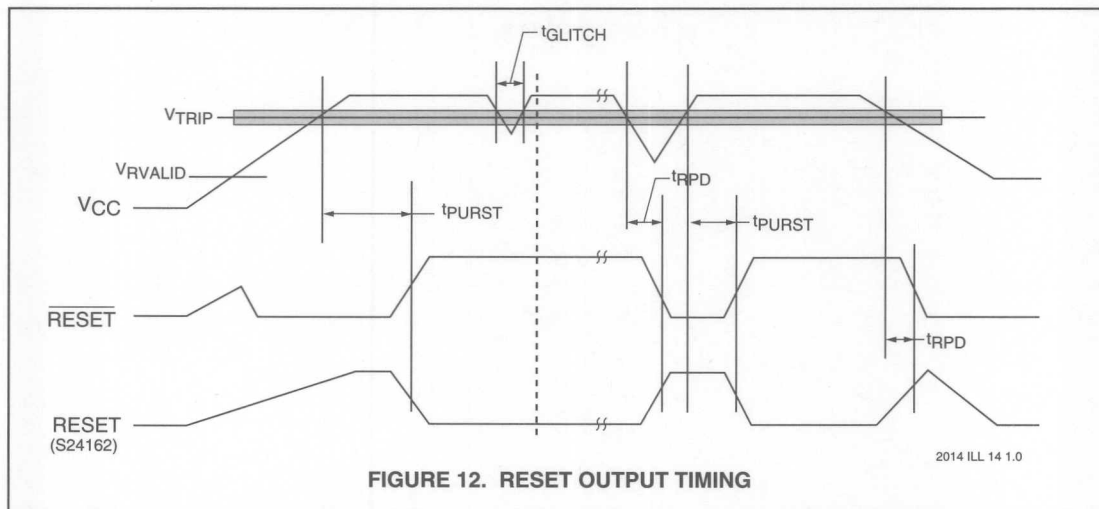


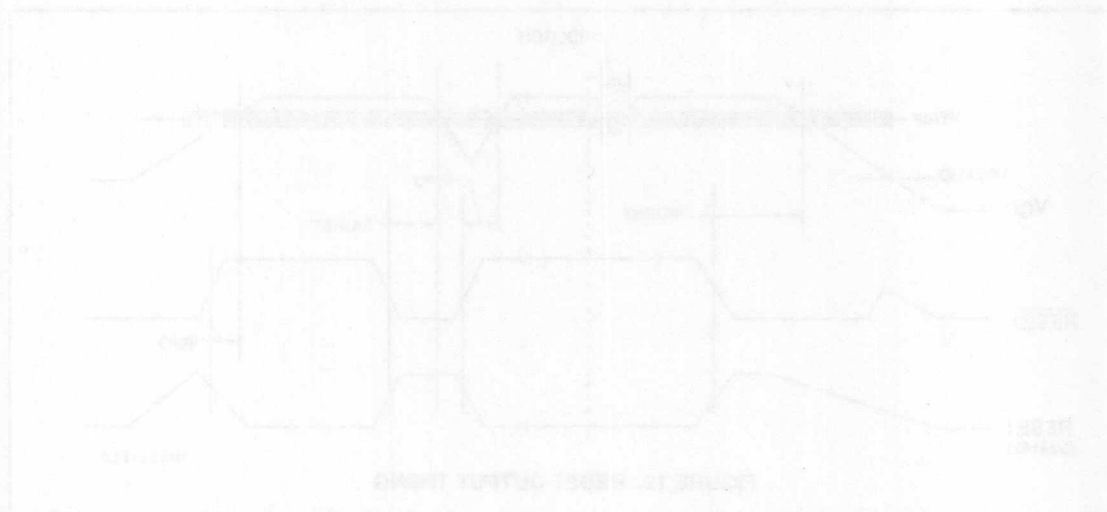
2014 ILL '13 1.0

FIGURE 11. BUS TIMING**RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS** $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	S24162/163-2.7		S24162/163-A		S24162/163-B		Unit
		Min	Max	Min	Max	Min	Max	
V_{TRIP}	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
t_{PURST}	Power-Up Reset Timeout	130	270	130	270	130	270	ms
t_{RPD}	V_{TRIP} to RESET Output Delay		5		5		5	μs
V_{RVALID}	RESET Output Valid	1		1		1		V
t_{GLITCH}	Glitch Reject Pulse Width		30		30		30	ns
V_{OLRS}	RESET Output Low Voltage $I_{OL} = 1\text{mA}$		0.4		0.4		0.4	V

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SECTION 3 **Precision Voltage Supervisory Circuit with Watchdog Timers and I²C Nonvolatile Memory**

SMS2902 Dual Reset I/Os, Watchdog and 2K Memory	3-3
SMS2904 Dual Reset I/Os, Watchdog and 4K Memory	3-17
SMS2916 Dual Reset I/Os, Watchdog and 16K Memory	3-31



SECTION 3	Excavation, Retention, Support, and Foundation
3-1	Excavation, Retention, Support, and Foundation
3-2	Excavation, Retention, Support, and Foundation
3-3	Excavation, Retention, Support, and Foundation

Precision Voltage Supervisory Circuit With Watchdog Timer and 2K I²C Memory

3 and 5 Volt Systems

FEATURES

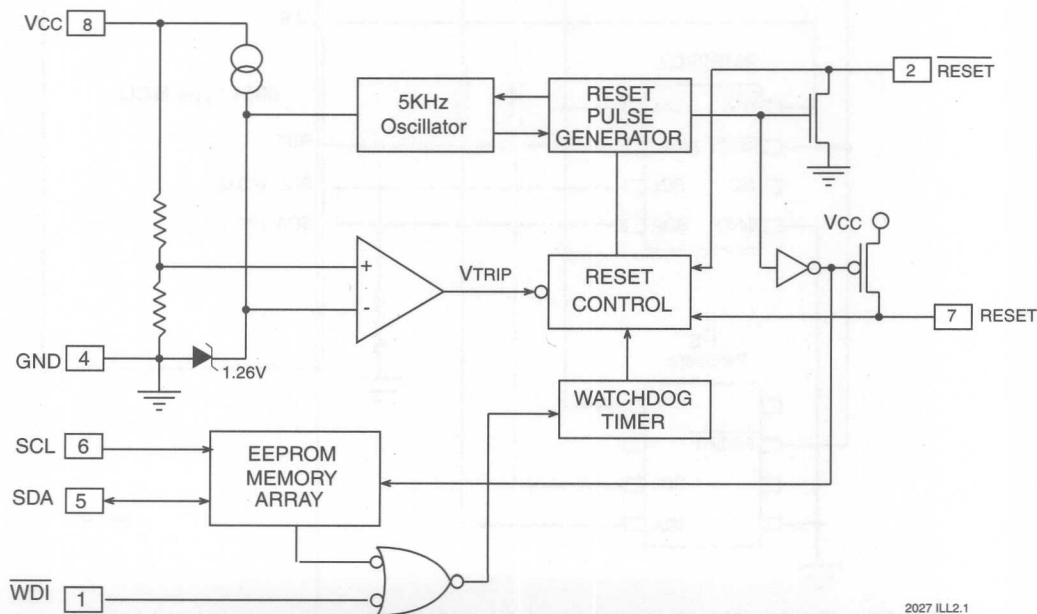
- Precision Voltage Monitor
 - Automatic V_{CC} Supply Monitor
 - Complementary reset outputs for complex microcontroller systems
 - Integrated memory write lockout function
 - No external components required
- Watchdog Timer
 - Nominal 1.6 second Timeout
- Memory Internally Organized 256 X 8
 - Two Wire Serial Interface (I²C™)
- High Reliability
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: 100 years
- 8-Pin PDIP or SOIC Packages

OVERVIEW

The SMS2902 is a power supervisory circuit that monitors V_{CC} (either in a 5V system or 3V system) and will generate complementary reset outputs. The reset pins also act as I/Os and may be used for signal conditioning. The SMS2902 also has an on-board watchdog timer that has a nominal time out period of 1.6 seconds.

The SMS2902 integrates a 2K-bit nonvolatile serial memory. It features the industry standard I²C serial interface allowing quick implementation in an end-users' system.

BLOCK DIAGRAM



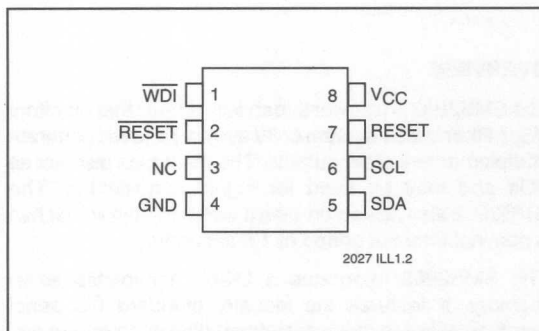
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SMS2902

Advance Information

PIN CONFIGURATIONS



PIN NAMES

Symbol	Pin	Description
WDI	1	Watchdog Input /a high to low transition will clear the watchdog timer
RESET	2	Active Low RESET Input/Output
NC	3	No Connect, tie to ground or leave open
GND	4	Analog and Digital Ground
SDA	5	Serial Memory Input/ Output data line
SCL	6	Serial Memory clock input
RESET	7	Active High RESET Input/ Output
VCC	8	Supply Voltage

2027 PGM T1.1

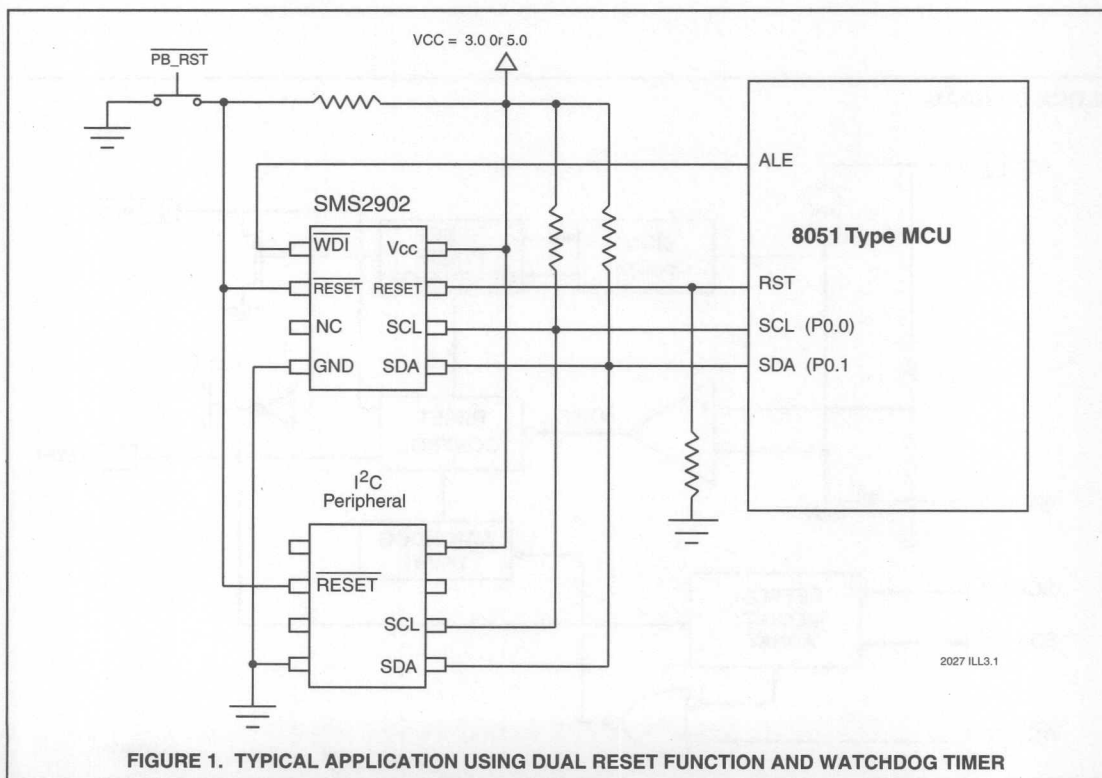
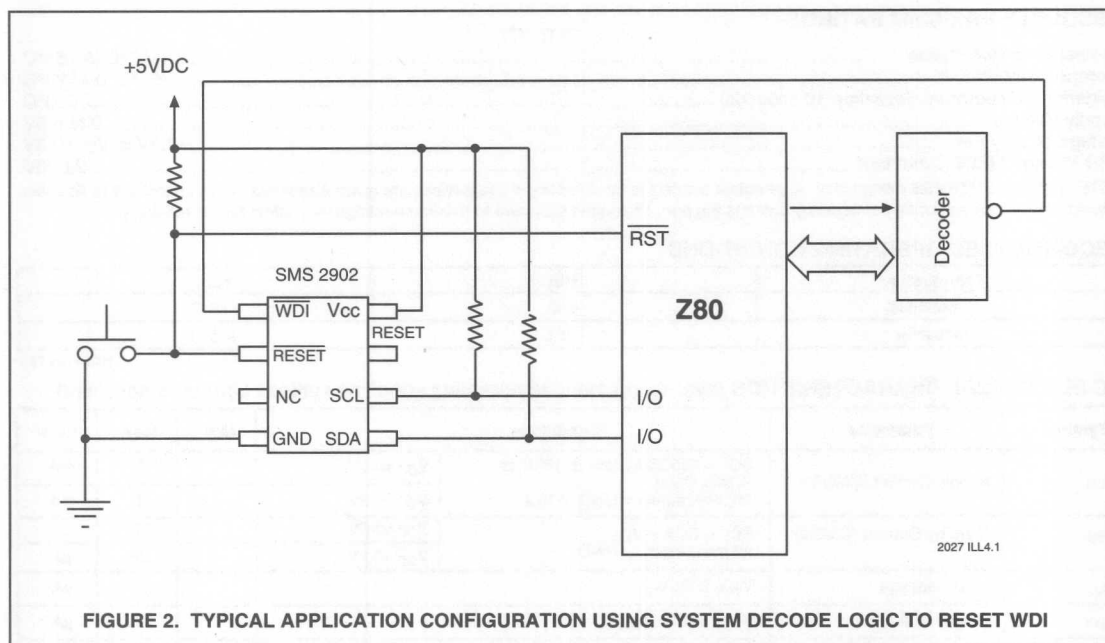


FIGURE 1. TYPICAL APPLICATION USING DUAL RESET FUNCTION AND WATCHDOG TIMER



CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C _{IN}	Input Capacitance	5	pF
L _{OUT}	Output Capacitance	8	pF

2027 PGM T2..0

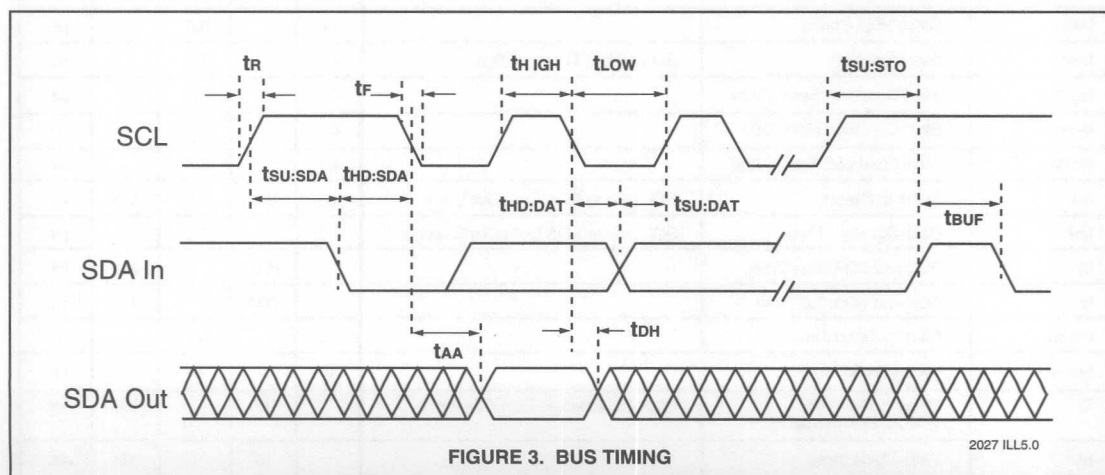


FIGURE 3. BUS TIMING

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**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

2027 PGM T3.0

DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA, RESET	$0.7 \times V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$ SDA		0.4	V

2027 PGM T4.0

AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

2027 PGM T5.0

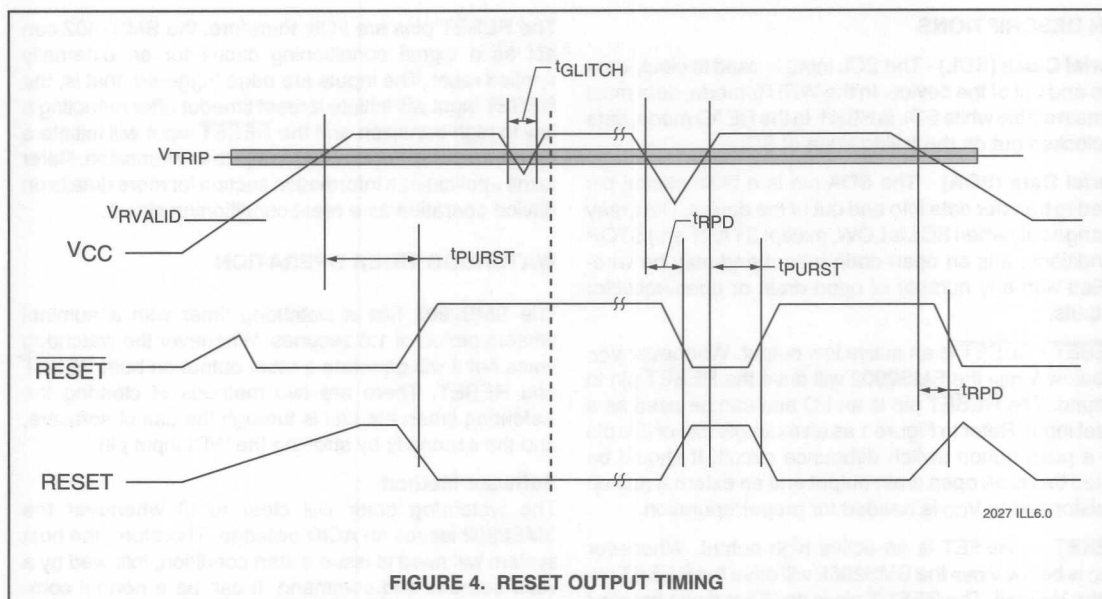


FIGURE 4. RESET OUTPUT TIMING

RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85°C

Symbol	Parameter	SMS2902-2.7		SMS2902-A		SMS2902-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
tpURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
trPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage IOL = 1mA		0.4		0.4		0.4	V
VOHRS	RESET Output High Voltage IOH = 800 μA	VCC-.75		VCC-.75		VCC-.75		V

2027 PGM T6.0

**PIN DESCRIPTIONS**

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wired ORed with any number of open-drain or open-collector outputs.

RESET - $\overline{\text{RESET}}$ is an active low output. Whenever V_{CC} is below V_{TRIP} the SMS2902 will drive the $\overline{\text{RESET}}$ pin to ground. The $\overline{\text{RESET}}$ pin is an I/O and can be used as a reset input. Refer to Figure 1 as an example use of this pin as a push button switch debounce circuit. It should be noted this is an open drain output and an external pull-up resistor tied to V_{CC} is needed for proper operation.

RESET — RESET is an active high output. Whenever V_{CC} is below V_{TRIP} the SMS2902 will drive the RESET pin to the V_{CC} rail. The RESET pin is an I/O and can be used as a reset input. It should be noted this is an open drain output and an external pull-down resistor tied to ground is needed for proper operation.

WDI - The $\overline{\text{WDI}}$ input is used as a hardware method of clearing the watchdog timer. A high to low transition on this pin will clear the watchdog timer. If a transition is not detected within 1.6 seconds the watchdog will time out and force the reset outputs active.

ENDURANCE AND DATA RETENTION

The SMS2902 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

Reset Controller Description

The SMS2902 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output.

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP} . The RESET outputs will be valid so long as V_{CC} is $> 1.0V$. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP} .

The RESET pins are I/Os; therefore, the SMS2902 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a reset conditioning circuit.

WATCHDOG TIMER OPERATION

The SMS2902 has a watchdog timer with a nominal timeout period of 1.6 seconds. Whenever the watchdog times out it will generate a reset output on both $\overline{\text{RESET}}$ and RESET. There are two methods of clearing the watchdog timer; the first is through the use of software, and the second is by strobing the WDI input pin.

Software Method

The watchdog timer will clear to t_0 whenever the SMS2902 issues an ACKnowledge. Therefore, the host system will need to issue a start condition, followed by a valid address and command. It can be a normal command as in the sequence of reading or writing to the memory, or it can be a dummy command issued solely for the purpose of resetting the watchdog timer. Refer to Figure 12 for detailed sequence of operations.

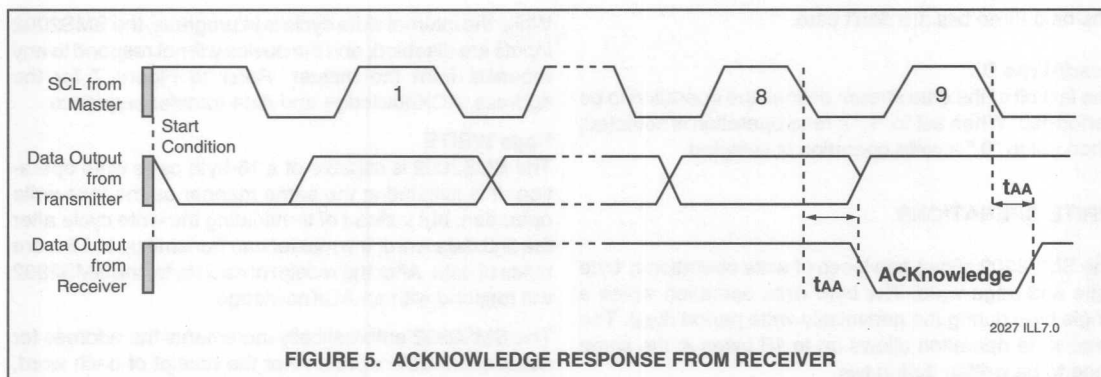
The watchdog timer will be held in the cleared state during power-on while V_{CC} is less than V_{TRIP} . Once V_{CC} exceeds V_{TRIP} the watchdog will continue to be held in a cleared state for the duration of t_{PURST} . After t_{PURST} , the timer will be released and begin counting.

If either reset input is asserted the watchdog timer will be cleared and remain in the reset condition until either t_{PURST} has expired or the reset input is released, whichever is longer.

If the watchdog times out and no action is taken by the host the SMS2902 will drive the reset outputs active for the duration of t_{PURST} at which point it will release the outputs and clear the watchdog timer again and release it to begin a new count. Refer to Figure 13 for detailed sequence of operations.

Hardware Method

A high to low transition on $\overline{\text{WDI}}$ will clear the watchdog timer. If a transition is not detected within 1.6 seconds the watchdog will time out and force the reset outputs active.



CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition.

DEVICE OPERATION

The SMS2902 is a 2K-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the SMS2902 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

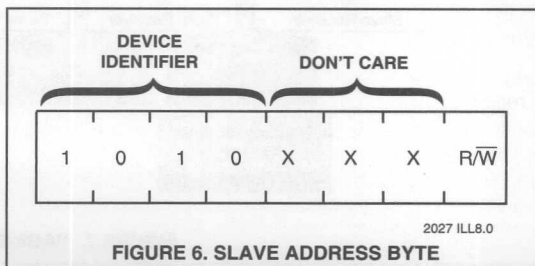
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 5).

The SMS2902 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the SMS2902 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the SMS2902 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the SMS2902 will continue to transmit data. If an ACKnowledge is not detected, the SMS2902 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 6). For the SMS2902 this is fixed as 1010[B].





The next three bits are don't care.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The SMS2902 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

Upon receipt of both the slave address and word address, the SMS2902 responds with an ACKnowledge for each. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMS2902 begins the internal write cycle.

While the internal write cycle is in progress, the SMS2902 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The SMS2902 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more bytes of data. After the receipt of each byte, the SMS2902 will respond with an ACKnowledge.

The SMS2902 automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

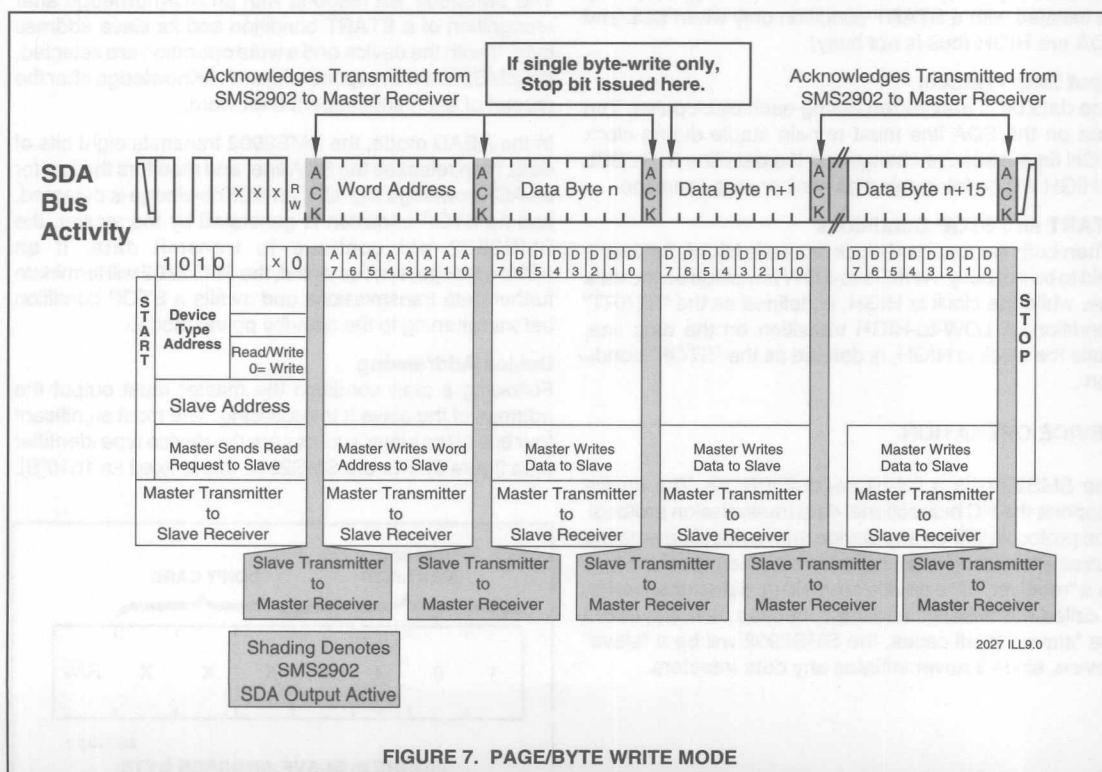


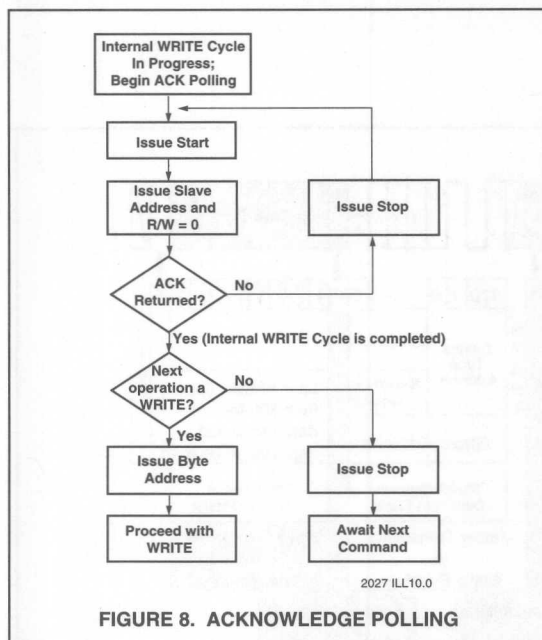
FIGURE 7. PAGE/BYTE WRITE MODE



Acknowledge Polling

When the SMS2902 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 8).



READ OPERATIONS

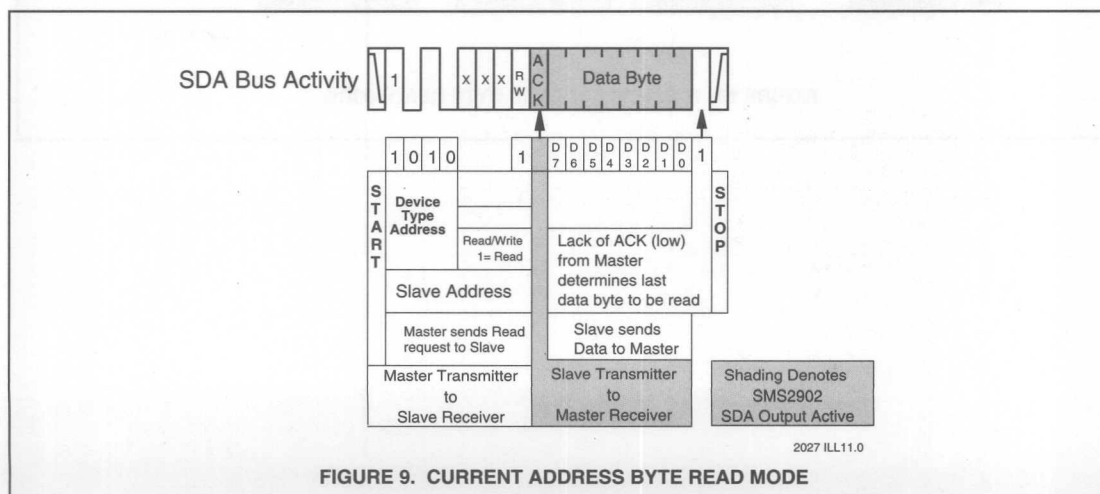
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The SMS2902 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n , the next read operation would access data from address location $n+1$ and increment the current address pointer. When the SMS2902 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location $n+1$.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the SMS2902 discontinues data transmission. See Figure 9 for the address acknowledge and data transfer sequence.





Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMS2902 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The SMS2902 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The SMS2902 discontinues data transmission and reverts to its standby power mode. See Figure 10 for the address, acknowledge and data transfer sequence.

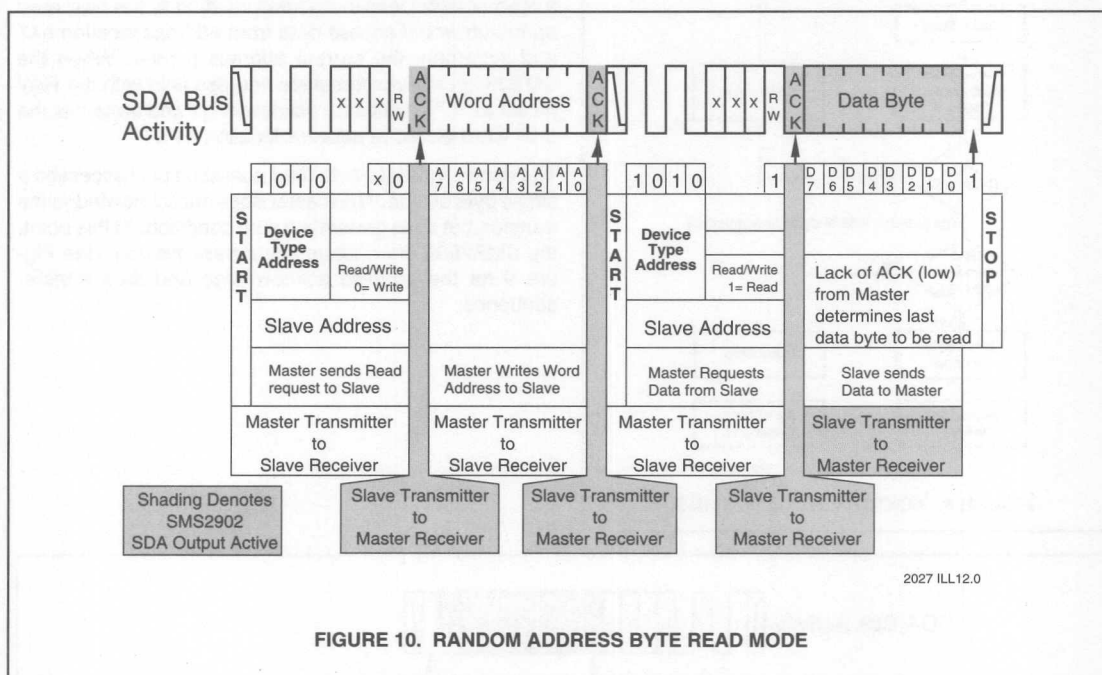


FIGURE 10. RANDOM ADDRESS BYTE READ MODE



Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the SMS2902. The SMS2902 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 11 for the address, acknowledge and data transfer sequence.

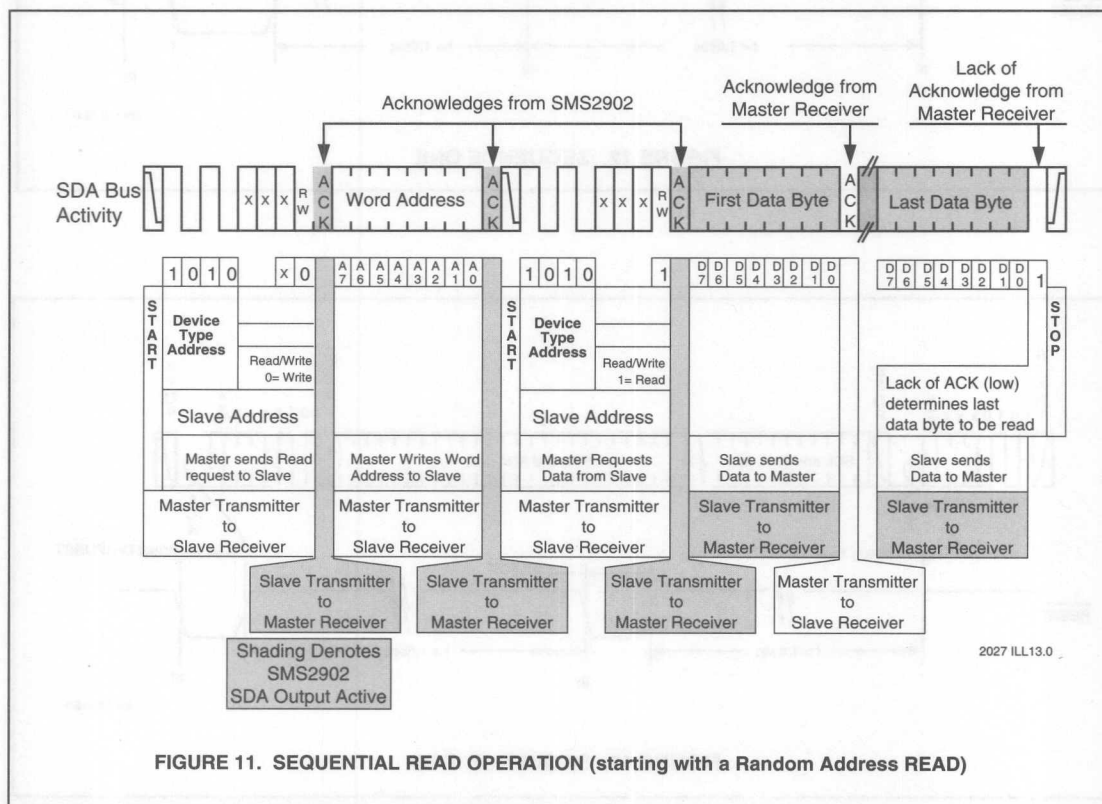


FIGURE 11. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

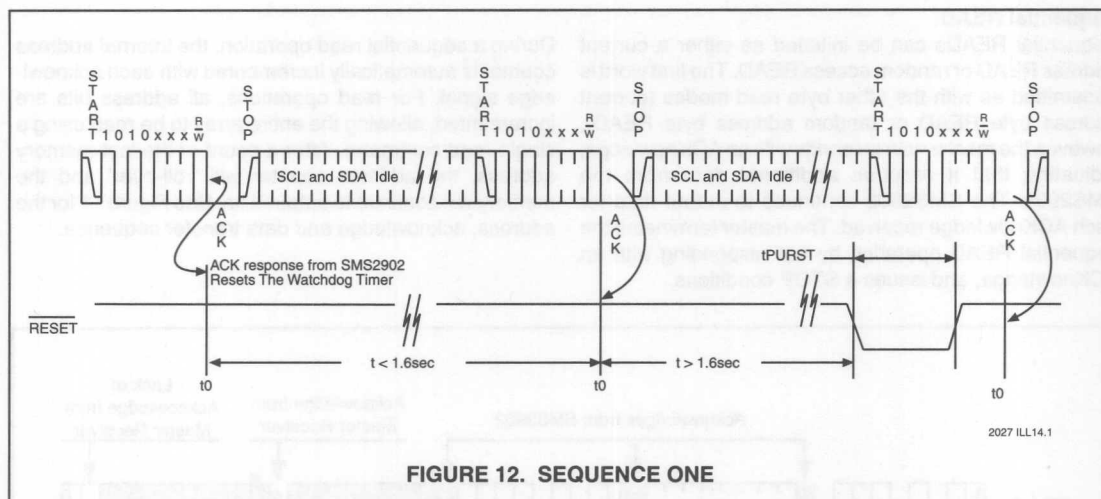


FIGURE 12. SEQUENCE ONE

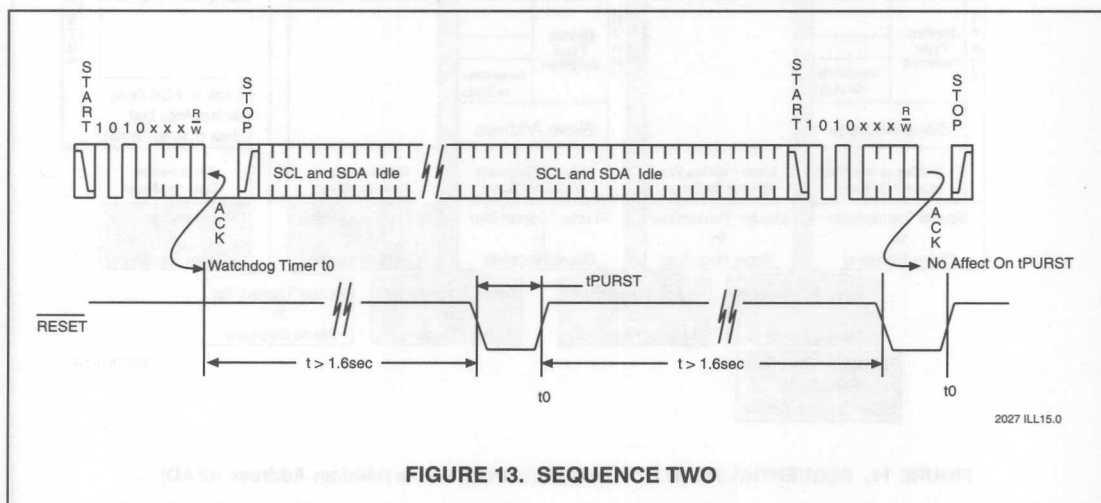
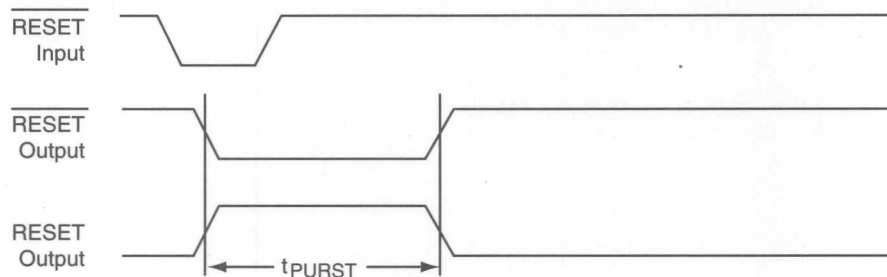


FIGURE 13. SEQUENCE TWO



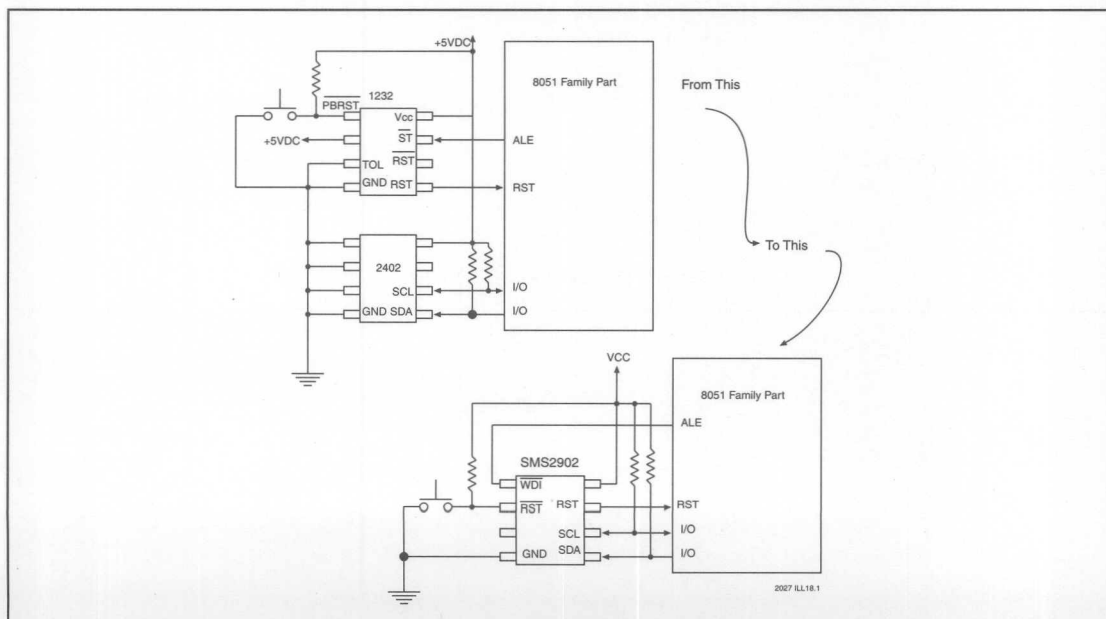
Frequently the supervisory circuit will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the SMS2902 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



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If you happen to be using one of the more common supervisory circuits like a 1232, you might consider reducing your component count such as illustrated below.

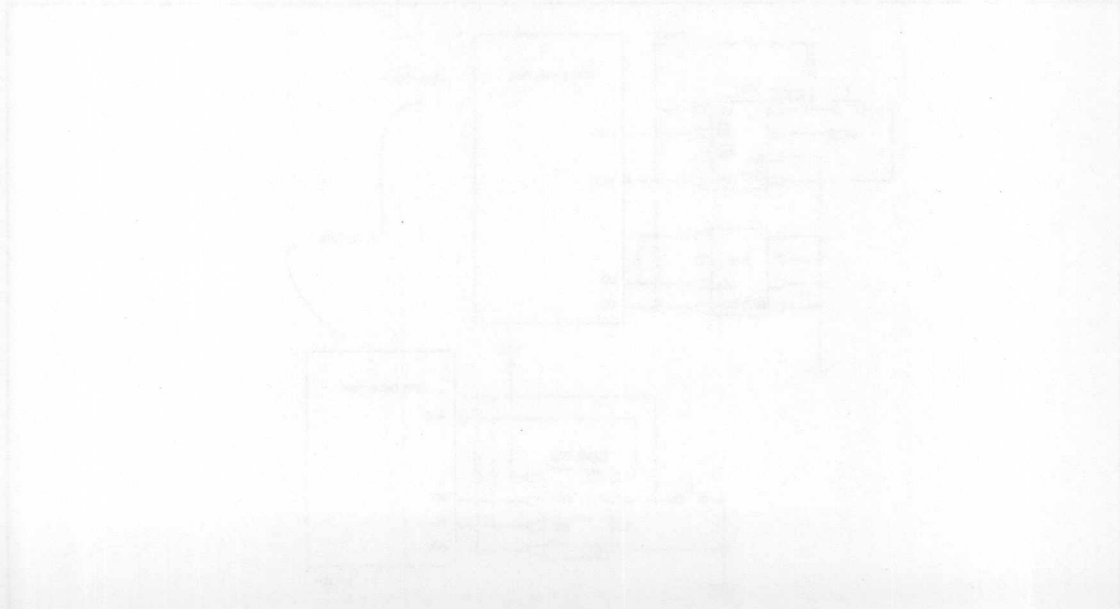




The SMS2902 is a high-speed, low-power, single-channel, single-ended, CMOS-compatible, differential-to-single-ended converter. It is designed to interface a differential signal source to a single-ended load. The device is fabricated in a 0.18 μm CMOS process and is available in a 14-pin SOIC package. It features a typical slew rate of 10 V/ns and a typical settling time of 10 ns. The device is designed to operate from a single 5 V supply and has a typical quiescent current of 10 mA. It is designed to interface a differential signal source to a single-ended load. The device is fabricated in a 0.18 μm CMOS process and is available in a 14-pin SOIC package. It features a typical slew rate of 10 V/ns and a typical settling time of 10 ns. The device is designed to operate from a single 5 V supply and has a typical quiescent current of 10 mA.



Figure 1. Timing Diagram



**Precision Voltage Supervisory Circuit
 With Watchdog Timer and 4K I²C Memory**

3 and 5 Volt Systems

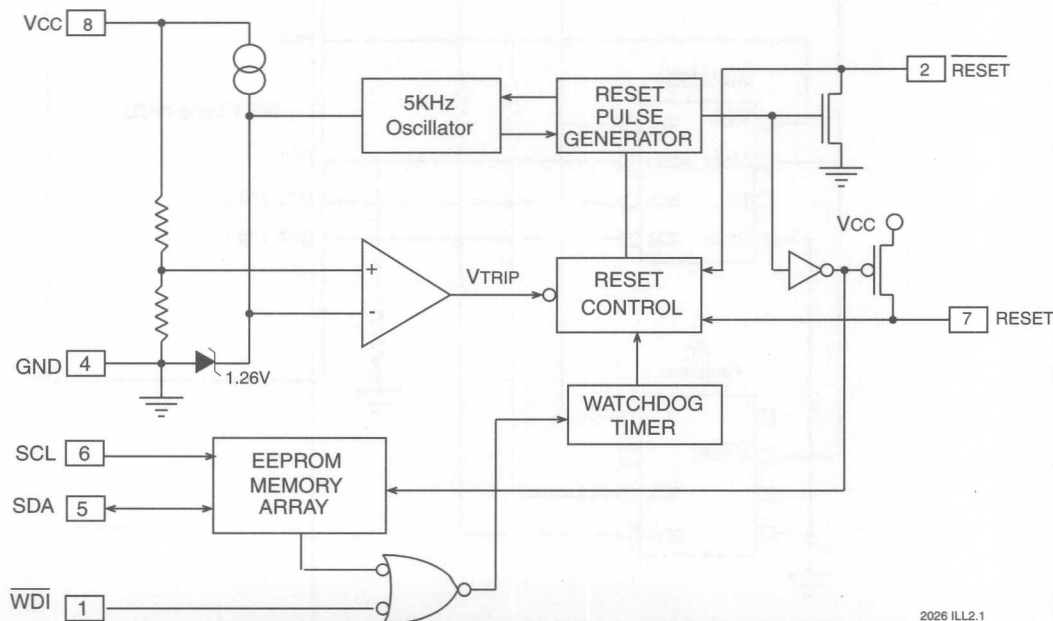
FEATURES

- **Precision Voltage Monitor**
 - Automatic V_{CC} Supply Monitor
 - Complementary reset outputs for complex microcontroller systems
 - Integrated memory write lockout function
 - No external components required
- **Watchdog Timer**
 - Nominal 1.6 second Timeout
- **Memory Internally Organized 512 X 8**
 - Two Wire Serial Interface (I²C™)
- **High Reliability**
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: 100 years
- **8-Pin PDIP or SOIC Packages**

OVERVIEW

The SMS2904 is a power supervisory circuit that monitors V_{CC} (either in a 5V system or 3V system) and will generate complementary reset outputs. The reset pins also act as I/Os and may be used for signal conditioning. The SMS2904 also has an on-board watchdog timer that has a nominal time out period of 1.6 seconds.

The SMS2904 integrates a 4K-bit nonvolatile serial memory. It features the industry standard I²C serial interface allowing quick implementation in an end-users' system.

BLOCK DIAGRAM


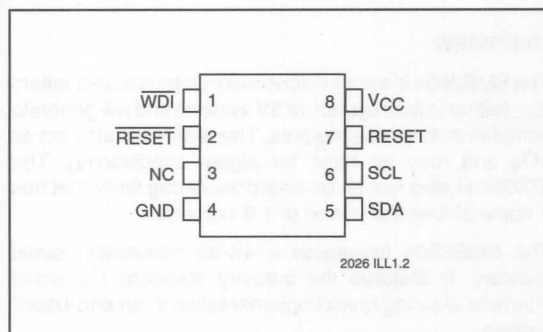
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SMS2904

Advance Information

PIN CONFIGURATIONS



PIN NAMES

Symbol	Pin	Description
WDI	1	Watchdog Input /a high to low transition will clear the watchdog timer
RESET	2	Active Low RESET Input/Output
NC	3	No Connect, tie to ground or leave open
GND	4	Analog and Digital Ground
SDA	5	Serial Memory Input/ Output data line
SCL	6	Serial Memory clock input
RESET	7	Active High RESET Input/ Output
VCC	8	Supply Voltage

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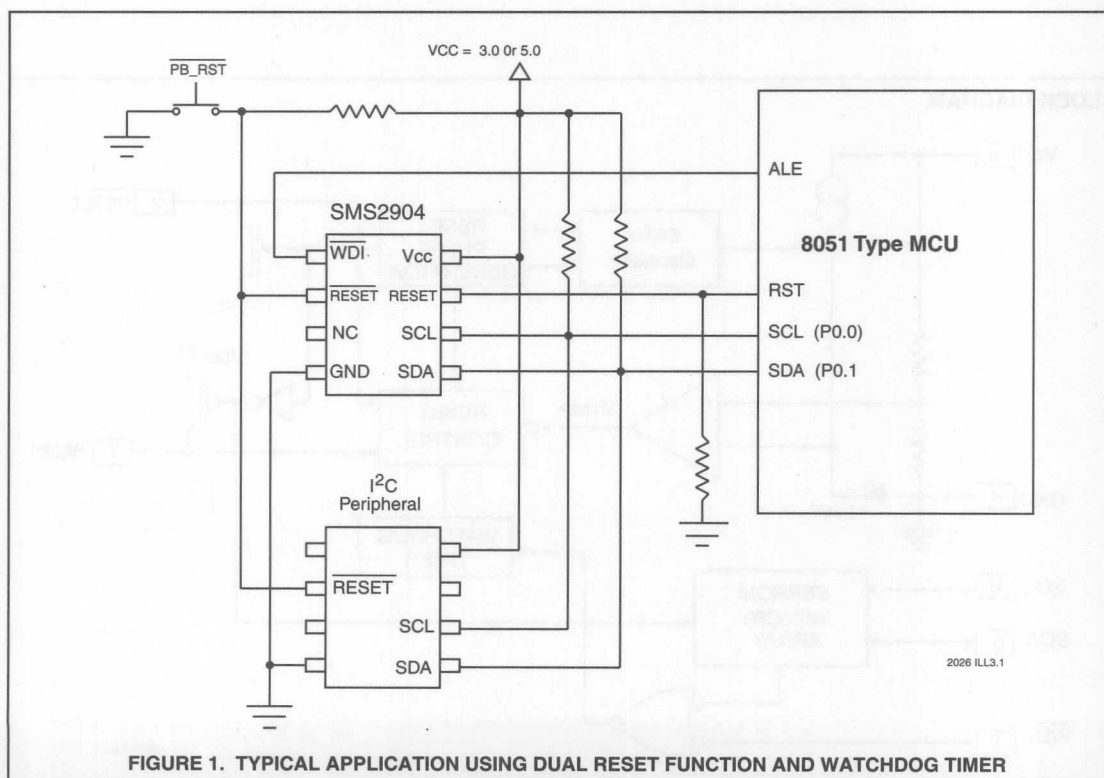
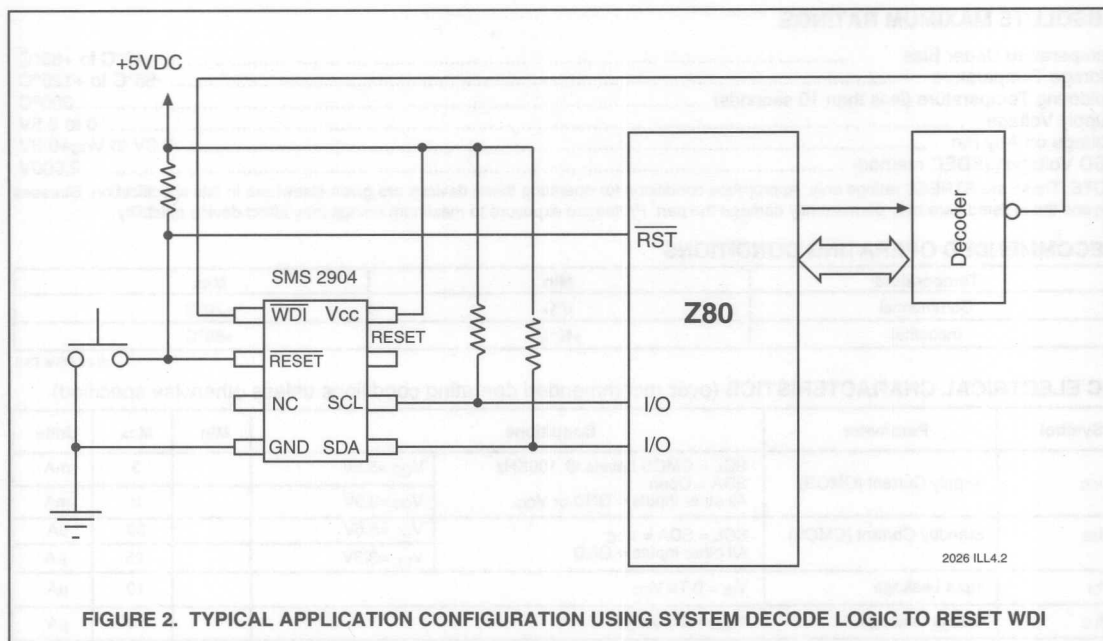
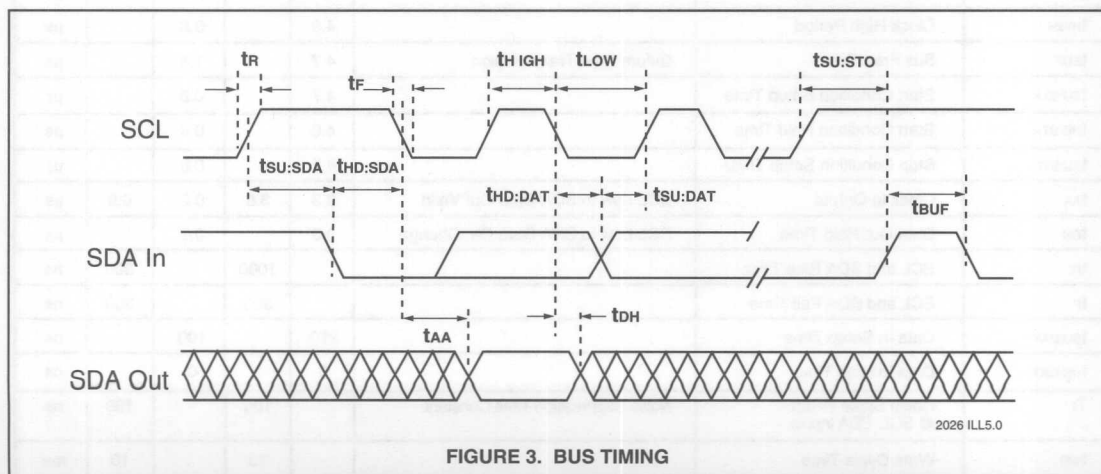


FIGURE 1. TYPICAL APPLICATION USING DUAL RESET FUNCTION AND WATCHDOG TIMER

**CAPACITANCE** $T_A = 25^{\circ}\text{C}$, $f = 100\text{KHz}$

Symbol	Parameter	Max	Units
C _{IN}	Input Capacitance	5	pF
L _{OUT}	Output Capacitance	8	pF

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SMS2904

SMS2904

Advance Information

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

2026 PGM T3.0

DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA, RESET	$0.7 \times V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$ SDA		0.4	V

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AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

2026 PGM T5.0

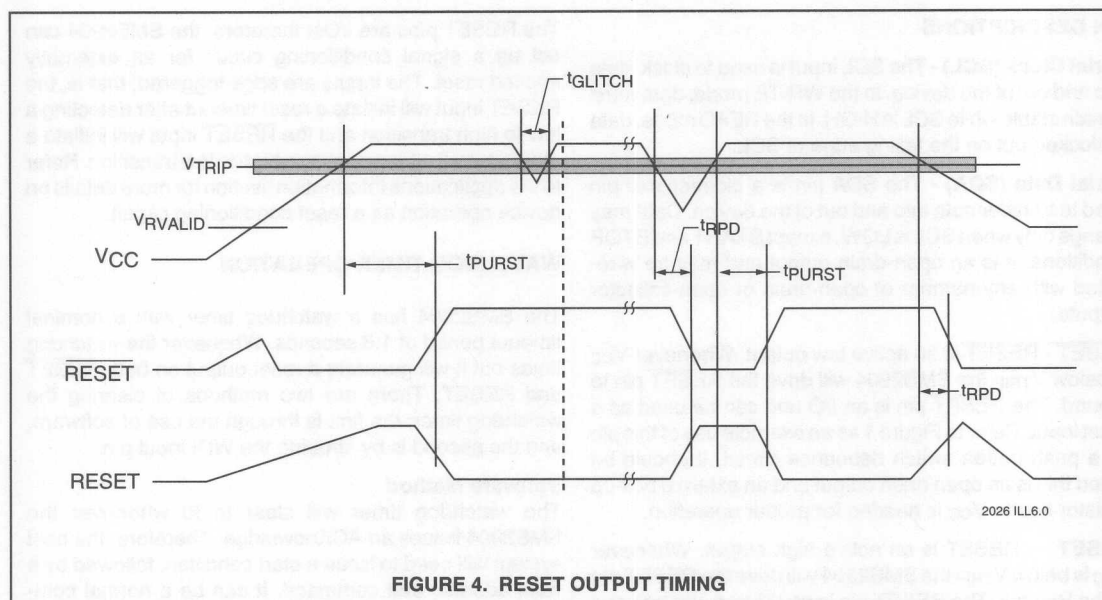


FIGURE 4. RESET OUTPUT TIMING

RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85°C

Symbol	Parameter	SMS2904-2.7		SMS2904-A		SMS2904-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
tPURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
tRPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage IOL = 1mA		0.4		0.4		0.4	V
VOHRS	RESET Output High Voltage IOH = 800 μA	VCC-.75		VCC-.75		VCC-.75		V

2026 PGM T6.1

**PIN DESCRIPTIONS**

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

RESET - $\overline{\text{RESET}}$ is an active low output. Whenever V_{CC} is below V_{TRIP} the SMS2904 will drive the $\overline{\text{RESET}}$ pin to ground. The $\overline{\text{RESET}}$ pin is an I/O and can be used as a reset input. Refer to Figure 1 as an example use of this pin as a push button switch debounce circuit. It should be noted this is an open drain output and an external pull-up resistor tied to V_{CC} is needed for proper operation.

RESET — RESET is an active high output. Whenever V_{CC} is below V_{TRIP} the SMS2904 will drive the RESET pin to the V_{CC} rail. The RESET pin is an I/O and can be used as a reset input. It should be noted this is an open drain output and an external pull-down resistor tied to ground is needed for proper operation.

WDI - The $\overline{\text{WDI}}$ input is used as a hardware method of clearing the watchdog timer. A high to low transition on this pin will clear the watchdog timer. If a transition is not detected within 1.6 seconds the watchdog will time out and force the reset outputs active.

ENDURANCE AND DATA RETENTION

The SMS2904 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

Reset Controller Description

The SMS2904 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output.

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP} . The RESET outputs will be valid so long as V_{CC} is $> 1.0V$. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP} .

The RESET pins are I/Os; therefore, the SMS2904 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the RESET input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a reset conditioning circuit.

WATCHDOG TIMER OPERATION

The SMS2904 has a watchdog timer with a nominal timeout period of 1.6 seconds. Whenever the watchdog times out it will generate a reset output on both $\overline{\text{RESET}}$ and RESET. There are two methods of clearing the watchdog timer; the first is through the use of software, and the second is by strobing the WDI input pin.

Software Method

The watchdog timer will clear to t_0 whenever the SMS2904 issues an ACKnowledge. Therefore, the host system will need to issue a start condition, followed by a valid address and command. It can be a normal command as in the sequence of reading or writing to the memory, or it can be a dummy command issued solely for the purpose of resetting the watchdog timer. Refer to Figure 12 for detailed sequence of operations.

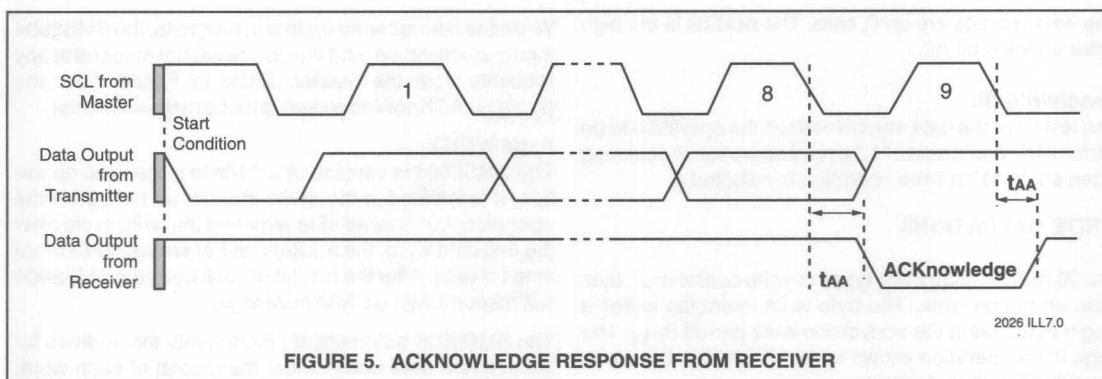
The watchdog timer will be held in the cleared state during power-on while V_{CC} is less than V_{TRIP} . Once V_{CC} exceeds V_{TRIP} the watchdog will continue to be held in a cleared state for the duration of t_{PURST} . After t_{PURST} , the timer will be released and begin counting.

If either reset input is asserted the watchdog timer will be cleared and remain in the reset condition until either t_{PURST} has expired or the reset input is released, whichever is longer.

If the watchdog times out and no action is taken by the host the SMS2904 will drive the reset outputs active for the duration of t_{PURST} at which point it will release the outputs and clear the watchdog timer again and release it to begin a new count. Refer to Figure 13 for detailed sequence of operations.

Hardware Method

A high to low transition on $\overline{\text{WDI}}$ will clear the watchdog timer. If a transition is not detected within 1.6 seconds the watchdog will time out and force the reset outputs active.

**FIGURE 5. ACKNOWLEDGE RESPONSE FROM RECEIVER**

CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition.

DEVICE OPERATION

The SMS2904 is a 4,096-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the SMS2904 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

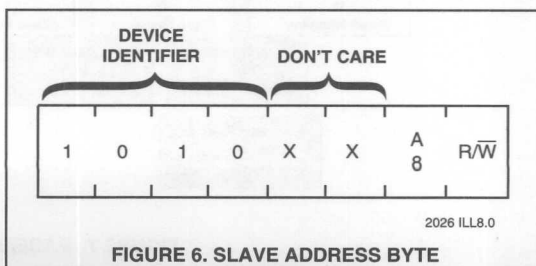
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 5).

The SMS2904 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the SMS2904 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the SMS2904 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the SMS2904 will continue to transmit data. If an ACKnowledge is not detected, the SMS2904 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 6). For the SMS2904 this is fixed as 1010[B].

**FIGURE 6. SLAVE ADDRESS BYTE**



The next two bits are don't care. The next bit is the high order address bit A8.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The SMS2904 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

Upon receipt of both the slave address and word address, the SMS2904 responds with an ACKnowledge for each. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMS2904 begins the internal write cycle.

While the internal write cycle is in progress, the SMS2904 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The SMS2904 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more bytes of data. After the receipt of each byte, the SMS2904 will respond with an ACKnowledge.

The SMS2904 automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

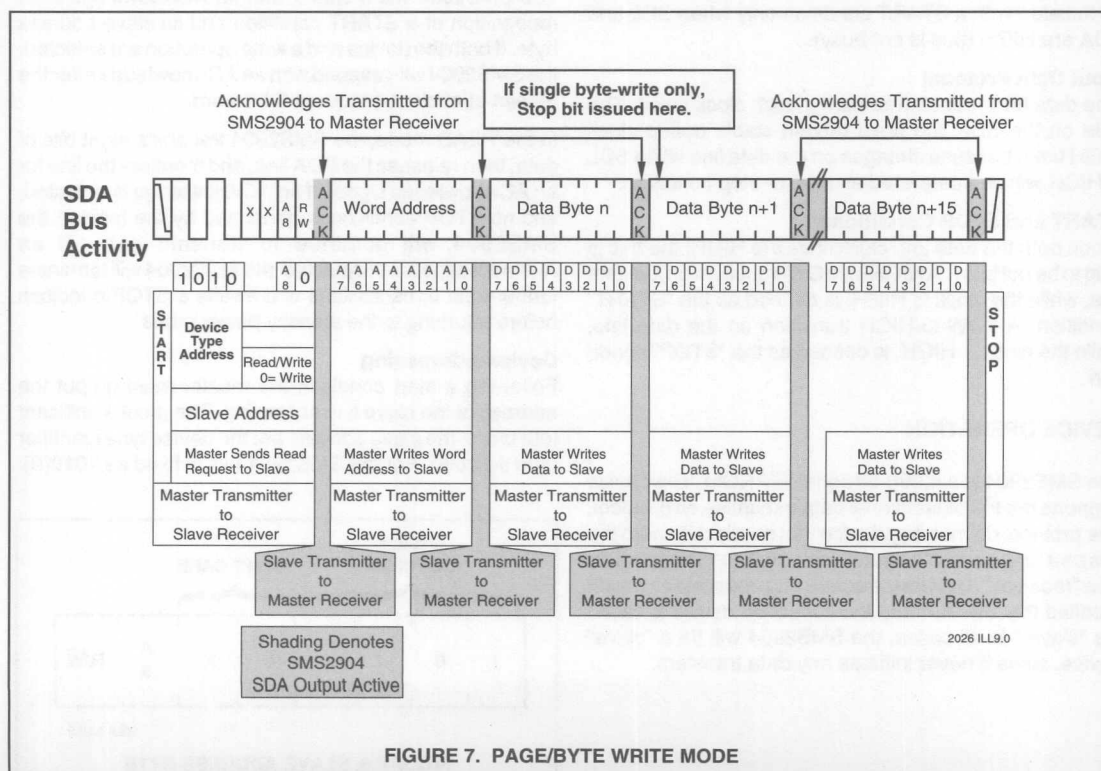


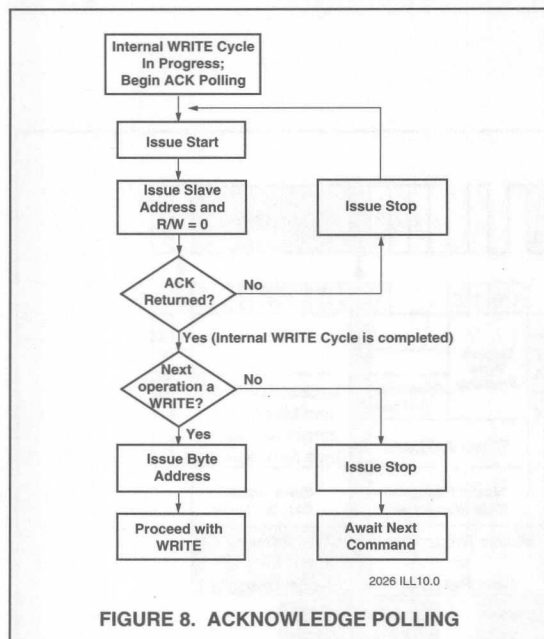
FIGURE 7. PAGE/BYTE WRITE MODE



Acknowledge Polling

When the SMS2904 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 8).



READ OPERATIONS

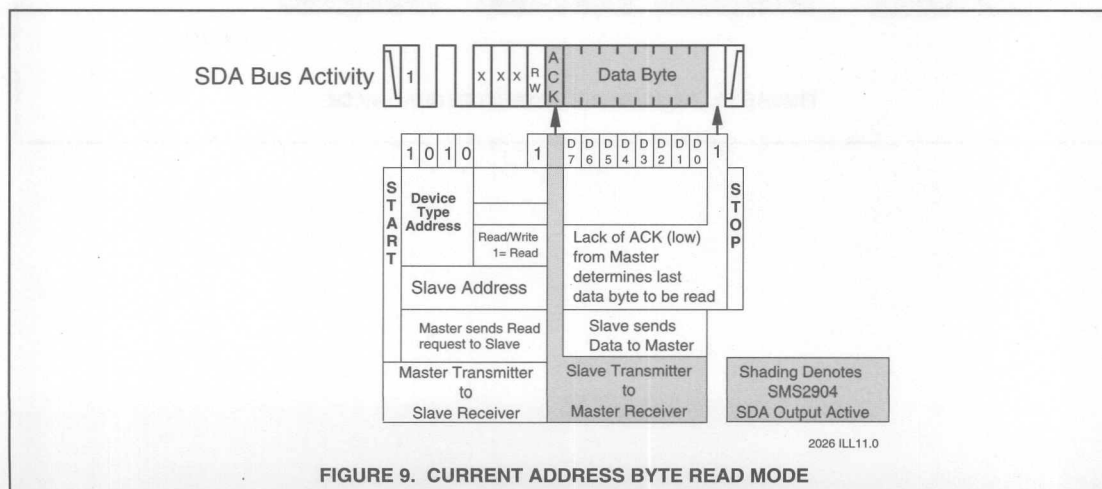
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The SMS2904 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the SMS2904 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the SMS2904 discontinues data transmission. See Figure 9 for the address acknowledge and data transfer sequence.





Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMS2904 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The SMS2904 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The SMS2904 discontinues data transmission and reverts to its standby power mode. See Figure 10 for the address, acknowledge and data transfer sequence.

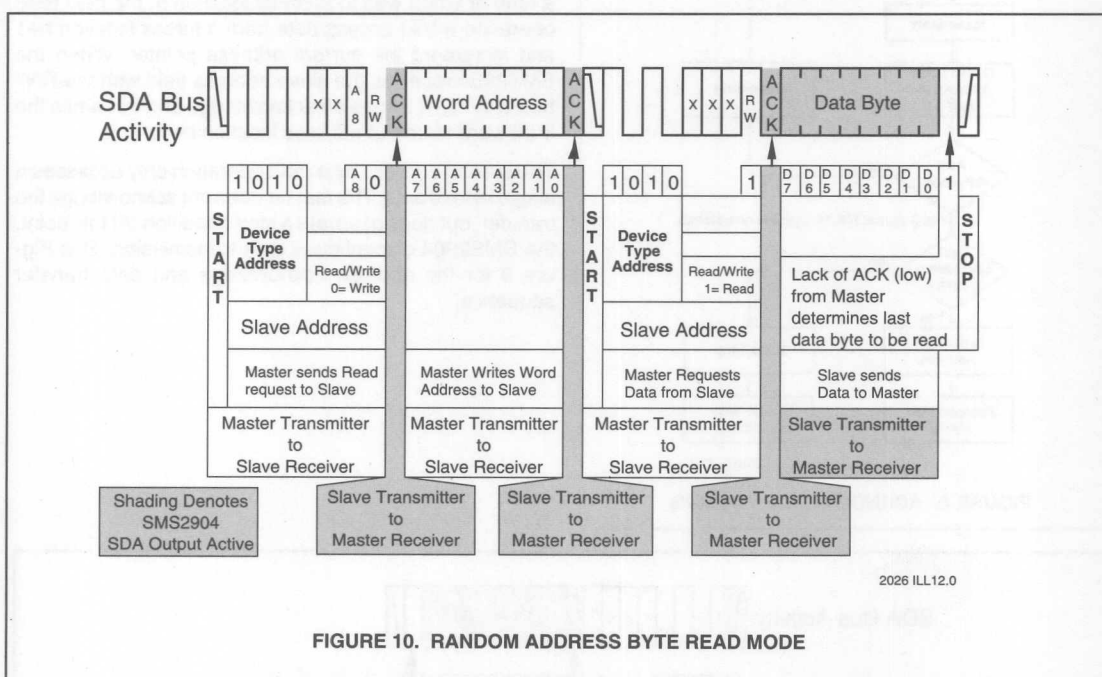


FIGURE 10. RANDOM ADDRESS BYTE READ MODE



Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the SMS2904. The SMS2904 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 11 for the address, acknowledge and data transfer sequence.

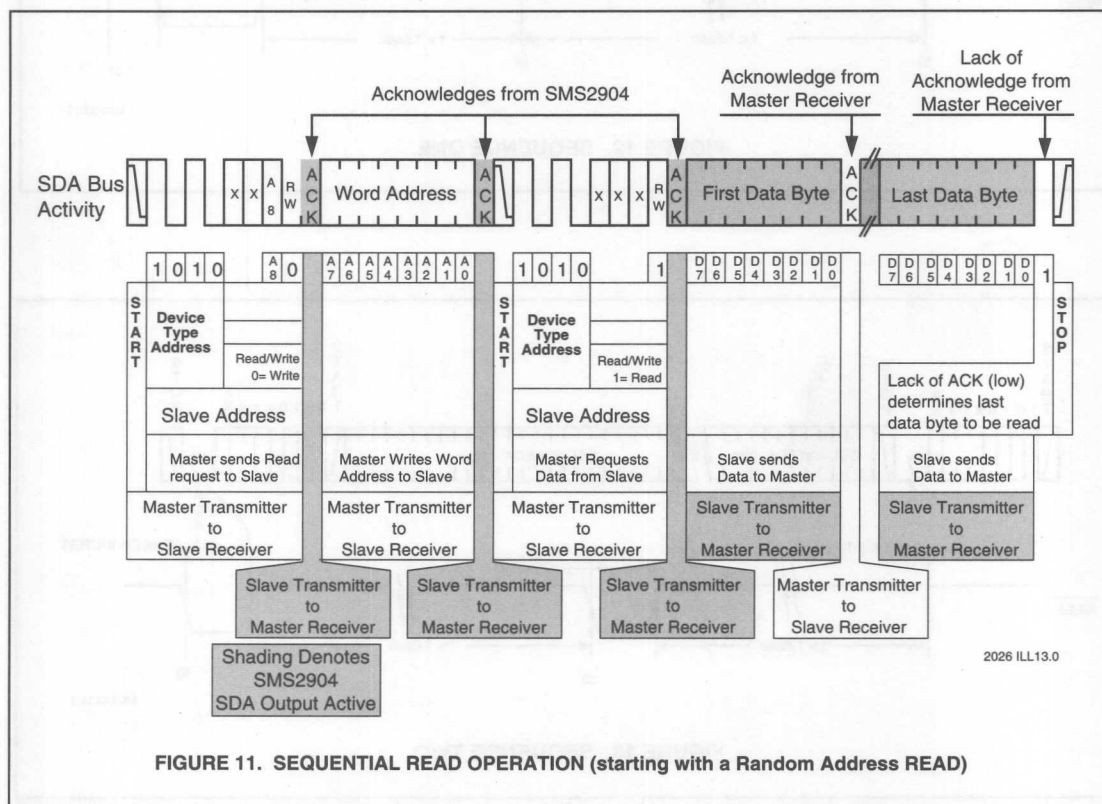
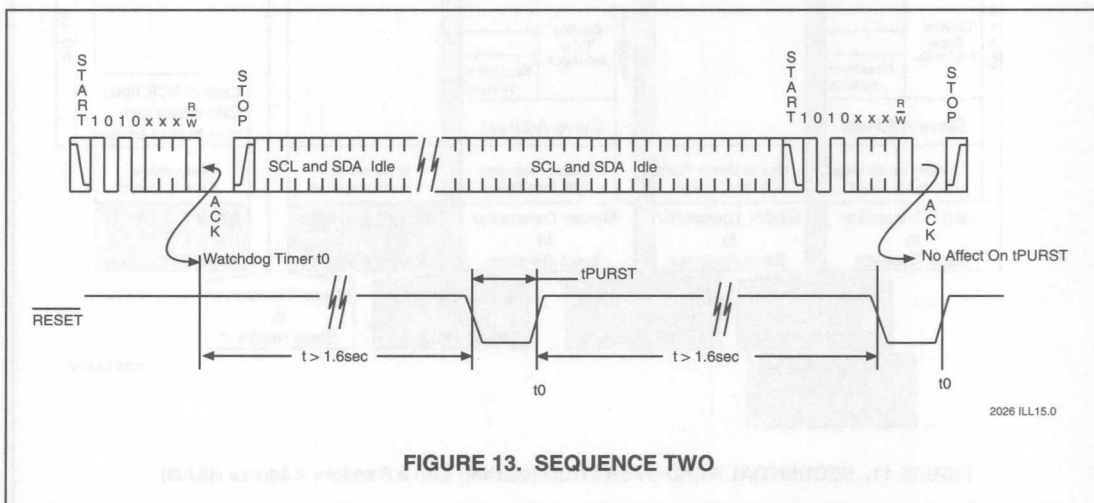
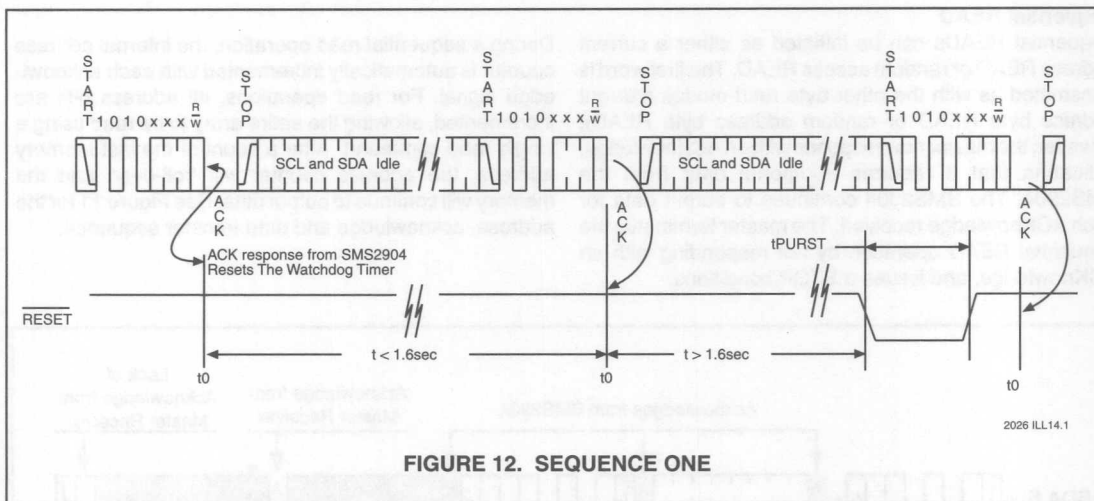


FIGURE 11. SEQUENTIAL READ OPERATION (starting with a Random Address READ)





SMS2904

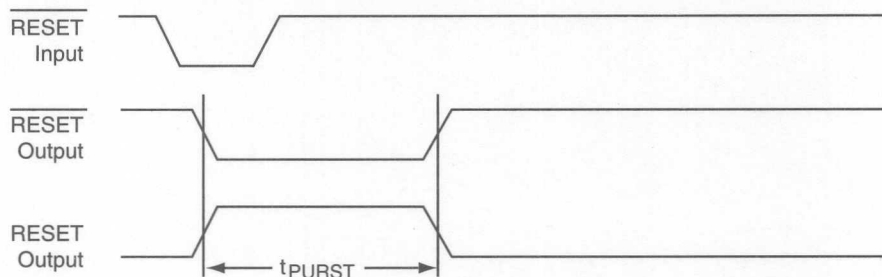
SMS2904

Advance Information



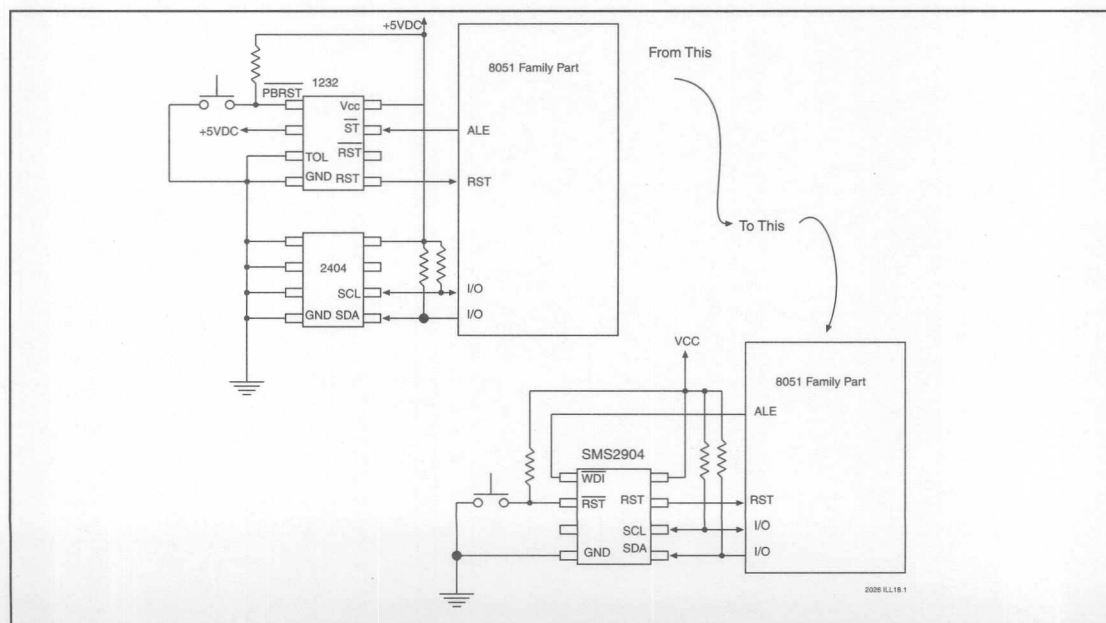
Frequently the supervisory circuit will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the SMS2904 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



2026 ILL16.0

If you happen to be using one of the more common supervisory circuits like a 1232, you might consider reducing your component count such as illustrated below.



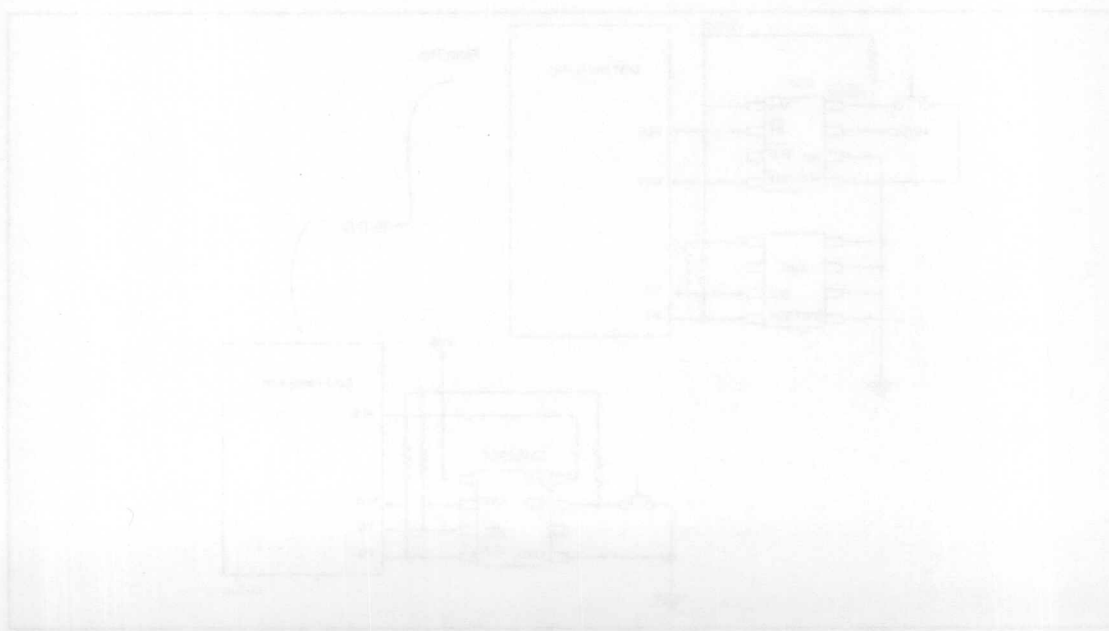
2026 ILL16.1



The SMS2904 is a high-speed, low-power, single-channel, differential line driver. It is designed to drive a wide range of loads, including twisted-pair cables, coaxial cables, and other differential signaling systems. The device is fabricated in a 0.25-μm CMOS process, which allows it to operate at high speeds while consuming very little power. It features a differential input and output, making it ideal for driving balanced lines. The device is available in a small, surface-mount package, which makes it easy to integrate into a variety of systems. The SMS2904 is a versatile and reliable component for any application requiring high-speed, low-power differential signaling.



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**Precision Voltage Supervisory Circuit
 With Watchdog Timer and 16K I²C Memory**

3 and 5 Volt Systems

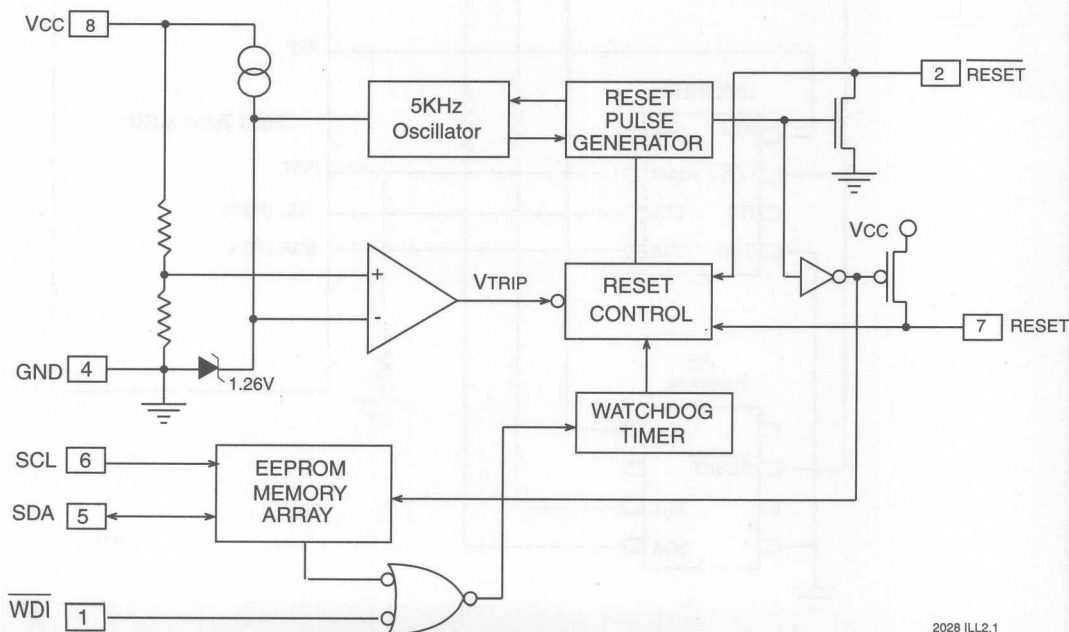
FEATURES

- Precision Voltage Monitor
 - Automatic V_{CC} Supply Monitor
 - Complementary reset outputs for complex microcontroller systems
 - Integrated memory write lockout function
 - No external components required
- Watchdog Timer
 - Nominal 1.6 second Timeout
- Memory Internally Organized 2K X 8
 - Two Wire Serial Interface (I²C™)
- High Reliability
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: 100 years
- 8-Pin PDIP or SOIC Packages

OVERVIEW

The SMS2916 is a power supervisory circuit that monitors V_{CC} (either in a 5V system or 3V system) and will generate complementary reset outputs. The reset pins also act as I/Os and may be used for signal conditioning. The SMS2916 also has an on-board watchdog timer that has a nominal time out period of 1.6 seconds.

The SMS2916 integrates a 16K-bit nonvolatile serial memory. It features the industry standard I²C serial interface allowing quick implementation in an end-users' system.

BLOCK DIAGRAM


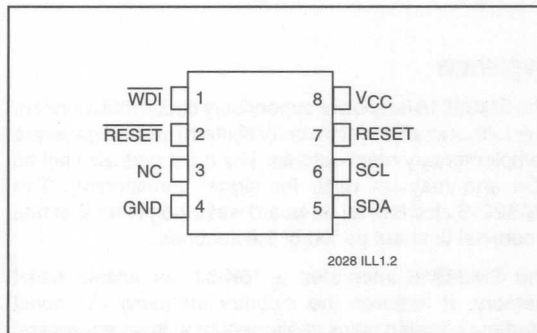
2028 ILL2.1



SMS2916

Preliminary

PIN CONFIGURATIONS



PIN NAMES

Symbol	Pin	Description
$\overline{\text{WDI}}$	1	Watchdog Input /a high to low transition will clear the watchdog timer
$\overline{\text{RESET}}$	2	Active Low RESET Input/Output
NC	3	No Connect, tie to ground or leave open
GND	4	Analog and Digital Ground
SDA	5	Serial Memory Input/ Output data line
SCL	6	Serial Memory clock input
RESET	7	Active High RESET Input/ Output
Vcc	8	Supply Voltage

2028 PGM T1.1

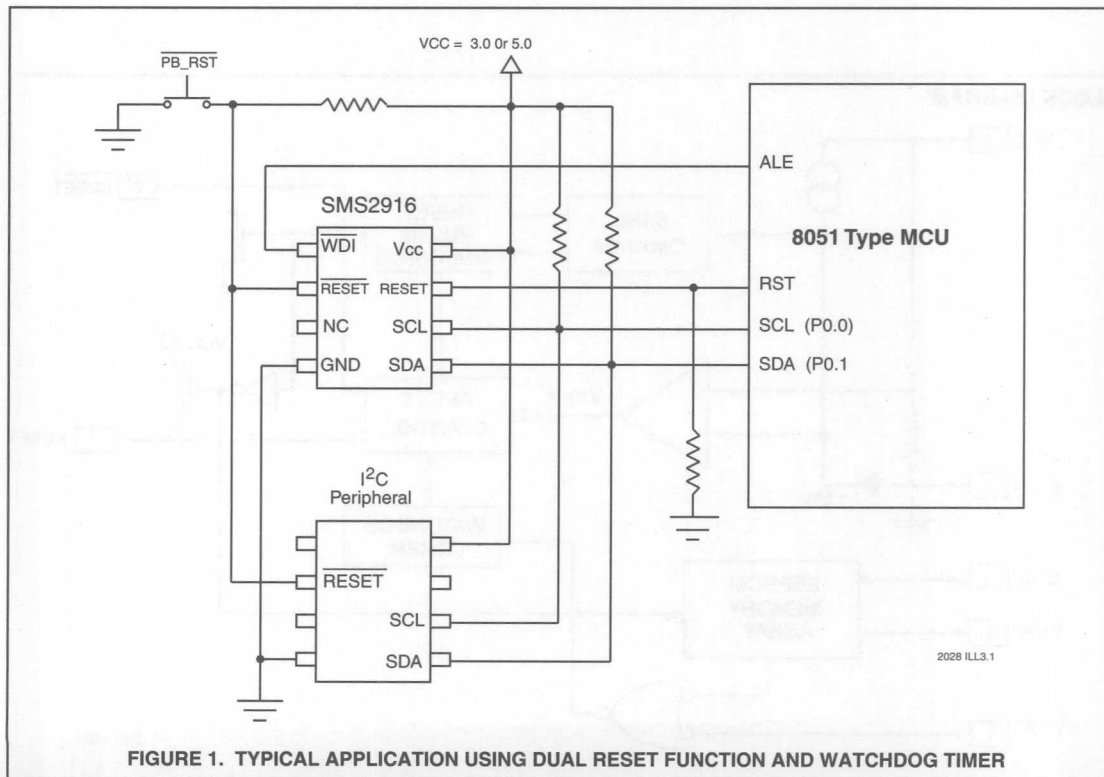
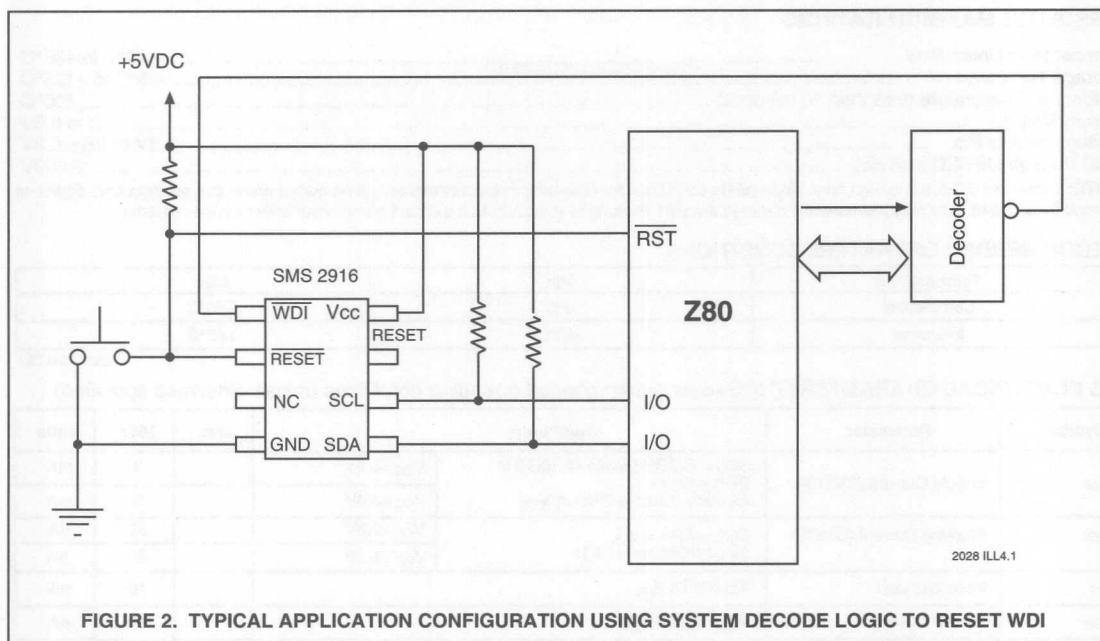
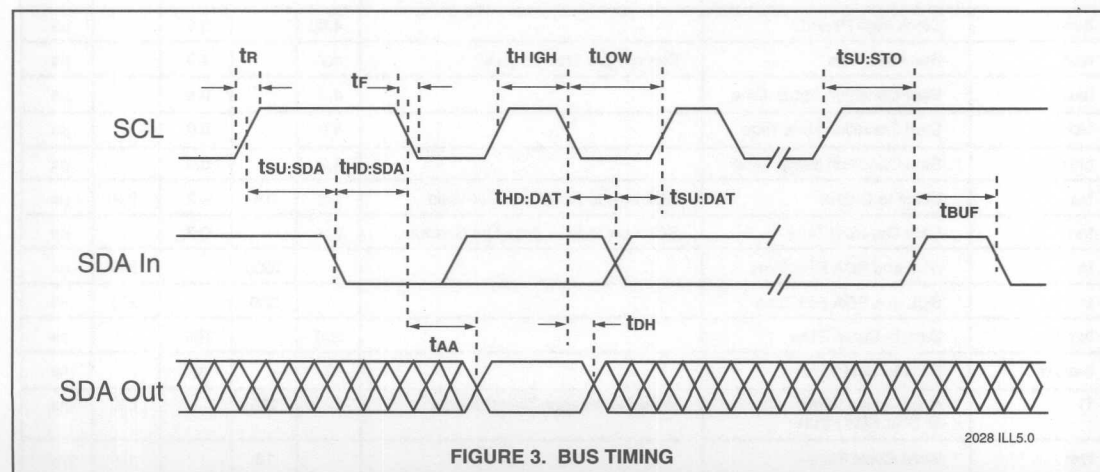


FIGURE 1. TYPICAL APPLICATION USING DUAL RESET FUNCTION AND WATCHDOG TIMER

**FIGURE 2. TYPICAL APPLICATION CONFIGURATION USING SYSTEM DECODE LOGIC TO RESET WDI****CAPACITANCE** $T_A = 25^\circ\text{C}$, $f = 100\text{KHz}$

Symbol	Parameter	Max	Units
C _{IN}	Input Capacitance	5	pF
L _{OUT}	Output Capacitance	8	pF

2028 PGM T2..0

**FIGURE 3. BUS TIMING**

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

2028 PGM T3.0

DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA, RESET	$0.7 \times V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$ SDA		0.4	V

2028 PGM T4.0

AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

2028 PGM T5.0

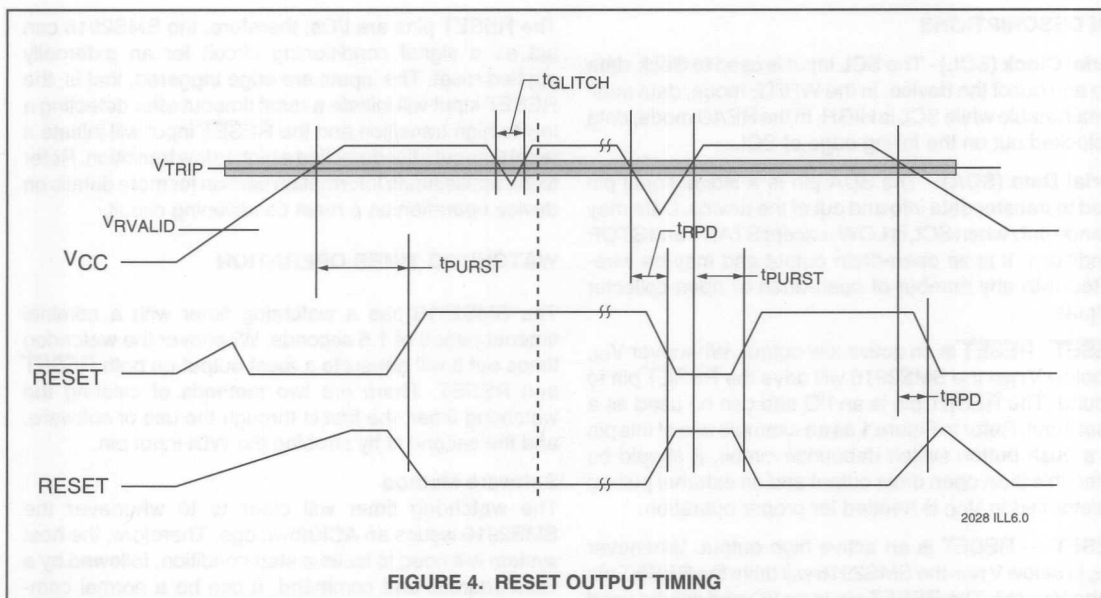


FIGURE 4. RESET OUTPUT TIMING

RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85°C

Symbol	Parameter	SMS2916-2.7		SMS2916-A		SMS2916-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
tpURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
trPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage IOL = 1mA		0.4		0.4		0.4	V
VOHRS	RESET Output High Voltage IOH = 800 μA	VCC-.75		VCC-.75		VCC-.75		V

2028 PGM T6.0



PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

RESET - $\overline{\text{RESET}}$ is an active low output. Whenever V_{CC} is below V_{TRIP} the SMS2916 will drive the $\overline{\text{RESET}}$ pin to ground. The $\overline{\text{RESET}}$ pin is an I/O and can be used as a reset input. Refer to Figure 1 as an example use of this pin as a push button switch debounce circuit. It should be noted this is an open drain output and an external pull-up resistor tied to V_{CC} is needed for proper operation.

RESET — RESET is an active high output. Whenever V_{CC} is below V_{TRIP} the SMS2916 will drive the RESET pin to the V_{CC} rail. The RESET pin is an I/O and can be used as a reset input. It should be noted this is an open drain output and an external pull-down resistor tied to ground is needed for proper operation.

WDI - The $\overline{\text{WDI}}$ input is used as a hardware method of clearing the watchdog timer. A high to low transition on this pin will clear the watchdog timer. If a transition is not detected within 1.6 seconds the watchdog will time out and force the reset outputs active.

ENDURANCE AND DATA RETENTION

The SMS2916 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

Reset Controller Description

The SMS2916 provides a precision $\overline{\text{RESET}}$ controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain $\overline{\text{RESET}}$ outputs; pin 7 is an active high output and pin 2 is an active low output.

During power-up, the $\overline{\text{RESET}}$ outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP} . The $\overline{\text{RESET}}$ outputs will be valid so long as V_{CC} is $> 1.0V$. During power-down, the $\overline{\text{RESET}}$ outputs will begin driving active when V_{CC} falls below V_{TRIP} .

The $\overline{\text{RESET}}$ pins are I/Os; therefore, the SMS2916 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a low to high transition and the RESET input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a reset conditioning circuit.

WATCHDOG TIMER OPERATION

The SMS2916 has a watchdog timer with a nominal timeout period of 1.6 seconds. Whenever the watchdog times out it will generate a reset output on both $\overline{\text{RESET}}$ and RESET . There are two methods of clearing the watchdog timer; the first is through the use of software, and the second is by strobing the $\overline{\text{WDI}}$ input pin.

Software Method

The watchdog timer will clear to t_0 whenever the SMS2916 issues an ACKnowledge. Therefore, the host system will need to issue a start condition, followed by a valid address and command. It can be a normal command as in the sequence of reading or writing to the memory, or it can be a dummy command issued solely for the purpose of resetting the watchdog timer. Refer to Figure 12 for detailed sequence of operations.

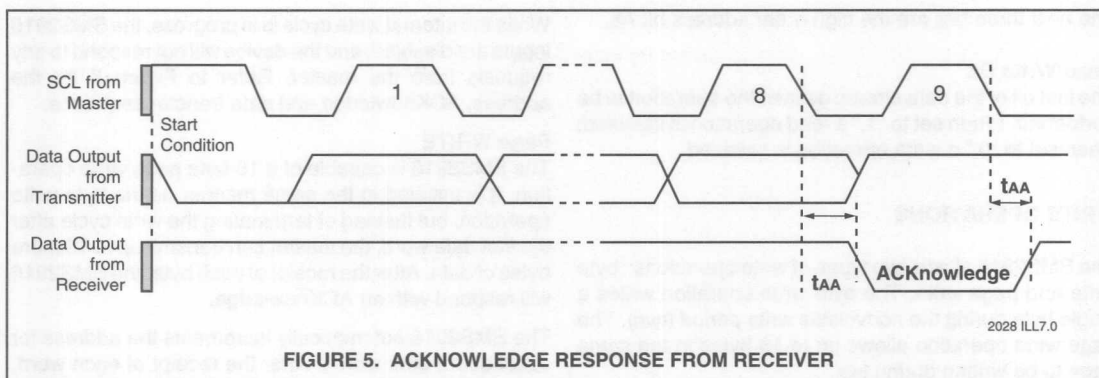
The watchdog timer will be held in the cleared state during power-on while V_{CC} is less than V_{TRIP} . Once V_{CC} exceeds V_{TRIP} the watchdog will continue to be held in a cleared state for the duration of t_{PURST} . After t_{PURST} , the timer will be released and begin counting.

If either reset input is asserted the watchdog timer will be cleared and remain in the reset condition until either t_{PURST} has expired or the reset input is released, whichever is longer.

If the watchdog times out and no action is taken by the host the SMS2916 will drive the reset outputs active for the duration of t_{PURST} at which point it will release the outputs and clear the watchdog timer again and release it to begin a new count. Refer to Figure 13 for detailed sequence of operations.

Hardware Method

A high to low transition on $\overline{\text{WDI}}$ will clear the watchdog timer. If a transition is not detected within 1.6 seconds the watchdog will time out and force the reset outputs active.



CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition.

DEVICE OPERATION

The SMS2916 is a 16K-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the SMS2916 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

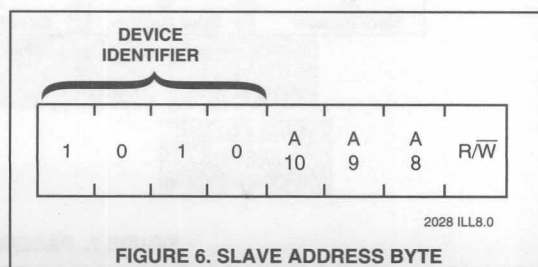
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 5).

The SMS2916 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the SMS2916 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the SMS2916 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the SMS2916 will continue to transmit data. If an ACKnowledge is not detected, the SMS2916 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 6). For the SMS2916 this is fixed as 1010[B].





The next three bits are the high order address bit A8.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The SMS2916 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

Upon receipt of both the slave address and word address, the SMS2916 responds with an ACKnowledge for each. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMS2916 begins the internal write cycle.

While the internal write cycle is in progress, the SMS2916 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The SMS2916 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more bytes of data. After the receipt of each byte, the SMS2916 will respond with an ACKnowledge.

The SMS2916 automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

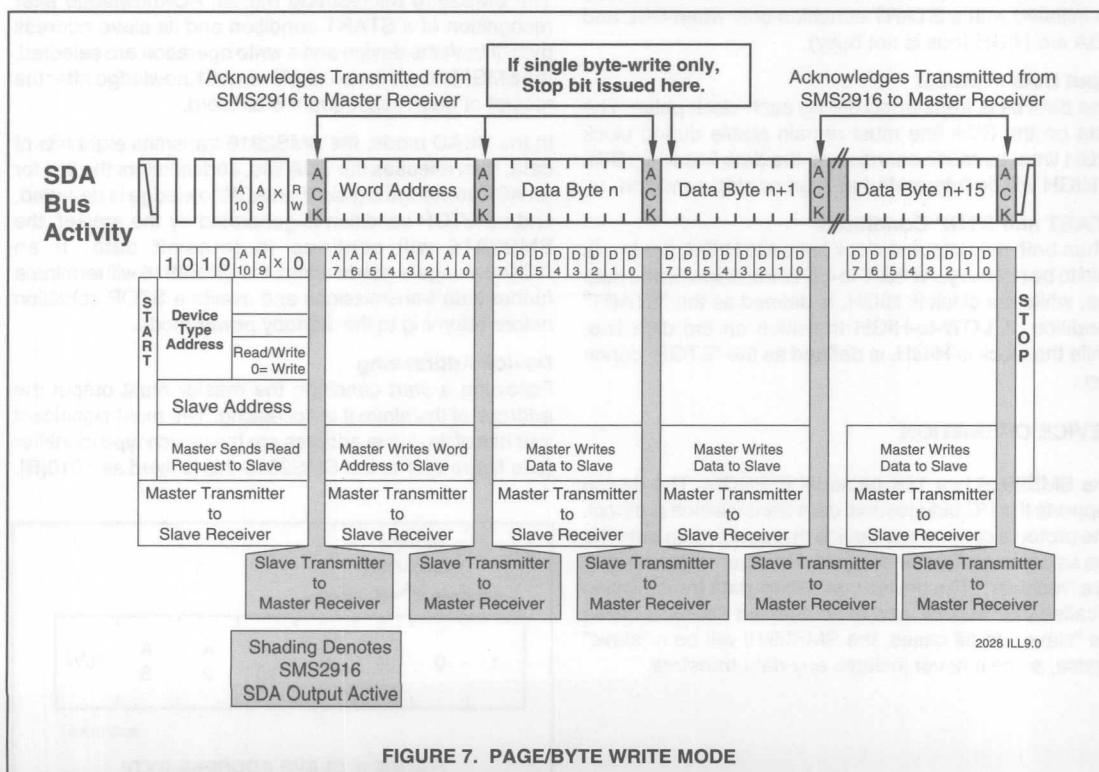


FIGURE 7. PAGE/BYTE WRITE MODE



Acknowledge Polling

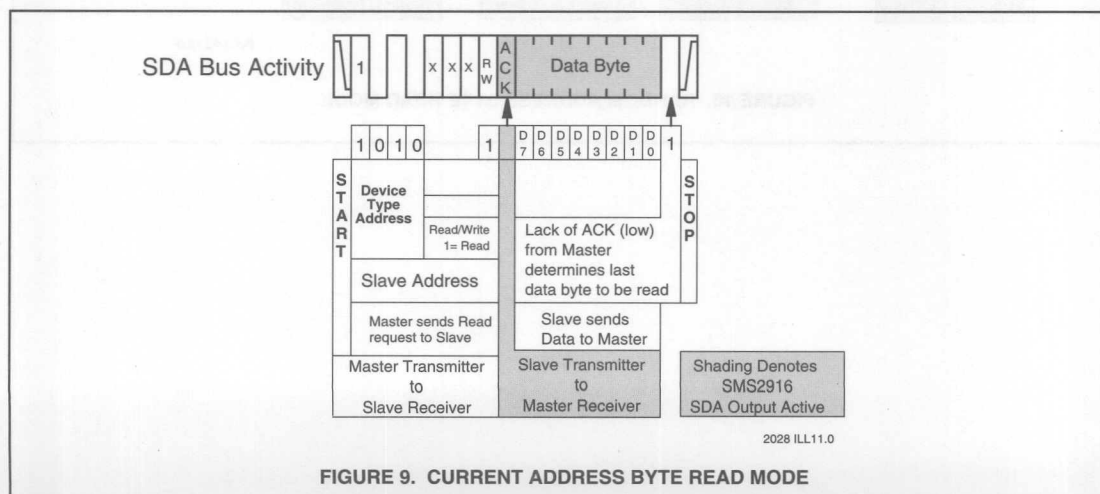
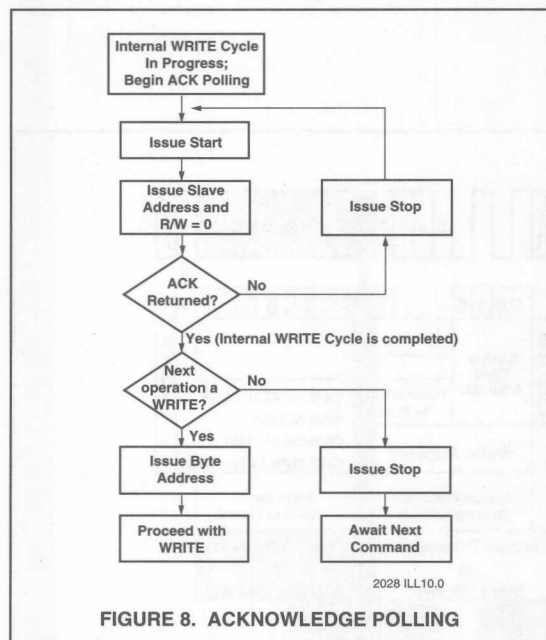
To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 8).

READ OPERATIONS

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the SMS2916 discontinues data transmission. See Figure 9 for the address acknowledge and data transfer sequence.





Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMS2916 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The SMS2916 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The SMS2916 discontinues data transmission and reverts to its standby power mode. See Figure 10 for the address, acknowledge and data transfer sequence.

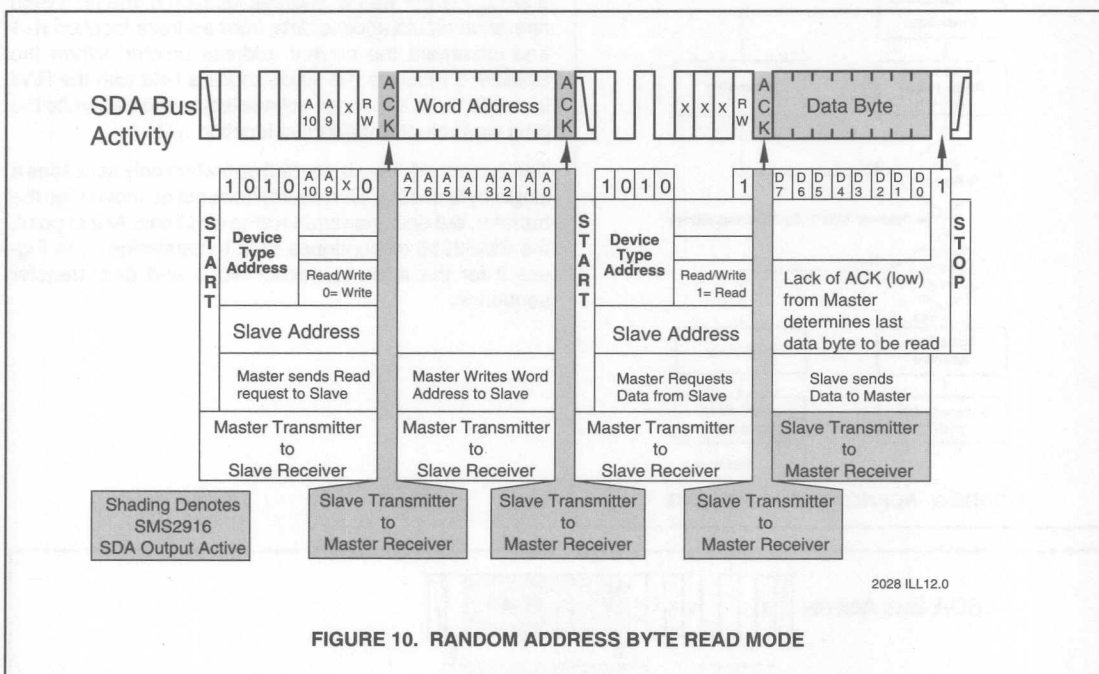
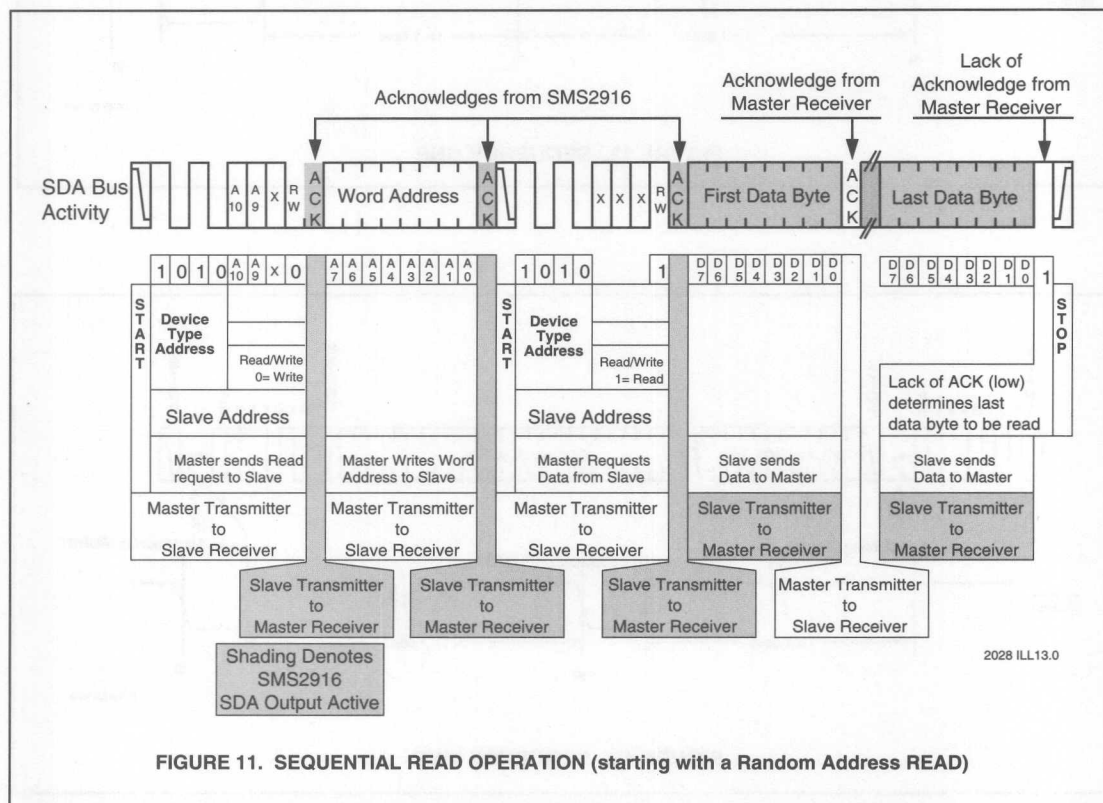


FIGURE 10. RANDOM ADDRESS BYTE READ MODE



Sequential READ

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 11 for the address, acknowledge and data transfer sequence.



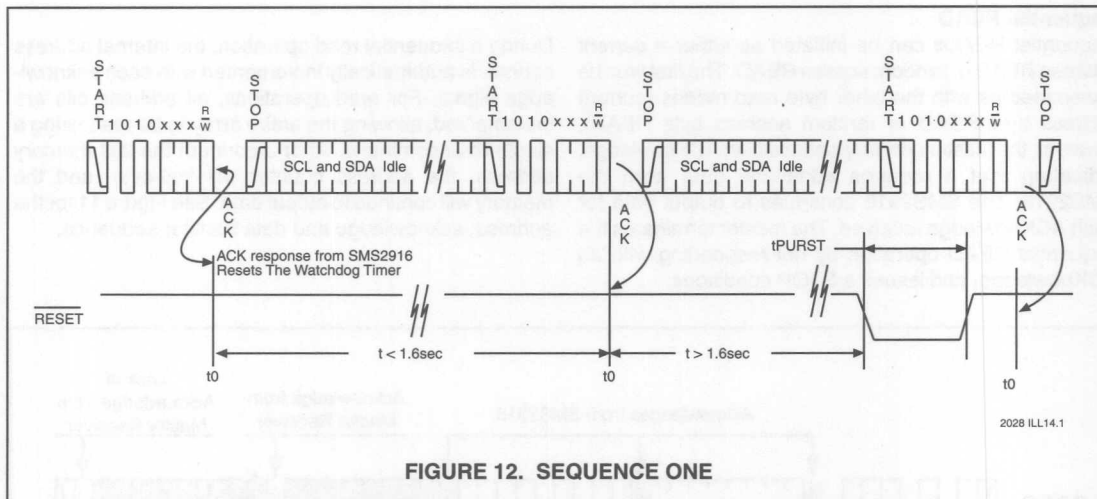


FIGURE 12. SEQUENCE ONE

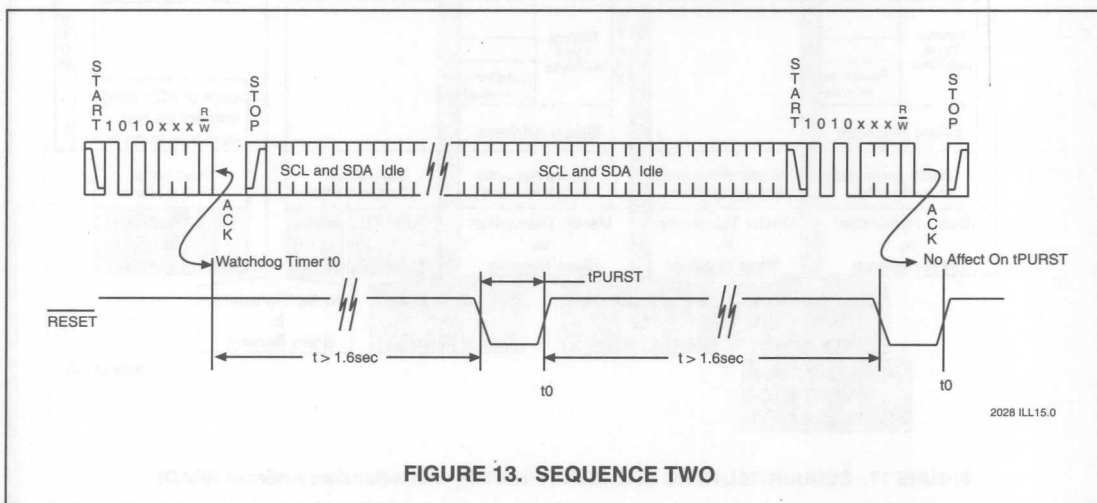


FIGURE 13. SEQUENCE TWO



SMS2916

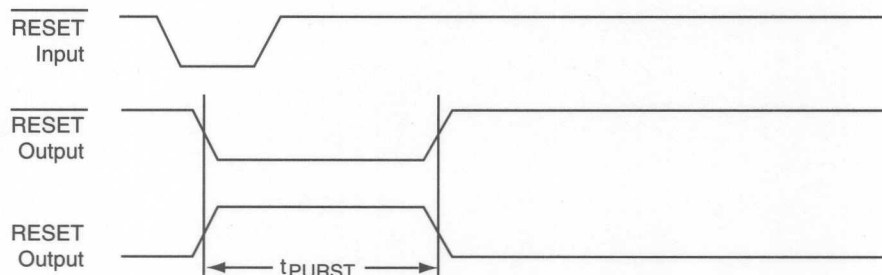
SMS2916

Preliminary



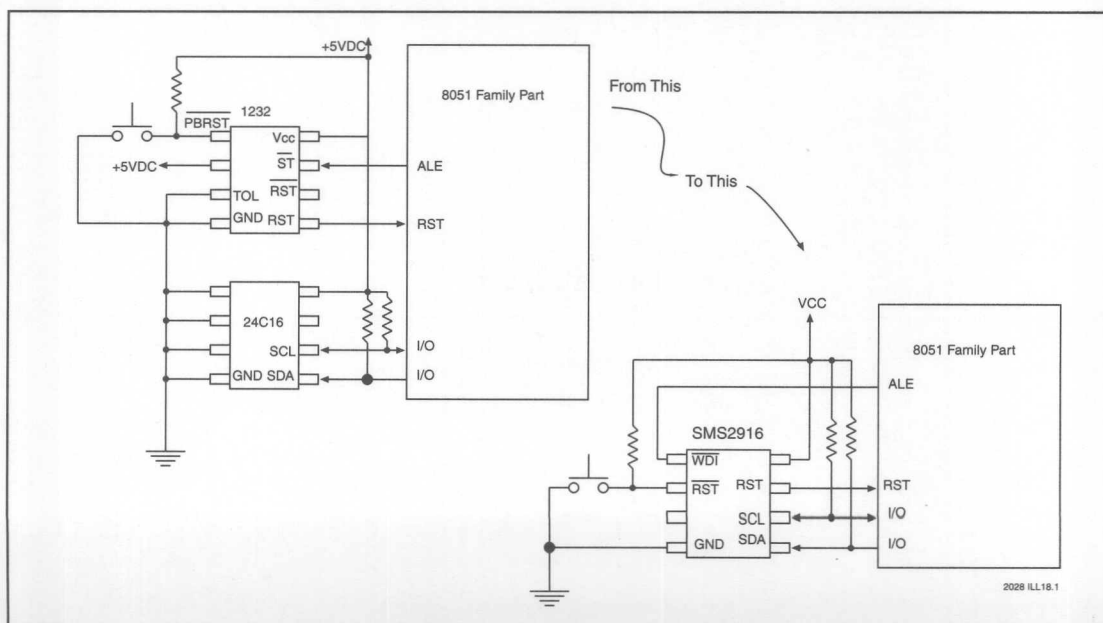
Frequently the supervisory circuit will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the SMS2916 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



2028 ILL16.0

If you happen to be using one of the more common supervisory circuits like a 1232, you might consider reducing your component count such as illustrated below.



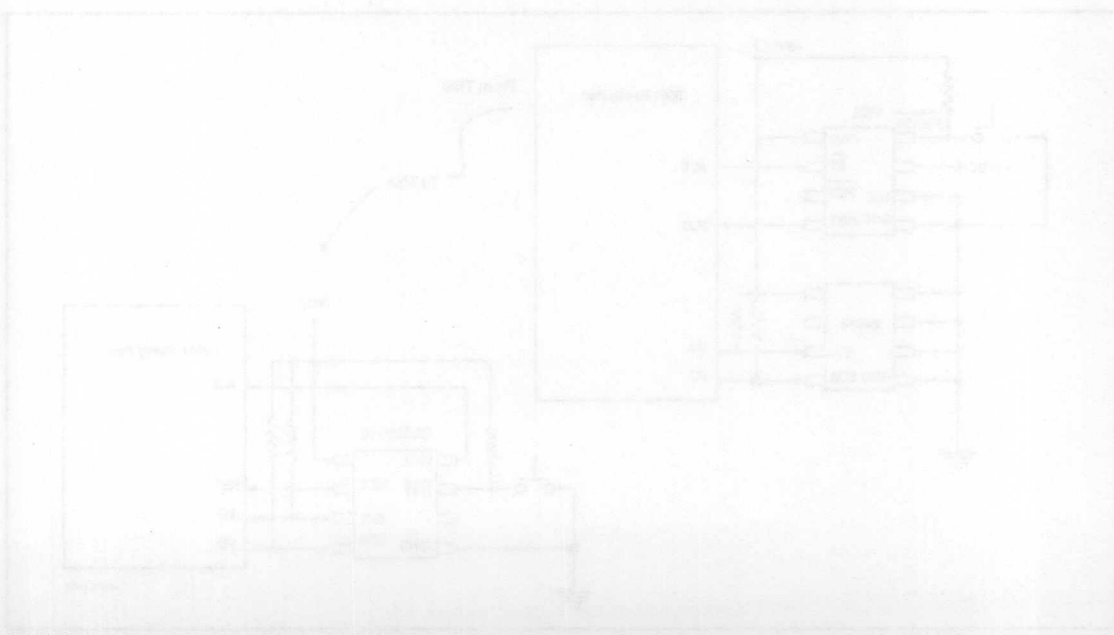
2028 ILL16.1



Figure 1 shows the typical output voltage regulation of the device. The output voltage is regulated to within 1% of the nominal value over the full range of input voltage and load current. The output voltage is also regulated to within 1% of the nominal value over the full range of input voltage and load current. The output voltage is also regulated to within 1% of the nominal value over the full range of input voltage and load current.



Figure 1. Typical output voltage regulation of the device. The output voltage is regulated to within 1% of the nominal value over the full range of input voltage and load current.





SECTION 4 **Precision Reset Controllers with a Microwire Nonvolatile Memory**

S93462	Dual Reset I/Os Plus 1K Memory in a x8 Data Configuration	4-3
S93463	Dual Reset I/Os Plus 1K Memory in a x16 Data Configuration	4-3
S93662	Dual Reset I/Os (Active High and Low) 4K Memory in a x8 Data Configuration ...	4-15
S93663	Dual Reset I/Os (Active High and Low) 4K Memory in a x16 Data Configuration .	4-15



Fixed-Point Controllers with a Micro-Processor Memory

SECTION

4-1	Fixed-Point Controllers with a Micro-Processor Memory
4-2	Fixed-Point Controllers with a Micro-Processor Memory
4-3	Fixed-Point Controllers with a Micro-Processor Memory
4-4	Fixed-Point Controllers with a Micro-Processor Memory
4-5	Fixed-Point Controllers with a Micro-Processor Memory

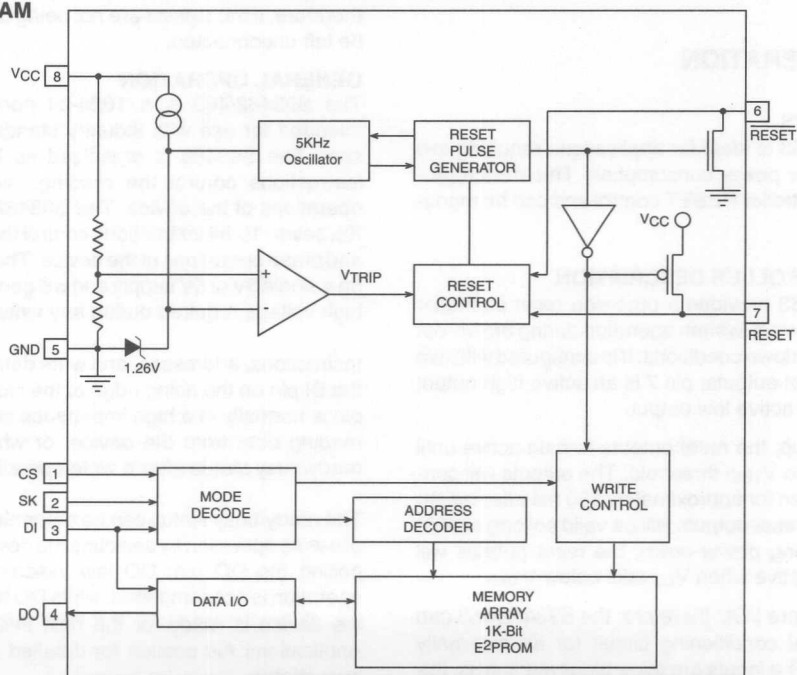
Precision Supply-Voltage Monitor and Reset Controller
FEATURES

- Precision Monitor & RESET Controller
 - RESET and RESET Outputs
 - Guaranteed RESET Assertion to $V_{CC} = 1V$
 - 150ms Reset Pulse Width
 - Internal 1.26V Reference with $\pm 1\%$ Accuracy
 - ZERO External Components Required
- Memory
 - 1K-bit Microwire Memory
 - S93462
 - Internally Ties ORG Low
 - 100% Compatible With all 8-bit Implementations
 - Sixteen Byte Page Write Capability
 - S93463
 - Internally Ties ORG High
 - 100% Compatible With all 16-bit Implementations
 - Eight Word Page Write Capability

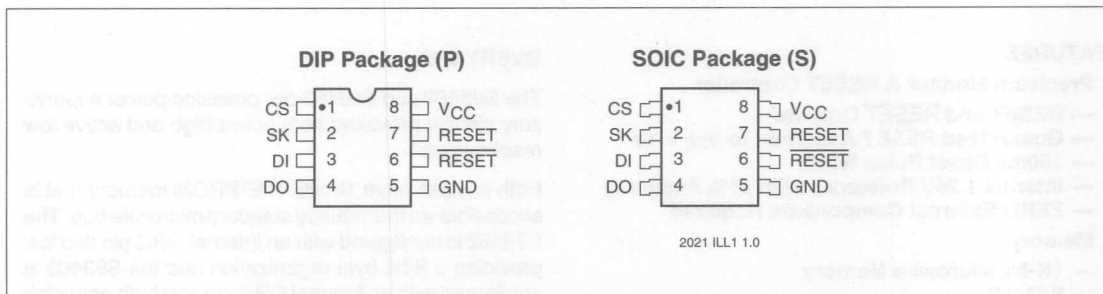
OVERVIEW

The S93462 and S93463 are precision power supervisory circuits providing both active high and active low reset outputs.

Both devices have 1k-bits of E²PROM memory that is accessible via the industry standard microwire bus. The S93462 is configured with an internal ORG pin tied low providing a 8-bit byte organization and the S93463 is configured with an internal ORG pin tied high providing a 16-bit word organization. Both the S93462 and S93463 have page write capability. The devices are designed for a minimum 1,000,000 program/erase cycles and have data retention in excess of 100 years.

BLOCK DIAGRAM


2021 ILL2 1.0

**PIN CONFIGURATION****PIN FUNCTIONS**

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V _{CC}	+2.7 to 6.0V Power Supply
GND	Ground
RESET/ $\overline{\text{RESET}}$	RESET I/O

a low to high transition and the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a debounce/reset extender circuit.

It should be noted the reset outputs are open drain. When used as outputs driving a circuit they need to be either tied high ($\overline{\text{RESET}}$) or tied to ground (RESET) through the use of pull-up or pull-down resistors. Refer to the applications aid section for help in determining the value of resistor to be used. Internally these pins are weakly pulled up ($\overline{\text{RESET}}$) and pulled down (RESET); therefore, if the signals are not being used the pins may be left unconnected.

DEVICE OPERATION**APPLICATIONS**

The S93462/463 is ideal for applications requiring low voltage and low power consumption. This device provides microcontroller RESET control and can be manually resettable.

RESET CONTROLLER DESCRIPTION

The S93462/463 provides a precision reset controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain reset outputs; pin 7 is an active high output and pin 6 is an active low output.

During power-up, the reset outputs remain active until V_{CC} reaches the V_{TRIP} threshold. The outputs will continue to be driven for approximately 150 ms after reaching V_{TRIP}. The reset outputs will be valid so long as V_{CC} is $\geq 1.0\text{V}$. During power-down, the reset outputs will begin driving active when V_{CC} falls below V_{TRIP}.

The reset pins are I/Os; therefore, the S93462/463 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting

GENERAL OPERATION

The S93462/463 is a 1024-bit nonvolatile memory intended for use with industry standard microprocessors. The S93463 is organized as X16, seven 9-bit instructions control the reading, writing and erase operations of the device. The S93462 is organized as X8, seven 10-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. See the Applications Aid section for detailed use of the ready busy status.



The format for all instructions is: one start bit; two op code bits and either six (x16) or seven (x8) address or instruction bits.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the S93462/463 will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start automatic erase and write cycle to the memory location specified in the instruction. The ready/busy status of the S93462/463 can be determined by selecting the device and polling the DO pin.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status of the S93462/463 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

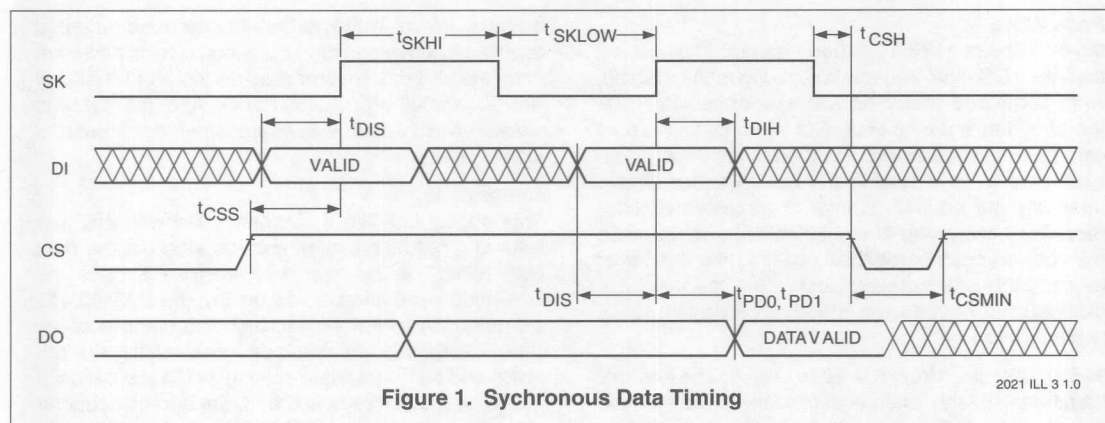


Figure 1. Synchronous Data Timing

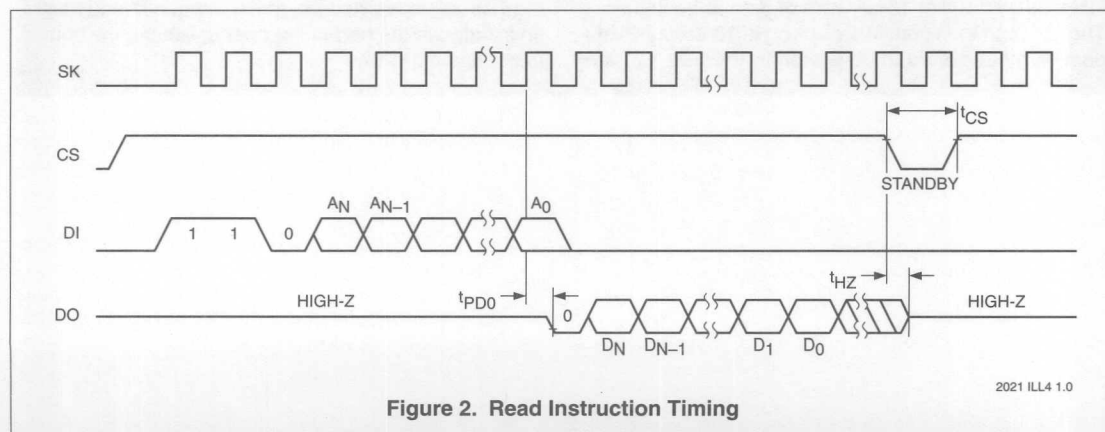


Figure 2. Read Instruction Timing



Erase/Write Enable and Disable

The S93462/463 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all S93462/463 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The

clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93462/463 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits will be in a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93462/463 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Page Write

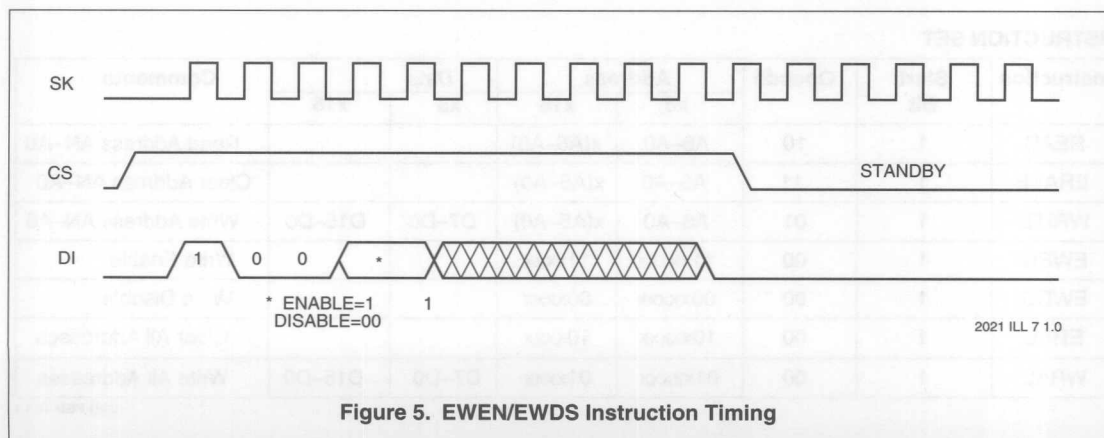
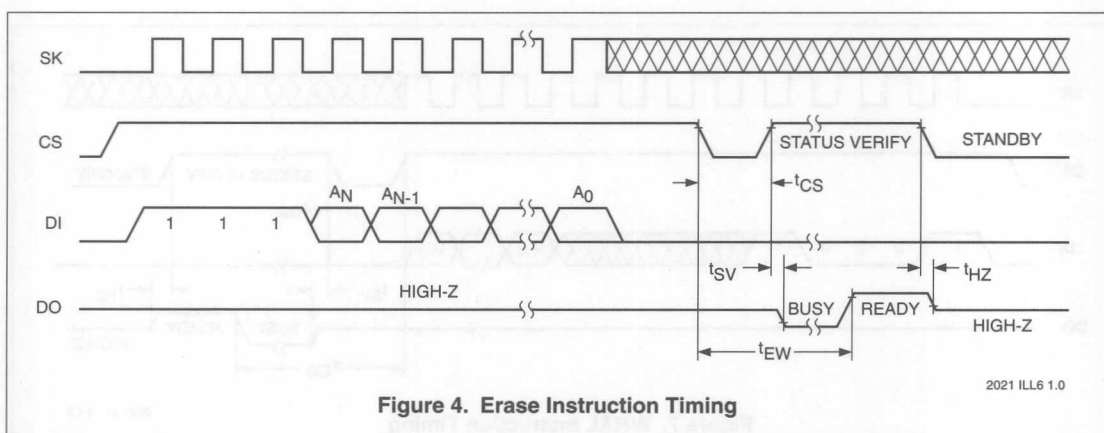
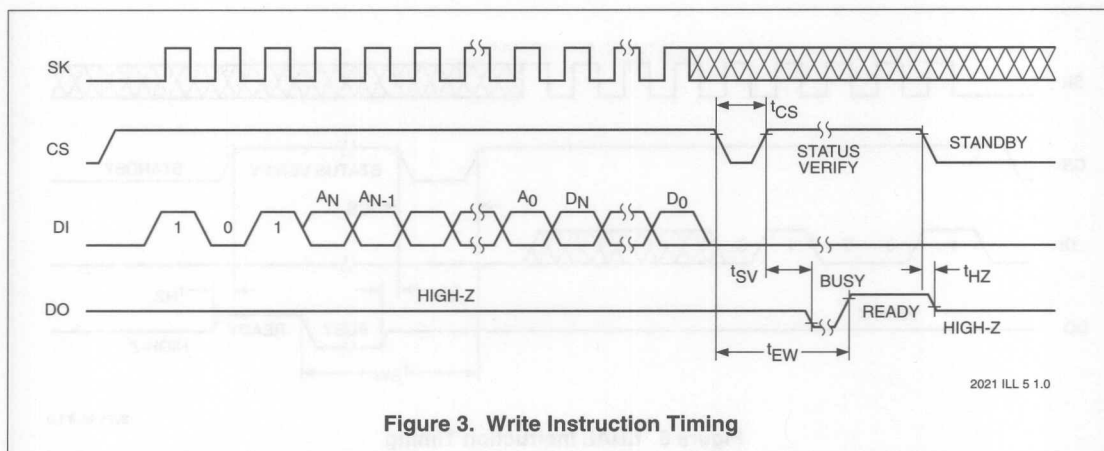
93462 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 7-bit address immediately followed by the first byte of data to be written. The host can then continue clocking in 8-bit bytes of data with each byte to be written to the next higher address. Internally the address pointer is incremented after receiving each group of eight clocks; however, once the address counter reaches xxx 1111 it will roll over to xxx 0000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

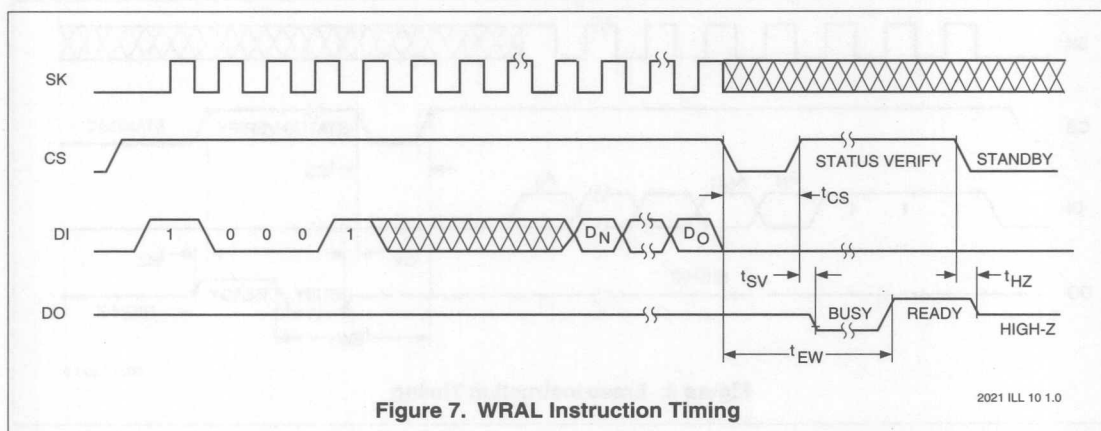
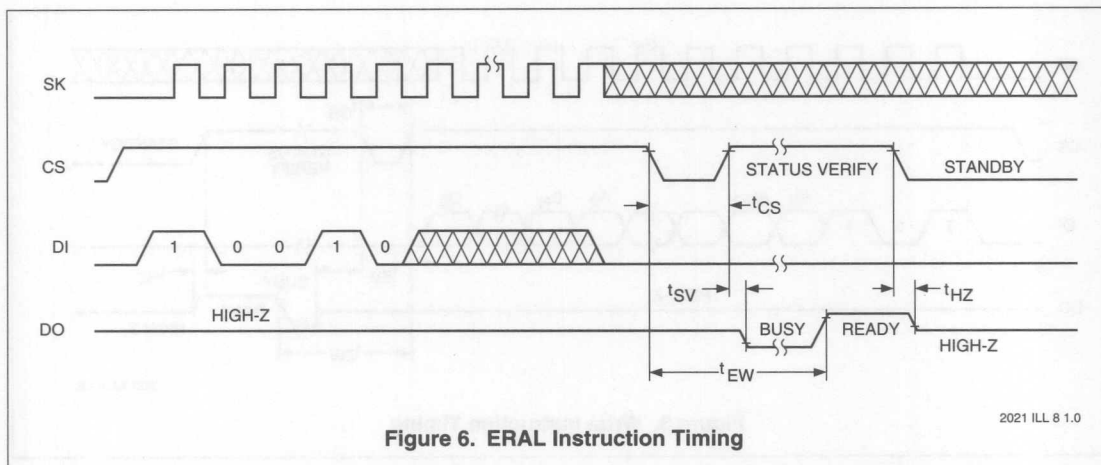
93463 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 6-bit address immediately followed by the first 16-bit word of data to be written. The host can then continue clocking in 16-bit words of data with each word to be written to the next higher

address. Internally the address pointer is incremented after receiving each group of sixteen clocks; however, once the address counter reaches xxx x111 it will roll over to xx x000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

Continuous Read

This begins just like a standard read with the host issuing a read instruction and clocking out the data byte [word]. If the host then keeps CS high and continues generating clocks on SK, the S93462/463 will output data from the next higher address location. The S93462/463 will continue incrementing the address and outputting data so long as CS stays high. If the highest address is reached, the address counter will roll over to address 0000. CS going low will reset the instruction register and any subsequent read must be initiated in the normal manner of issuing the command and address.





INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A6-A0	x(A5-A0)			Read Address AN-A0
ERASE	1	11	A6-A0	x(A5-A0)			Clear Address AN-A0
WRITE	1	01	A6-A0	x(A5-A0)	D7-D0	D15-D0	Write Address AN-A0
EWEN	1	00	11xxxx	11xxx			Write Enable
EWDS	1	00	00xxxx	00xxx			Write Disable
ERAL	1	00	10xxxx	10xxx			Clear All Addresses
WRAL	1	00	01xxxx	01xxx	D7-D0	D15-D0	Write All Addresses

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**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground ⁽¹⁾	-2.0V to +V _{CC} +2.0V
V _{CC} with Respect to Ground	-2.0V to +7.0V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽²⁾	100 mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N _{END} ⁽³⁾	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T _{DR} ⁽³⁾	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V _{ZAP} ⁽³⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I _{LTH} ⁽³⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

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D.C. OPERATING CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I _{CC}	Power Supply Current (Operating)			3	mA	DI = 0.0V, f _{SK} = 1MHz V _{CC} = 5.0V, CS = 5.0V, Output Open
I _{SB}	Power Supply Current (Standby)			50	μA	CS = 0V Reset Outputs Open
I _{LI}	Input Leakage Current			2	μA	V _{IN} = 0V to V _{CC}
I _{LO}	Output Leakage Current (Including ORG pin)			10	μA	V _{OUT} = 0V to V _{CC} , CS = 0V
V _{IL1}	Input Low Voltage	-0.1		0.8	V	4.5V ≤ V _{CC} < 5.5V
V _{IH1}	Input High Voltage	2		V _{CC} +1	V	
V _{IL2}	Input Low Voltage	0		V _{CC} X0.2	V	1.8V ≤ V _{CC} < 2.7V
V _{IH2}	Input High Voltage	V _{CC} X0.7		V _{CC} +1	V	
V _{OL1}	Output Low Voltage			0.4	V	4.5V ≤ V _{CC} < 5.5V I _{OL} = 2.1mA I _{OH} = -400μA
V _{OH1}	Output High Voltage	2.4			V	
V _{OL2}	Output Low Voltage			0.2	V	1.8V ≤ V _{CC} < 2.7V I _{OL} = 1mA I _{OH} = -100μA
V _{OH2}	Output High Voltage	V _{CC} -0.2			V	

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Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.

2021-03 5/3/98

**PIN CAPACITANCE**

Symbol	Test	Max.	Units	Conditions
C _{OUT} ⁽¹⁾	OUTPUT CAPACITANCE (DO)	5	pF	V _{OUT} =OV
C _{IN} ⁽¹⁾	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V _{IN} =OV

Note:

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(1) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

SYMBOL	PARAMETER	Limits				UNITS	Test Conditions
		V _{CC} =2.7V-4.5V		V _{CC} =4.5V-5.5V			
		Min.	Max.	Min.	Max.		
t _{CSS}	CS Setup Time	100		50		ns	C _L = 100pF
t _{CSH}	CS Hold Time	0		0		ns	
t _{DIS}	DI Setup Time	200		100		ns	
t _{DIH}	DI Hold Time	200		100		ns	
t _{PD1}	Output Delay to 1		0.5		0.25	μs	
t _{PD0}	Output Delay to 0		0.5		0.25	μs	
t _{HZ} ⁽¹⁾	Output Delay to High-Z		200		100	ns	
t _{EW}	Program/Erase Pulse Width		10		10	ms	
t _{CSMIN}	Minimum CS Low Time	0.5		0.25		μs	
t _{SKHI}	Minimum SK High Time	0.5		0.25		μs	
t _{SKLOW}	Minimum SK Low Time	0.5		0.25		μs	
t _{SV}	Output Delay to Status Valid		0.5		0.25	μs	
SK _{MAX}	Maximum Clock Frequency	DC	500	DC	1000	KHZ	

Note:

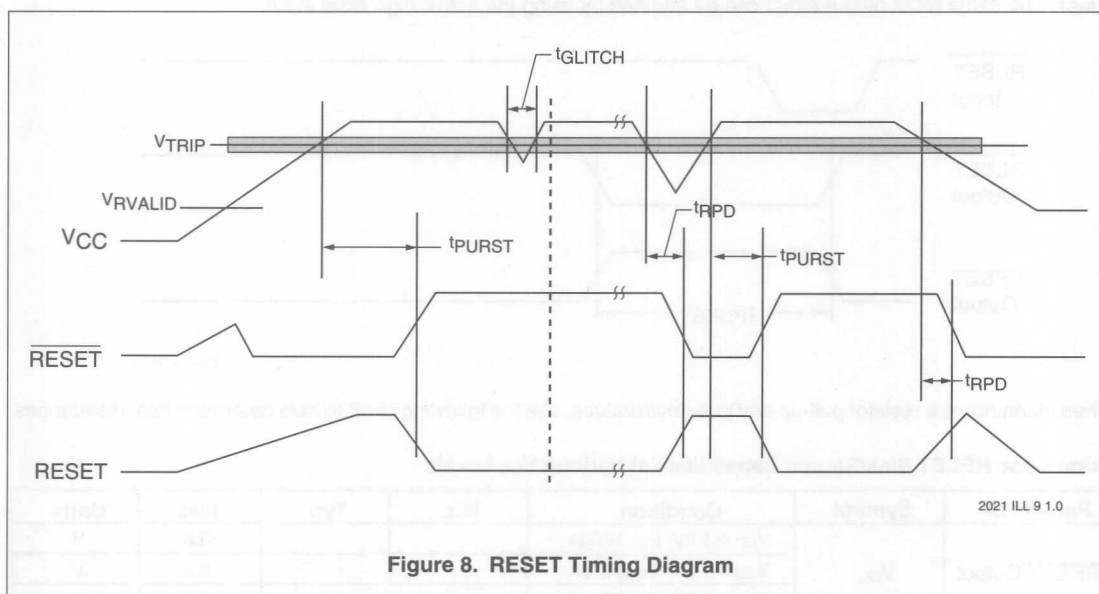
2021 PGM T6 1.0

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	2.7		5 Volt-A		5 Volt-B		Unit
		Min	Max	Min	Max	Min	Max	
V _{TRIP}	Reset Trip Point	2.55	2.7	4.25	4.5	4.50	4.75	V
t _{PURST}	Power-Up Reset Timeout	130	270	130	270	130	270	ms
t _{RPD}	V _{TRIP} to RESET Output Delay		5		5		5	μs
V _{RVALID}	RESET Output Valid	1		1		1		V
t _{GLITCH}	Glitch Reject Pulse Width		30		30		30	ns
V _{OLRS}	RESET Output Low Voltage I _{OL} =1mA		0.4		0.4		0.4	V
V _{OHRS}	RESET Output High I _{OH}	V _{CC} -75		V _{CC} -75		V _{CC} -75		V

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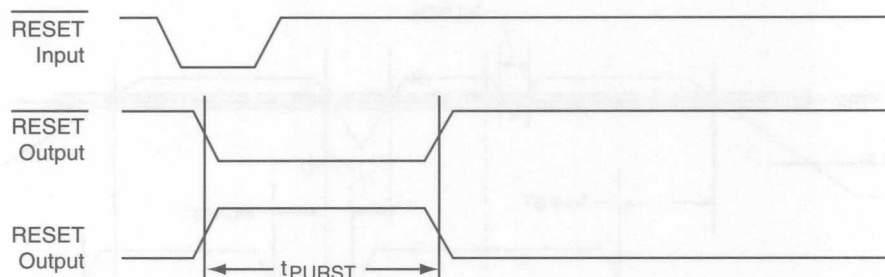
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Figure 8. RESET Timing Diagram



Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S93462/463 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



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When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL} = 100\mu A$			0.3	V
		$V_{CC} = 1.2V, I_{OL} = 100\mu A$			0.3	V
		$V_{CC} = 3.0V, I_{OL} = 500\mu A$			0.3	V
		$V_{CC} = 3.6V, I_{OL} = 500\mu A$			0.3	V
		$V_{CC} = 4.5V, I_{OL} = 750\mu A$			0.3	V
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL} = 100\mu A$			0.4	V
		$V_{CC} = 1.2V, I_{OL} = 150\mu A$			0.4	V
		$V_{CC} = 3.0V, I_{OL} = 750\mu A$			0.4	V
		$V_{CC} = 3.6V, I_{OL} = 1mA$			0.4	V
		$V_{CC} = 4.5V, I_{OL} = 1mA$			0.4	V
RESET Output Voltage	V_{OH}	$V_{CC} = 1.0V, I_{OH} = 400\mu A$	$V_{CC} - 0.75$			V
		$V_{CC} = 1.2V, I_{OH} = 800\mu A$	$V_{CC} - 0.75$			V
		$V_{CC} = 3.0V, I_{OH} = 800\mu A$	$V_{CC} - 0.5$			V
		$V_{CC} = 3.6V, I_{OH} = 800\mu A$	$V_{CC} - 0.5$			V
		$V_{CC} = 4.5V, I_{OH} = 800\mu A$	$V_{CC} - 0.5$			V

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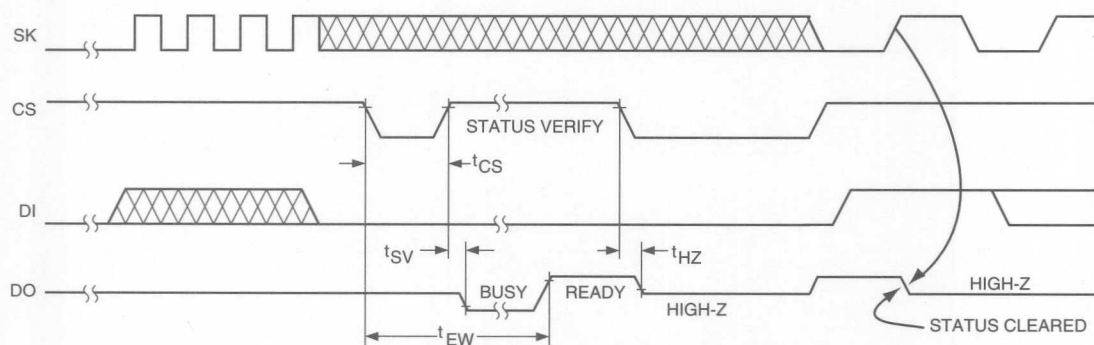


Ready/Busy Status

During the internal write operation the S93462/463 memory array is inaccessible. After starting the write operation (taking CS low) the host can implement a 10ms timeout routine or alternatively it can employ a polling routine that tests the state of the DO pin.

After starting the write, testing for the status is easily accomplished by taking CS high and testing the state of DO. If it is low the device is still busy with the internal write. If it is high the write operation has completed.

For the polling routine the host has the option of toggling CS for each test of DO, or it can place CS high and then intermittently test DO. SK is not required for any of these operations. Once the device is ready, it will continue to drive DO high whenever the S93462/463 is selected. The ready state of DO can be cleared by clocking in a start bit; this start bit can either be the beginning of a new command sequence or it can be a dummy start bit with CS returning low before the host issues a new command.



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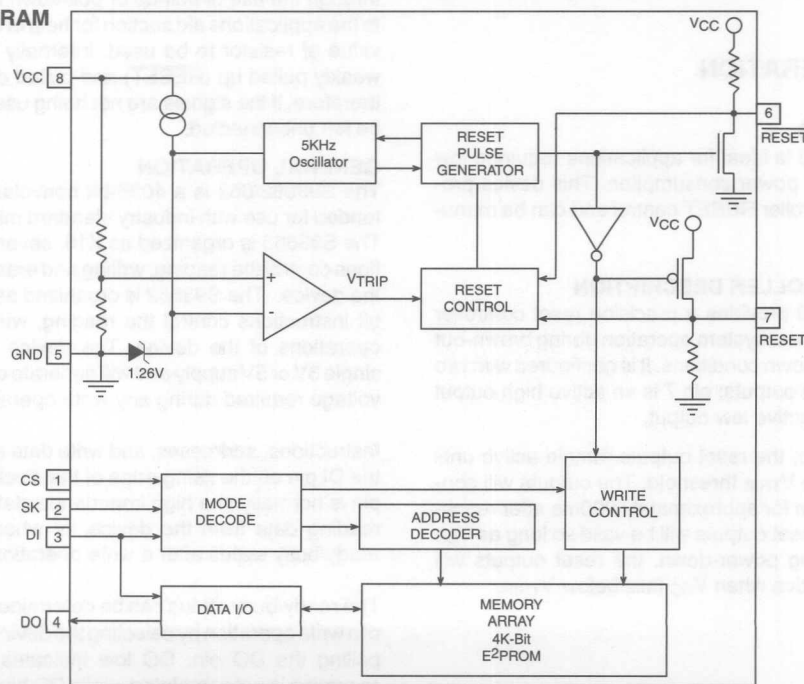
Precision Supply-Voltage Monitor and Reset Controller
FEATURES

- **Precision Monitor & RESET Controller**
 - RESET and RESET Outputs
 - Guaranteed RESET Assertion to $V_{CC} = 1V$
 - 200ms Reset Pulse Width
 - Internal 1.26V Reference with $\pm 1\%$ Accuracy
 - ZERO External Components Required
- **Memory**
 - 4K-bit Microwire Memory
 - S93662
 - Internally Ties ORG Low
 - 100% Compatible With all 8-bit Implementations
 - Sixteen Byte Page Write Capability
 - S93663
 - Internally Ties ORG High
 - 100% Compatible With all 16-bit Implementations
 - Eight Word Page Write Capability

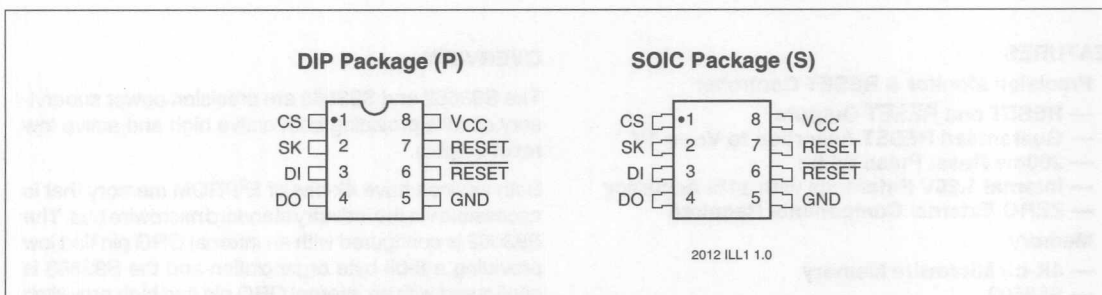
OVERVIEW

The S93662 and S93663 are precision power supervisory circuits providing both active high and active low reset outputs.

Both devices have 4k-bits of E²PROM memory that is accessible via the industry standard microwire bus. The S93662 is configured with an internal ORG pin tied low providing a 8-bit byte organization and the S93663 is configured with an internal ORG pin tied high providing a 16-bit word organization. Both the S93662 and S93663 have page write capability. The devices are designed for a minimum 1,000,000 program/erase cycles and have data retention in excess of 100 years.

BLOCK DIAGRAM


2012 ILL2 1.0

**PIN CONFIGURATION****PIN FUNCTIONS**

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V _{CC}	+2.7 to 6.0V Power Supply
GND	Ground
RESET/RESET	RESET I/O

DEVICE OPERATION**APPLICATIONS**

The S93662/663 is ideal for applications requiring low voltage and low power consumption. This device provides microcontroller RESET control and can be manually resettable.

RESET CONTROLLER DESCRIPTION

The S93662/663 provides a precision reset controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain reset outputs; pin 7 is an active high output and pin 6 is an active low output.

During power-up, the reset outputs remain active until V_{CC} reaches the V_{TRIP} threshold. The outputs will continue to be driven for approximately 200ms after reaching V_{TRIP}. The reset outputs will be valid so long as V_{CC} is $\geq 1.0V$. During power-down, the reset outputs will begin driving active when V_{CC} falls below V_{TRIP}.

The reset pins are I/Os; therefore, the S93662/663 can act as a stabilization circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a debounce/reset extender circuit.

It should be noted the reset outputs are open drain. When used as outputs driving a circuit they need to be either tied high ($\overline{\text{RESET}}$) or tied to ground (RESET) through the use of pull-up or pull-down resistors. Refer to the applications aid section for help in determining the value of resistor to be used. Internally these pins are weakly pulled up ($\overline{\text{RESET}}$) and pulled down (RESET); therefore, if the signals are not being used the pins may be left unconnected.

GENERAL OPERATION

The S93662/663 is a 4096-bit nonvolatile memory intended for use with industry standard microprocessors. The S93663 is organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. The S93662 is organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that



the device is ready for the next instruction. See the Applications Aid section for detailed use of the ready/busy status.

The format for all instructions is: one start bit; two op code bits and either eight (x16) or nine (x8) address or instruction bits.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the S93662/663 will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start automatic erase and write cycle to the memory location specified in the instruction. The ready/busy status of the S93662/663 can be determined by selecting the device and polling the DO pin.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status of the S93662/663 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

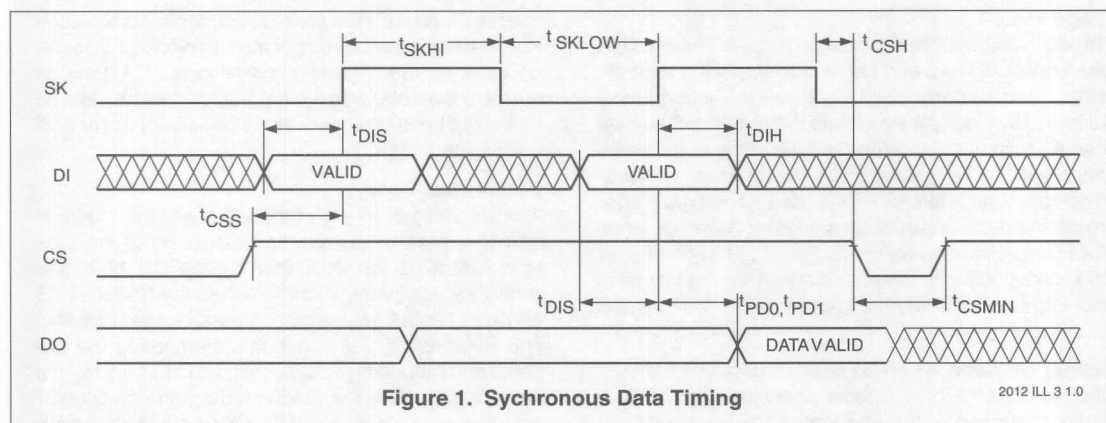


Figure 1. Synchronous Data Timing

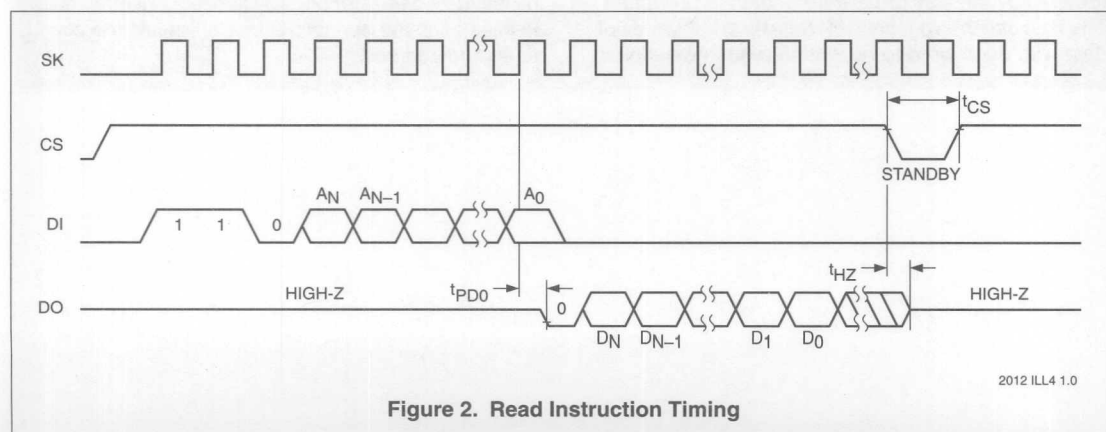


Figure 2. Read Instruction Timing

**Erase/Write Enable and Disable**

The S93662/663 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all S93662/663 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The

clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93662/663 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93662/663 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Page Write

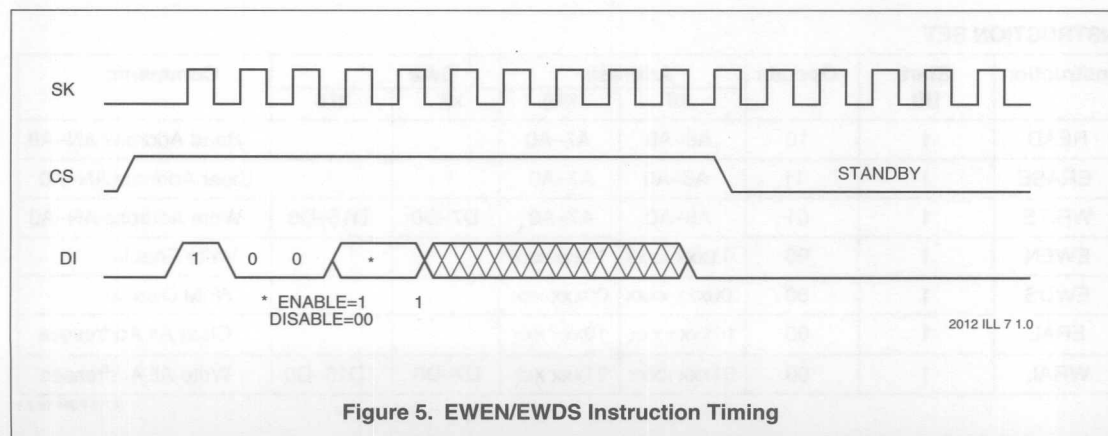
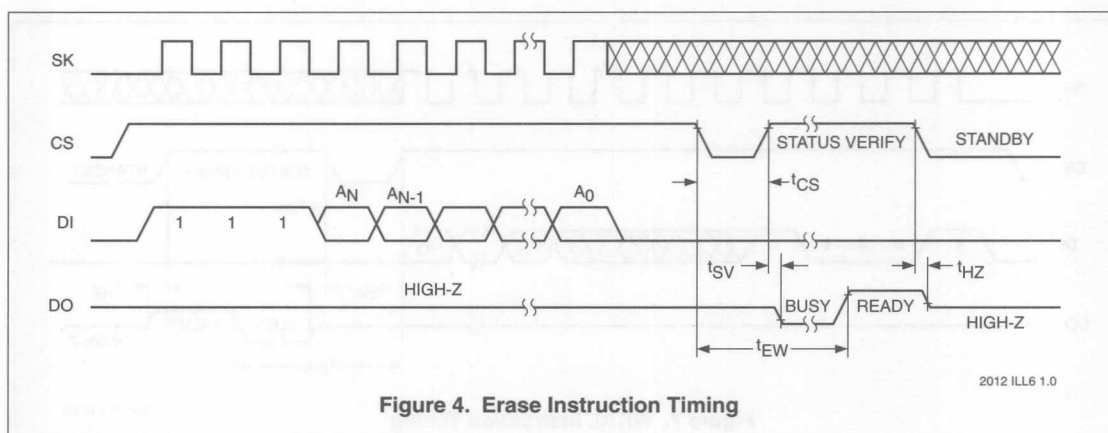
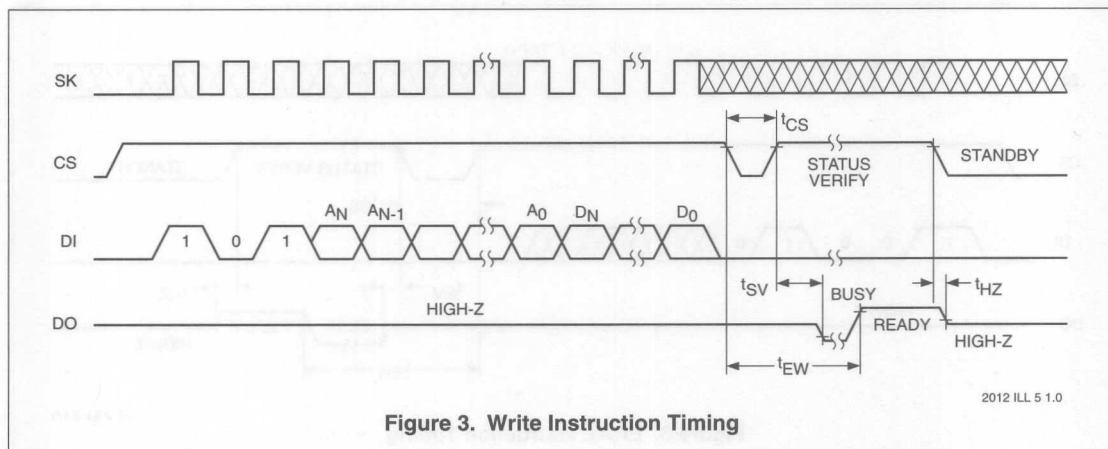
93662 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 9-bit byte address immediately followed by the first byte of data to be written. The host can then continue clocking in 8-bit bytes of data with each byte to be written to the next higher address. Internally the address pointer is incremented after receiving each group of eight clocks; however, once the address counter reaches x xxx 1111 it will roll over to x xxx 0000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

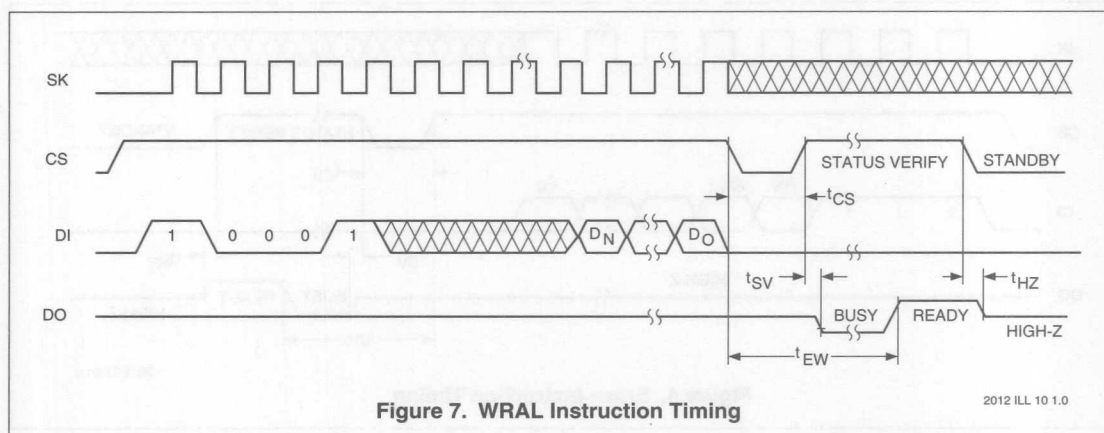
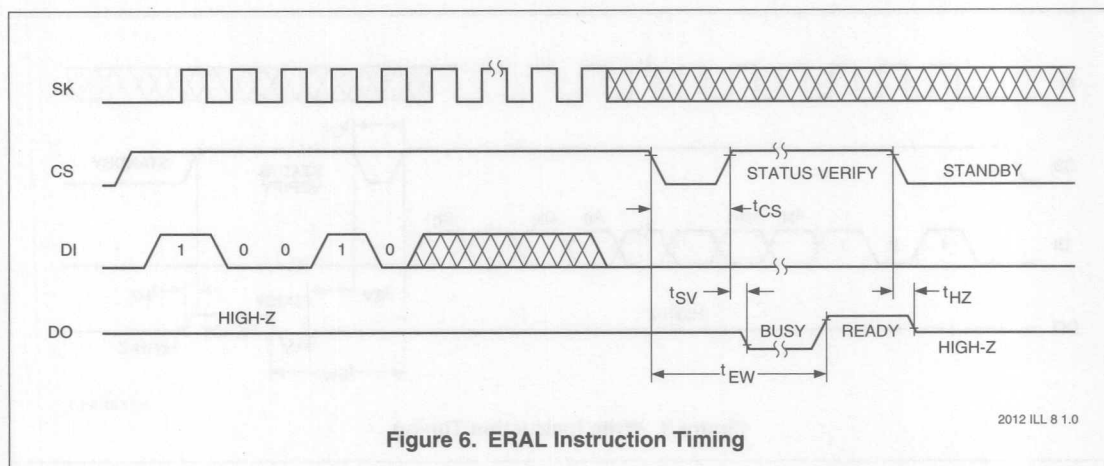
93663 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 8-bit byte address immediately followed by the first 16-bit word of data to be written. The host can then continue clocking in 16-bit words of data with each word to be written to the next higher

address. Internally the address pointer is incremented after receiving each group of sixteen clocks; however, once the address counter reaches xxx x111 it will roll over to xxx x000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

Continuous Read

This begins just like a standard read with the host issuing a read instruction and clocking out the data byte [word]. If the host then keeps CS high and continues generating clocks on SK, the S93662/663 will output data from the next higher address location. The S93662/663 will continue incrementing the address and outputting data so long as CS stays high. If the highest address is reached, the address counter will roll over to address 0000. CS going low will reset the instruction register and any subsequent read must be initiated in the normal manner of issuing the command and address.





INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A8-A0	A7-A0			Read Address AN-A0
ERASE	1	11	A8-A0	A7-A0			Clear Address AN-A0
WRITE	1	01	A8-A0	A7-A0	D7-D0	D15-D0	Write Address AN-A0
EWEN	1	00	11xxx xxxx	11xxx xxx			Write Enable
EWDS	1	00	00xxx xxxx	00xxx xxx			Write Disable
ERAL	1	00	10xxx xxxx	10xxx xxx			Clear All Addresses
WRAL	1	00	01xxx xxxx	01xxx xxx	D7-D0	D15-D0	Write All Addresses

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**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground ⁽¹⁾	-2.0V to +V _{CC} +2.0V
V _{CC} with Respect to Ground	-2.0V to +7.0V
Package Power Dissipation Capability (T _a = 25°C)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽²⁾	100 mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N _{END} ⁽³⁾	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T _{DR} ⁽³⁾	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V _{ZAP} ⁽³⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I _{LTH} ⁽³⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

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D.C. OPERATING CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I _{CC}	Power Supply Current (Operating)			3	mA	DI = 0.0V, f _{SK} = 1MHz V _{CC} = 5.0V, CS = 5.0V, Output Open
I _{SB}	Power Supply Current (Standby)			50	μA	CS = 0V Reset Outputs Open
I _{LI}	Input Leakage Current			2	μA	V _{IN} = 0V to V _{CC}
I _{LO}	Output Leakage Current (Including ORG pin)			10	μA	V _{OUT} = 0V to V _{CC} , CS = 0V
V _{IL1} V _{IH1}	Input Low Voltage Input High Voltage	-0.1 2		0.8 V _{CC} +1	V V	4.5V ≤ V _{CC} ≤ 5.5V
V _{IL2} V _{IH2}	Input Low Voltage Input High Voltage	0 V _{CC} X0.7		V _{CC} X0.2 V _{CC} +1	V V	1.8V ≤ V _{CC} < 2.7V
V _{OL1} V _{OH1}	Output Low Voltage Output High Voltage	2.4		0.4	V V	4.5V ≤ V _{CC} ≤ 5.5V I _{OL} = 2.1mA I _{OH} = -400μA
V _{OL2} V _{OH2}	Output Low Voltage Output High Voltage	V _{CC} -0.2		0.2	V V	1.8V ≤ V _{CC} < 2.7V I _{OL} = 1mA I _{OH} = -100μA

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Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.

**PIN CAPACITANCE**

Symbol	Test	Max.	Units	Conditions
C _{OUT} ⁽¹⁾	OUTPUT CAPACITANCE (DO)	5	pF	V _{OUT} =OV
C _{IN} ⁽¹⁾	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V _{IN} =OV

Note:

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(1) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

SYMBOL	PARAMETER	Limits				UNITS	Test Conditions
		V _{CC} =2.7V-4.5V		V _{CC} =4.5V-5.5V			
		Min.	Max.	Min.	Max.		
t _{CSS}	CS Setup Time	100		50		ns	C _L = 100pF
t _{CSH}	CS Hold Time	0		0		ns	
t _{DIS}	DI Setup Time	200		100		ns	
t _{DIH}	DI Hold Time	200		100		ns	
t _{PD1}	Output Delay to 1		0.5		0.25	μs	
t _{PD0}	Output Delay to 0		0.5		0.25	μs	
t _{HZ} ⁽¹⁾	Output Delay to High-Z		200		100	ns	
t _{EW}	Program/Erase Pulse Width		10		10	ms	
t _{CSMIN}	Minimum CS Low Time	0.5		0.25		μs	
t _{SKHI}	Minimum SK High Time	0.5		0.25		μs	
t _{SKLOW}	Minimum SK Low Time	0.5		0.25		μs	
t _{SV}	Output Delay to Status Valid		0.5		0.25	μs	
SK _{MAX}	Maximum Clock Frequency	DC	500	DC	1000	KHZ	

Note:

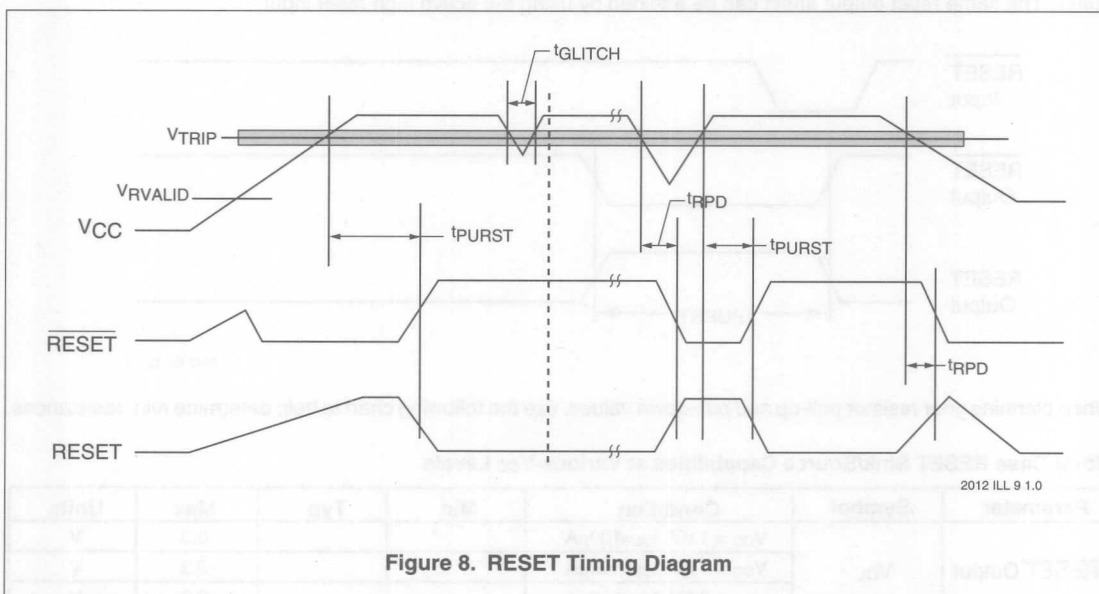
2012 PGM T6 1.0

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	2.7		5 Volt-A		5 Volt-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.50	4.75	V
tPURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
trPD	VTRIP to RESET Output Delay		5		5		5	μ s
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage $I_{OL}=1mA$		0.4		0.4		0.4	V
VOHRS	RESET Output High I_{OH}	$V_{CC}-0.75$		$V_{CC}-0.75$		$V_{CC}-0.75$		V

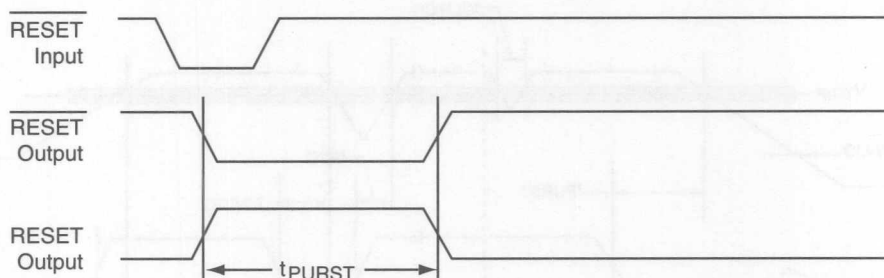
2012 PGM T1 1.1





Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S93662/663 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



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When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 1.2V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 3.0V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 3.6V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 4.5V, I_{OL}=750\mu A$			0.3	V
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.4	V
		$V_{CC} = 1.2V, I_{OL}=150\mu A$			0.4	V
		$V_{CC} = 3.0V, I_{OL}=750\mu A$			0.4	V
		$V_{CC} = 3.6V, I_{OL}=1mA$			0.4	V
		$V_{CC} = 4.5V, I_{OL}=1mA$			0.4	V
RESET Output Voltage	V_{OH}	$V_{CC} = 1.0V, I_{OH}=400\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 1.2V, I_{OH}=800\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 3.0V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 3.6V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 4.5V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V

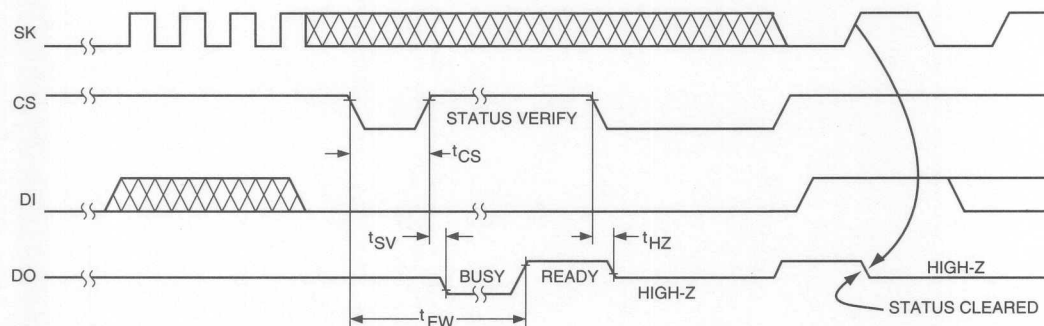
2012 PGM T5 1.0

**Ready/Busy Status**

During the internal write operation the S93662/663 memory array is inaccessible. After starting the write operation (taking CS low) the host can implement a 10ms timeout routine or alternatively it can employ a polling routine that tests the state of the DO pin.

After starting the write, testing for the status is easily accomplished by taking CS high and testing the state of DO. If it is low the device is still busy with the internal write. If it is high the write operation has completed.

For the polling routine the host has the option of toggling CS for each test of DO, or it can place CS high and then intermittently test DO. SK is not required for any of these operations. Once the device is ready, it will continue to drive DO high whenever the S93662/663 is selected. The ready state of DO can be cleared by clocking in a start bit; this start bit can either be the beginning of a new command sequence or it can be a dummy start bit with CS returning low before the host issues a new command.



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SECTION 5 **Precision Reset Controller with a Watchdog Timer and a Microwire Nonvolatile Memory**

S93WD462	Dual Reset I/Os Watchdog Timer Plus 1K Memory in a x8 Data Configuration	5-3
S93WD463	Dual Reset I/Os Watchdog Timer Plus 1K Memory in a x16 Data Configuration	5-3
S93WD662	Dual Reset I/Os (Active High and Low) Watchdog Timer and 4K Memory in a x8 Data Configuration	5-15
S93WD663	Dual Reset I/Os (Active High and Low) Watchdog Timer and 4K Memory in a x16 Data Configuration	5-15



SECTION 1 Predictive Model Output with a Histogram Filter and a Sigmoid Transfer Function

The model output is a vector of predicted values for each input variable. The output is calculated by applying a sigmoid transfer function to the weighted sum of the input variables. The output is then passed through a histogram filter to produce the final predicted values. The histogram filter is used to smooth the output and to remove any outliers. The final predicted values are then used to calculate the model's performance metrics.

**Precision Supply-Voltage Monitor and Reset Controller
With a Watchdog Timer and 1k-bit Microwire Memory**

FEATURES

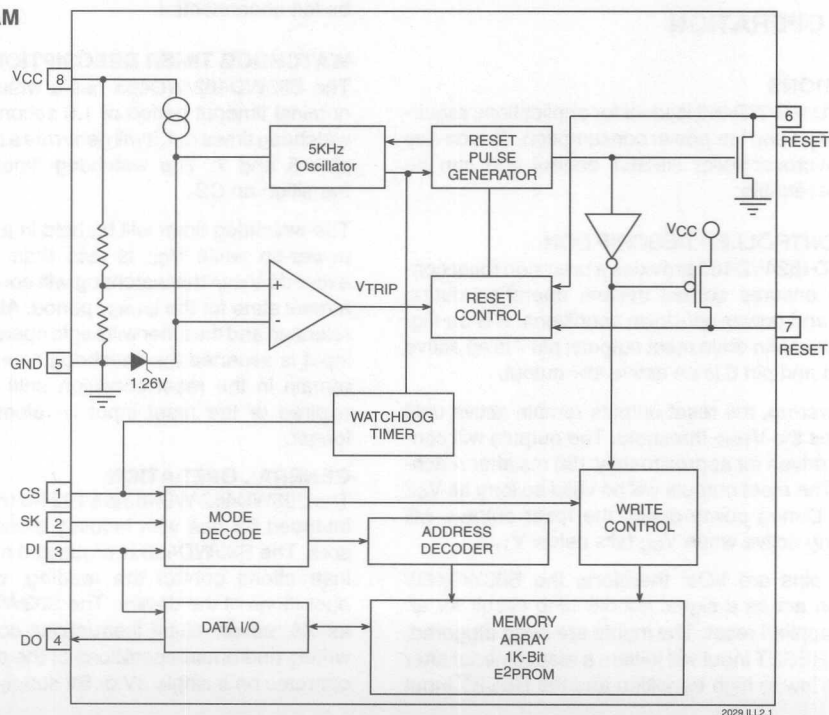
- Precision Monitor & RESET Controller
 - RESET and $\overline{\text{RESET}}$ Outputs
 - Guaranteed RESET Assertion to $V_{CC} = 1V$
 - 150ms Reset Pulse Width
 - Internal 1.26V Reference with $\pm 1\%$ Accuracy
 - ZERO External Components Required
- Watchdog Timer
 - Nominal 1.6 Second Timeout Period
 - Reset by Any Transition of CS
- Memory
 - 1K-bit Microwire Memory
 - S93WD462
 - Internally Ties ORG Low
 - 100% Compatible With all 8-bit Implementations
 - Sixteen Byte Page Write Capability
 - S93WD463
 - Internally Ties ORG High
 - 100% Compatible With all 16-bit Implementations
 - Eight Word Page Write Capability

OVERVIEW

The S93WD462 and S93WD463 are precision power supervisory circuits providing both active high and active low reset output. Both devices also incorporate a watchdog timer with a nominal timeout value of 1.6 seconds.

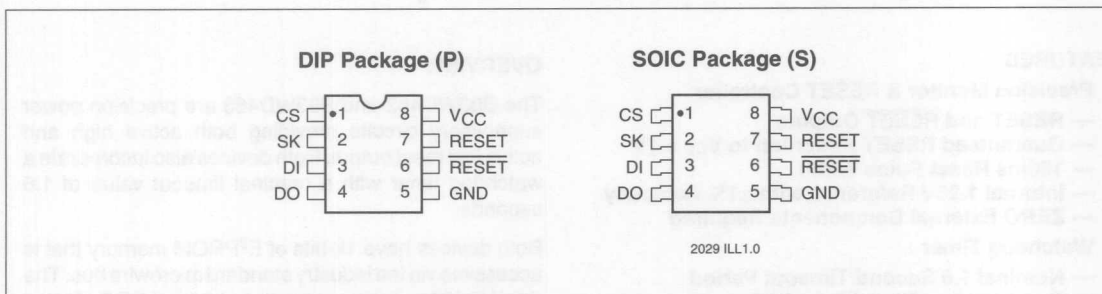
Both devices have 1k-bits of E²PROM memory that is accessible via the industry standard microwire bus. The S93WD462 is configured with an internal ORG pin tied low providing a 8-bit byte organization and the S93WD463 is configured with an internal ORG pin tied high providing a 16-bit word organization. Both the S93WD462 and S93WD463 have page write capability. The devices are designed for a minimum 1,000,000 program/erase cycles and have data retention in excess of 100 years.

BLOCK DIAGRAM





PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V _{CC}	+2.7 to 6.0V Power Supply
GND	Ground
RESET/RESET	RESET I/O

DEVICE OPERATION

APPLICATIONS

The S93WD462/WD463 is ideal for applications requiring low voltage and low power consumption. This device provides microcontroller RESET control and can be manually resettable.

RESET CONTROLLER DESCRIPTION

The S93WD462/WD463 provides a precision reset controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain reset outputs; pin 7 is an active high output and pin 6 is an active low output.

During power-up, the reset outputs remain active until V_{CC} reaches the V_{TRIP} threshold. The outputs will continue to be driven for approximately 150 ms after reaching V_{TRIP}. The reset outputs will be valid so long as V_{CC} is ≥ 1.0V. During power-down, the reset outputs will begin driving active when V_{CC} falls below V_{TRIP}.

The reset pins are I/Os; therefore, the S93WD462/WD463 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the RESET input

will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a debounce/reset extender circuit.

It should be noted the reset outputs are open drain. When used as outputs driving a circuit they need to be either tied high (RESET) or tied to ground (RESET) through the use of pull-up or pull-down resistors. Refer to the applications aid section for help in determining the value of resistor to be used. Internally these pins are weakly pulled up (RESET) and pulled down (RESET); therefore, if the signals are not being used the pins may be left unconnected.

WATCHDOG TIMER DESCRIPTION

The S93WD462/WD463 has a watchdog timer with a nominal timeout period of 1.6 seconds. Whenever the watchdog times out, it will generate a reset output to both pins 6 and 7. The watchdog timer is reset by any transition on CS.

The watchdog timer will be held in a reset state during power-on while V_{CC} is less than V_{TRIP}. Once V_{CC} exceeds V_{TRIP} the watchdog will continue to be held in a reset state for the t_{PURST} period. After t_{PURST} it will be released and the timer will begin operation. If either reset input is asserted the watchdog timer will be reset and remain in the reset condition until either t_{PURST} has expired or the reset input is released, whichever is longer.

GENERAL OPERATION

The S93WD462/WD463 is a 1024-bit nonvolatile memory intended for use with industry standard microprocessors. The S93WD463 is organized as X16, seven 9-bit instructions control the reading, writing and erase operations of the device. The S93WD462 is organized as X8, seven 10-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate



on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. See the Applications Aid section for detailed use of the ready busy status.

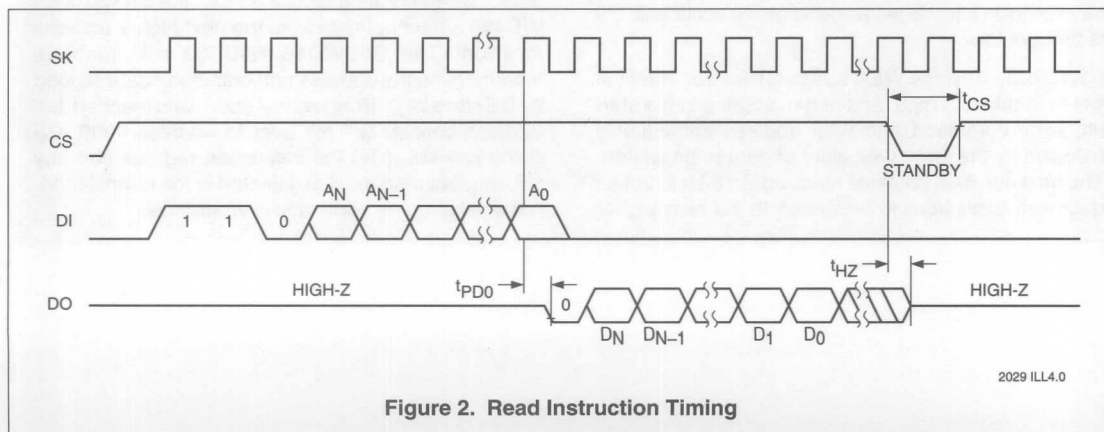
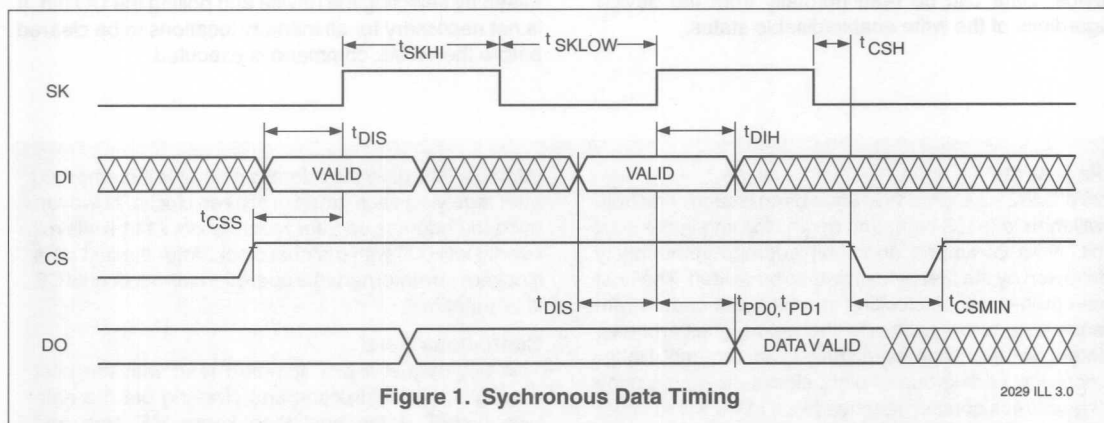
The format for all instructions is: one start bit; two op code bits and either six (x16) or seven (x8) address or instruction bits.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the S93WD462/WD463 will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start automatic erase and write cycle to the memory location specified in the instruction. The ready/busy status of the S93WD462/WD463 can be determined by selecting the device and polling the DO pin.





Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status of the S93WD462/WD463 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The S93WD462/WD463 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all S93WD462/WD463 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93WD462/WD463 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits will be in a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93WD462/WD463 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Page Write

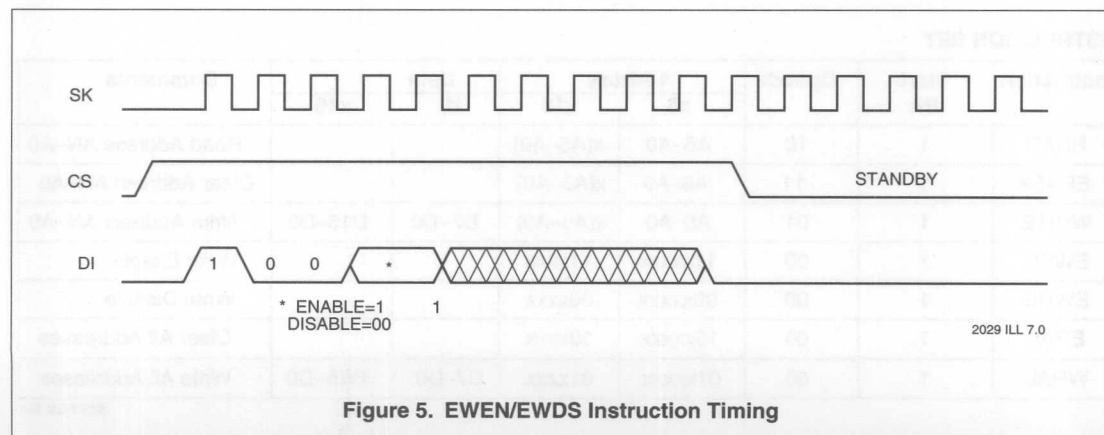
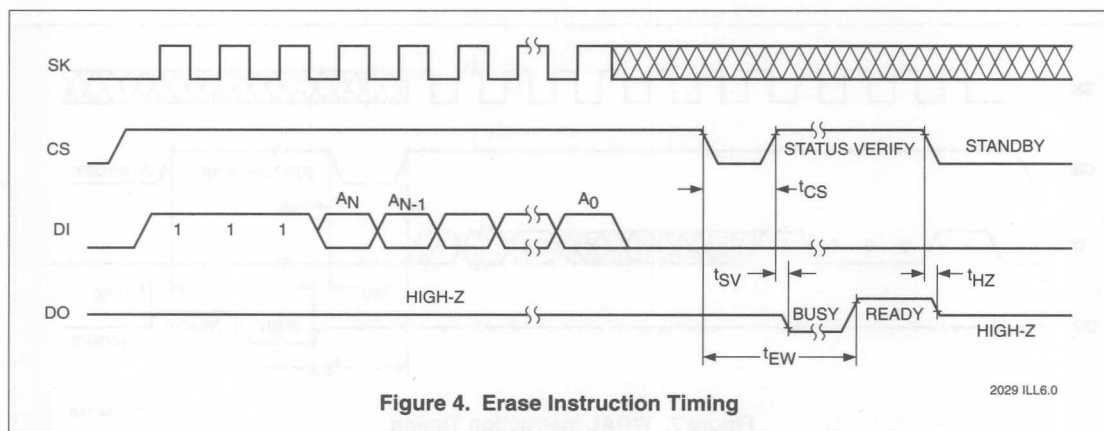
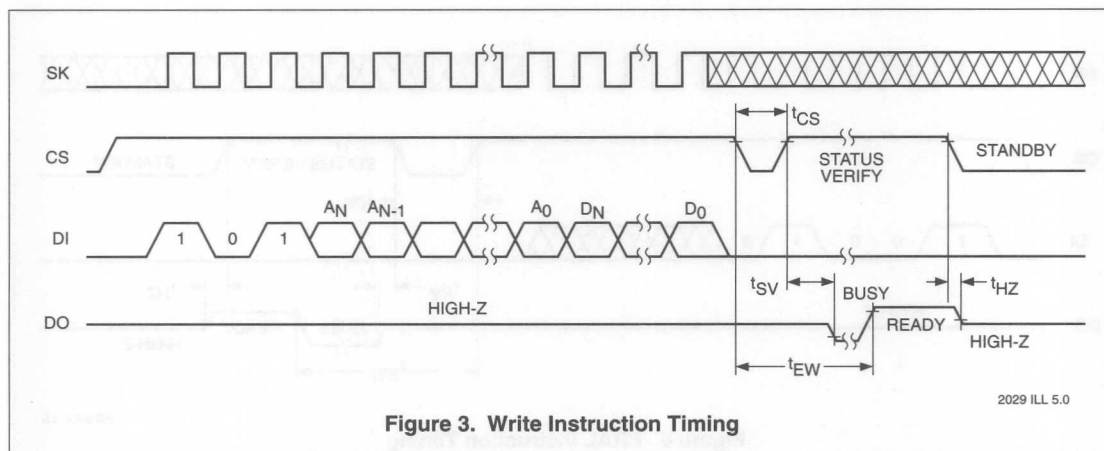
93WD462 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 7-bit address immediately followed by the first byte of data to be written. The host can then continue clocking in 8-bit bytes of data with each byte to be written to the next higher address. Internally the address pointer is incremented after receiving each group of eight clocks; however, once the address counter reaches xxx 1111 it will roll over to xxx 0000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

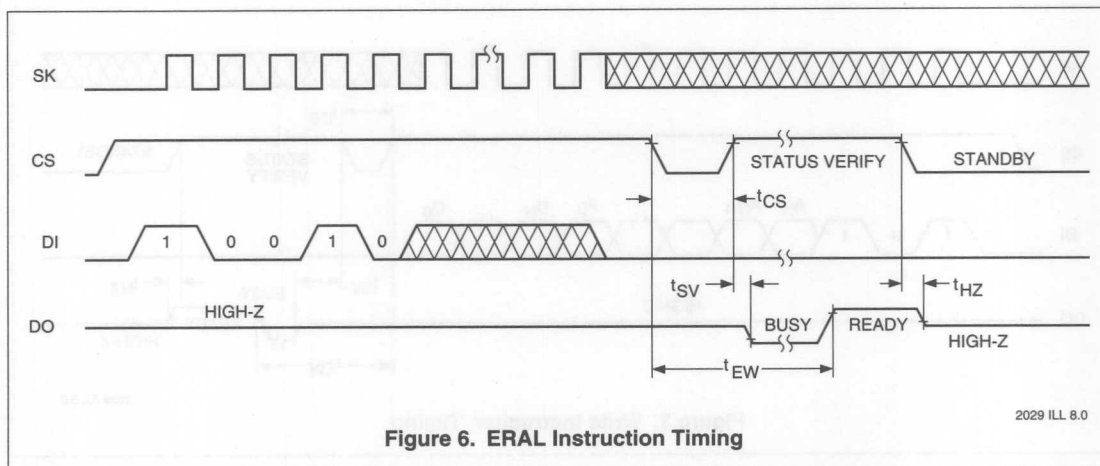
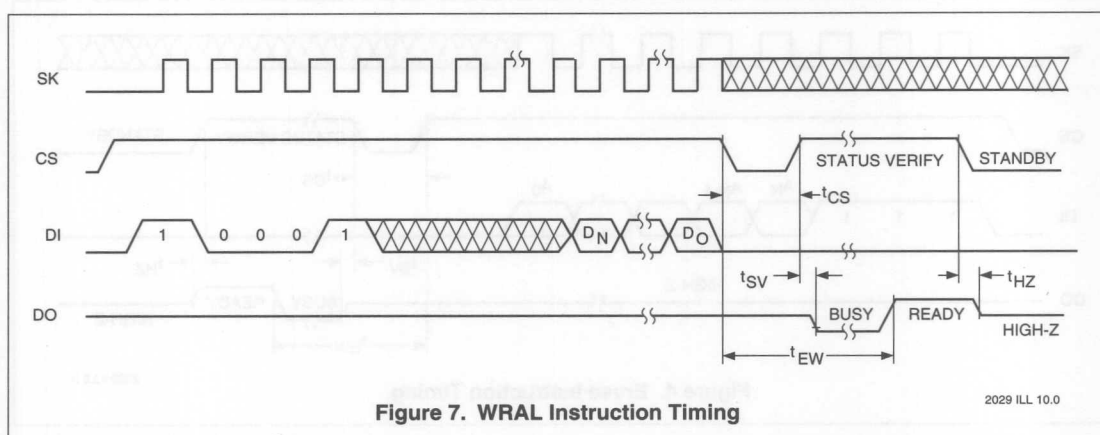
93WD463 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 6-bit address immediately followed by the first 16-bit word of data to be written. The host can then continue clocking in 16-bit words of data with each word to be written to the next higher

address. Internally the address pointer is incremented after receiving each group of sixteen clocks; however, once the address counter reaches xxx x111 it will roll over to xx x000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

Continuous Read

This begins just like a standard read with the host issuing a read instruction and clocking out the data byte [word]. If the host then keeps CS high and continues generating clocks on SK, the S93WD462/WD463 will output data from the next higher address location. The S93WD462/WD463 will continue incrementing the address and outputting data so long as CS stays high. If the highest address is reached, the address counter will roll over to address 0000. CS going low will reset the instruction register and any subsequent read must be initiated in the normal manner of issuing the command and address.



**Figure 6. ERAL Instruction Timing****Figure 7. WRAL Instruction Timing****INSTRUCTION SET**

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A6-A0	x(A5-A0)			Read Address AN-A0
ERASE	1	11	A6-A0	x(A5-A0)			Clear Address AN-A0
WRITE	1	01	A6-A0	x(A5-A0)	D7-D0	D15-D0	Write Address AN-A0
EWEN	1	00	11xxxxx	11xxxx			Write Enable
EWDS	1	00	00xxxxx	00xxxx			Write Disable
ERAL	1	00	10xxxxx	10xxxx			Clear All Addresses
WRAL	1	00	01xxxxx	01xxxx	D7-D0	D15-D0	Write All Addresses

2029 PGM T5.0

**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground ⁽¹⁾	-2.0V to $V_{CC} + 2.0V$
V_{CC} with Respect to Ground	-2.0V to +7.0V
Package Power Dissipation Capability ($T_a = 25^\circ\text{C}$)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽²⁾	100 mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

2029 PGM T7.0

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
$N_{END}^{(3)}$	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
$T_{DR}^{(3)}$	Data Retention	100		Years	MIL-STD-883, Test Method 1008
$V_{ZAP}^{(3)}$	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
$I_{LTH}^{(3)(4)}$	Latch-Up	100		mA	JEDEC Standard 17

2029 PGM T2.1

D.C. OPERATING CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC}	Power Supply Current (Operating)			3	mA	$D_I = 0.0V$, $f_{SK} = 1\text{MHz}$ $V_{CC} = 5.0V$, $CS = 5.0V$, Output Open
I_{SB}	Power Supply Current (Standby)			50	μA	$CS = 0V$ Reset Outputs Open
I_{LI}	Input Leakage Current			2	μA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current (Including ORG pin)			10	μA	$V_{OUT} = 0V$ to V_{CC} , $CS = 0V$
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage	-0.1 2		0.8 $V_{CC}+1$	V V	$4.5V \leq V_{CC} < 5.5V$
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	0 $V_{CC} \times 0.7$		$V_{CC} \times 0.2$ $V_{CC}+1$	V V	$1.8V \leq V_{CC} < 2.7V$
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	2.4		0.4	V V	$4.5V \leq V_{CC} < 5.5V$ $I_{OL} = 2.1\text{mA}$ $I_{OH} = -400\mu\text{A}$
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	$V_{CC}-0.2$		0.2	V V	$1.8V \leq V_{CC} < 2.7V$ $I_{OL} = 1\text{mA}$ $I_{OH} = -100\mu\text{A}$

2029 PGM T3.0

Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is $V_{CC} + 0.5V$, which may overshoot to $V_{CC} + 2.0V$ for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to $V_{CC} + 1V$.



PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C _{OUT} ⁽¹⁾	OUTPUT CAPACITANCE (DO)	5	pF	V _{OUT} =OV
C _{IN} ⁽¹⁾	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V _{IN} =OV

Note:

2029 PGM T4.0

(1) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

SYMBOL	PARAMETER	Limits				UNITS	Test Conditions
		V _{CC} =2.7V-4.5V		V _{CC} =4.5V-5.5V			
		Min.	Max.	Min.	Max.		
t _{CSS}	CS Setup Time	100		50		ns	C _L = 100pF
t _{CSH}	CS Hold Time	0		0		ns	
t _{DIS}	DI Setup Time	200		100		ns	
t _{DIH}	DI Hold Time	200		100		ns	
t _{PD1}	Output Delay to 1		0.5		0.25	μs	
t _{PD0}	Output Delay to 0		0.5		0.25	μs	
t _{HZ} ⁽¹⁾	Output Delay to High-Z		200		100	ns	
t _{EW}	Program/Erase Pulse Width		10		10	ms	
t _{CSSMIN}	Minimum CS Low Time	0.5		0.25		μs	
t _{SKHI}	Minimum SK High Time	0.5		0.25		μs	
t _{SKLOW}	Minimum SK Low Time	0.5		0.25		μs	
t _{SV}	Output Delay to Status Valid		0.5		0.25	μs	
SK _{MAX}	Maximum Clock Frequency	DC	500	DC	1000	KHZ	

Note:

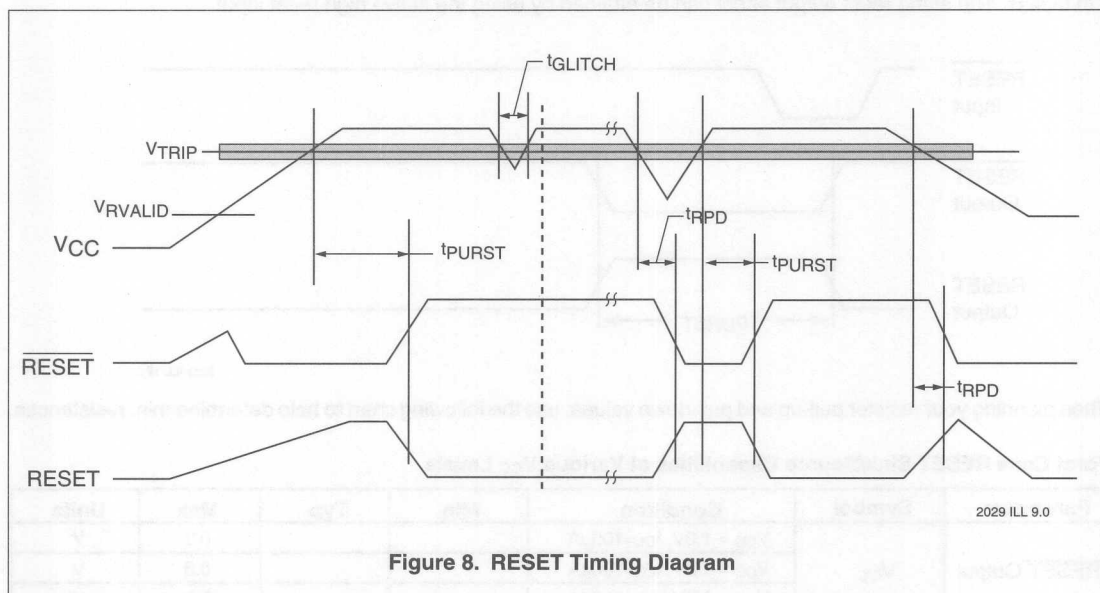
2029 PGM T6.0

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	2.7		5 Volt-A		5 Volt-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.50	4.75	V
tPURT	Power-Up Reset Timeout	130	270	130	270	130	270	ms
tRPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage IOL=1mA		0.4		0.4		0.4	V
VOHRS	RESET Output High IOH	VCC-.75		VCC-.75		VCC-.75		V

2029 PGM T1.0



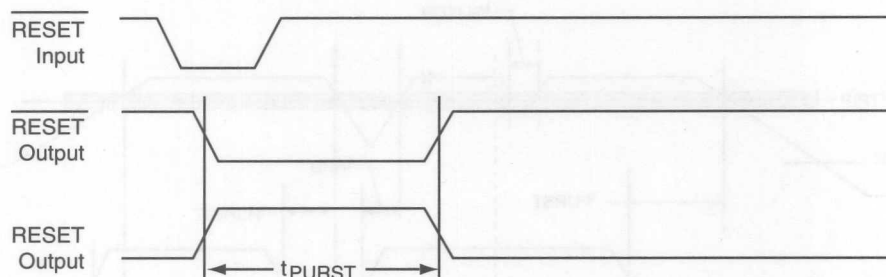
2029 ILL 9.0

Figure 8. RESET Timing Diagram



Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S93WD462/WD463 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



2029 ILL 12.0

When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V _{OL}	V _{CC} = 1.0V, I _{OL} =100μA			0.3	V
		V _{CC} = 1.2V, I _{OL} =100μA			0.3	V
		V _{CC} = 3.0V, I _{OL} =500μA			0.3	V
		V _{CC} = 3.6V, I _{OL} =500μA			0.3	V
		V _{CC} = 4.5V, I _{OL} =750μA			0.3	V
RESET Output Voltage	V _{OL}	V _{CC} = 1.0V, I _{OL} =100μA			0.4	V
		V _{CC} = 1.2V, I _{OL} =150μA			0.4	V
		V _{CC} = 3.0V, I _{OL} =750μA			0.4	V
		V _{CC} = 3.6V, I _{OL} =1mA			0.4	V
		V _{CC} = 4.5V, I _{OL} =1mA			0.4	V
RESET Output Voltage	V _{OH}	V _{CC} = 1.0V, I _{OH} =400μA	V _{CC} -0.75			V
		V _{CC} = 1.2V, I _{OH} =800μA	V _{CC} -0.75			V
		V _{CC} = 3.0V, I _{OH} =800μA	V _{CC} -0.5			V
		V _{CC} = 3.6V, I _{OH} =800μA	V _{CC} -0.5			V
		V _{CC} = 4.5V, I _{OH} =800μA	V _{CC} -0.5			V

2029 PGM T5.0

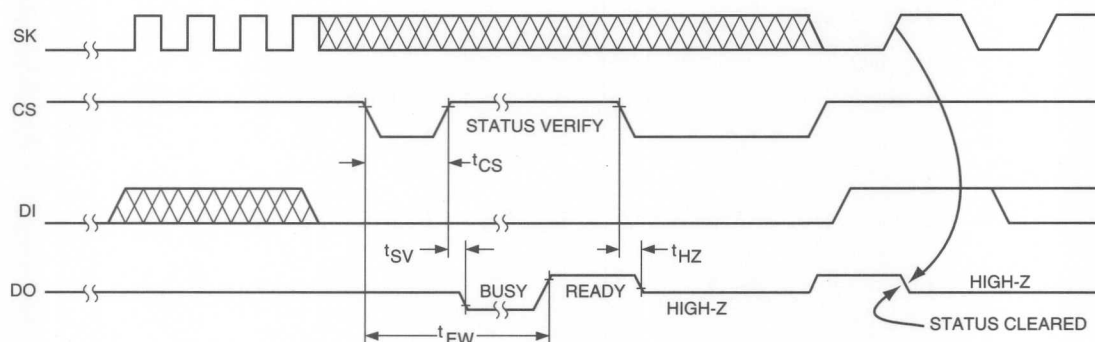


Ready/Busy Status

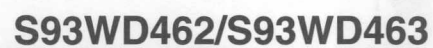
During the internal write operation the S93WD462/WD463 memory array is inaccessible. After starting the write operation (taking CS low) the host can implement a 10ms timeout routine or alternatively it can employ a polling routine that tests the state of the DO pin.

After starting the write, testing for the status is easily accomplished by taking CS high and testing the state of DO. If it is low the device is still busy with the internal write. If it is high the write operation has completed.

For the polling routine the host has the option of toggling CS for each test of DO, or it can place CS high and then intermittently test DO. SK is not required for any of these operations. Once the device is ready, it will continue to drive DO high whenever the S93WD462/WD463 is selected. The ready state of DO can be cleared by clocking in a start bit; this start bit can either be the beginning of a new command sequence or it can be a dummy start bit with CS returning low before the host issues a new command.



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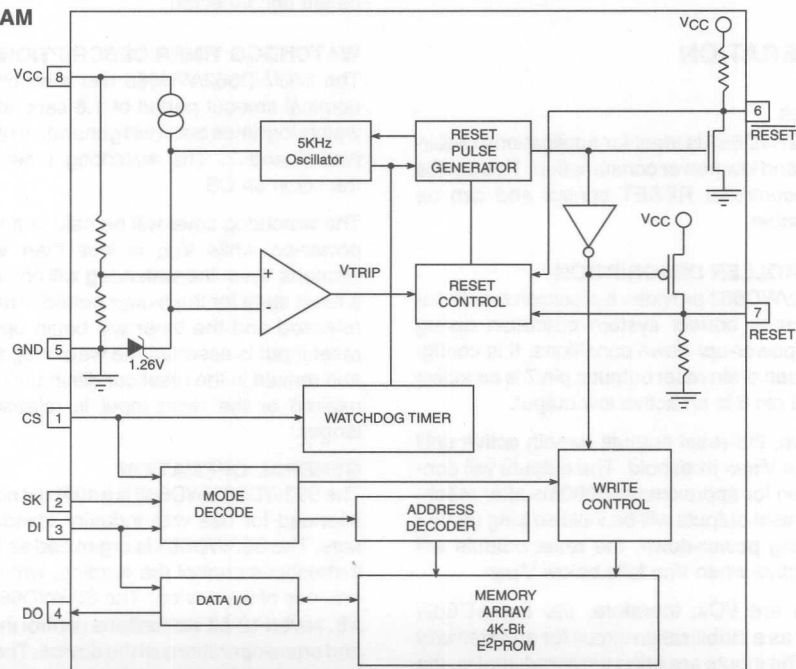
**Precision Supply-Voltage Monitor and Reset Controller
 With a Watchdog Timer and 4k-bit Microwire Memory**
FEATURES

- **Precision Monitor & RESET Controller**
 - RESET and $\overline{\text{RESET}}$ Outputs
 - Guaranteed RESET Assertion to $V_{CC} = 1V$
 - 200ms Reset Pulse Width
 - Internal 1.26V Reference with $\pm 1\%$ Accuracy
 - ZERO External Components Required
- **Watchdog Timer**
 - Nominal 1.6 Second Timeout Period
 - Reset by Any Transition of CS
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 - **S93WD662**
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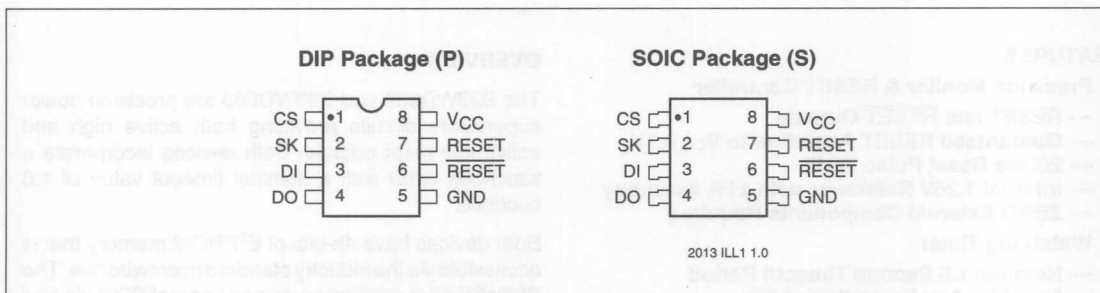
OVERVIEW

The S93WD662 and S93WD663 are precision power supervisory circuits providing both active high and active low reset outputs. Both devices incorporate a watchdog timer with a nominal timeout value of 1.6 seconds.

Both devices have 4k-bits of E²PROM memory that is accessible via the industry standard microwire bus. The S93WD662 is configured with an internal ORG pin tied low providing a 8-bit byte organization and the S93WD663 is configured with an internal ORG pin tied high providing a 16-bit word organization. Both the S93WD662 and S93WD663 have page write capability. The devices are designed for a minimum 1,000,000 program/erase cycles and have data retention in excess of 100 years.

BLOCK DIAGRAM


2013 ILL2 1.0

**PIN CONFIGURATION****PIN FUNCTIONS**

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V _{CC}	+2.7 to 6.0V Power Supply
GND	Ground
RESET/RESET	RESET I/O

a low to high transition and the **RESET** input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a debounce/reset extender circuit.

It should be noted the reset outputs are open drain. When used as outputs driving a circuit they need to be either tied high (**RESET**) or tied to ground (**RESET**) through the use of pull-up or pull-down resistors. Refer to the applications aid section for help in determining the value of resistor to be used. Internally these pins are weakly pulled up (**RESET**) and pulled down (**RESET**): therefore, if the signals are not being used the pins may be left unconnected.

DEVICE OPERATION**APPLICATIONS**

The S93WD662/WD663 is ideal for applications requiring low voltage and low power consumption. This device provides microcontroller RESET control and can be manually resettable.

RESET CONTROLLER DESCRIPTION

The S93WD662/WD663 provides a precision reset controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain reset outputs; pin 7 is an active high output and pin 6 is an active low output.

During power-up, the reset outputs remain active until V_{CC} reaches the V_{TRIP} threshold. The outputs will continue to be driven for approximately 200ms after reaching V_{TRIP}. The reset outputs will be valid so long as V_{CC} is $\geq 1.0V$. During power-down, the reset outputs will begin driving active when V_{CC} falls below V_{TRIP}.

The reset pins are I/Os; therefore, the S93WD662/WD663 can act as a stabilization circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting

WATCHDOG TIMER DESCRIPTION

The S93WD662/WD663 has a watchdog timer with a nominal timeout period of 1.6 seconds. Whenever the watchdog times out, it will generate a reset output to both pins 6 and 7. The watchdog timer is reset by any transition on CS.

The watchdog timer will be held in a reset state during power-on while V_{CC} is less than V_{TRIP}. Once V_{CC} exceeds V_{TRIP} the watchdog will continue to be held in a reset state for the t_{PURST} period. After t_{PURST} it will be released and the timer will begin operation. If either reset input is asserted the watchdog timer will be reset and remain in the reset condition until either t_{PURST} has expired or the reset input is released, whichever is longer.

GENERAL OPERATION

The S93WD662/WD663 is a 4096-bit nonvolatile memory intended for use with industry standard microprocessors. The S93WD663 is organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. The S93WD662 is organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate on chip, the high voltage required during any write operation.



Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. See the Applications Aid section for detailed use of the ready/busy status.

The format for all instructions is: one start bit; two op code bits and either eight (x16) or nine (x8) address or instruction bits.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the S93WD662/WD663 will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start automatic erase and write cycle to the memory location specified in the instruction. The ready/busy status of the S93WD662/WD663 can be determined by selecting the device and polling the DO pin.

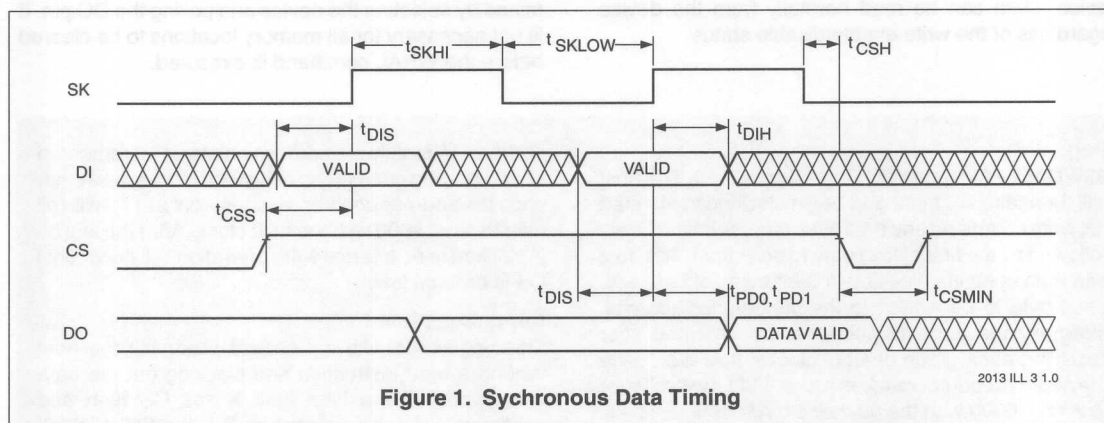


Figure 1. Synchronous Data Timing

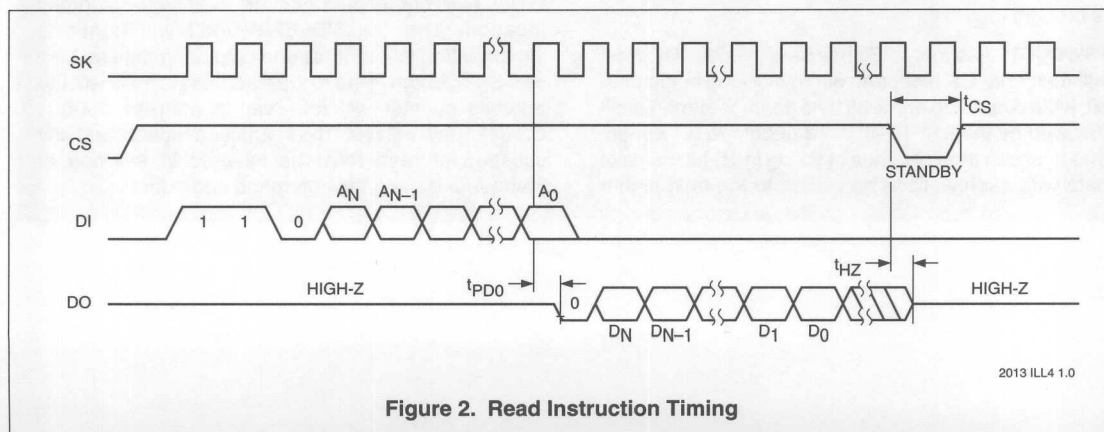


Figure 2. Read Instruction Timing



Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status of the S93WD662/WD663 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Erase/Write Enable and Disable

The S93WD662/WD663 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all S93WD662/WD663 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93WD662/WD663 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93WD662/WD663 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Page Write

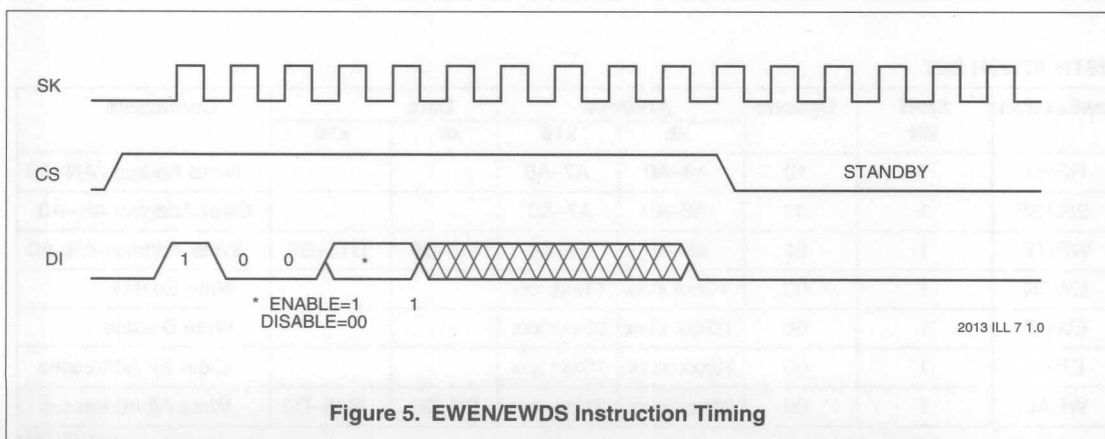
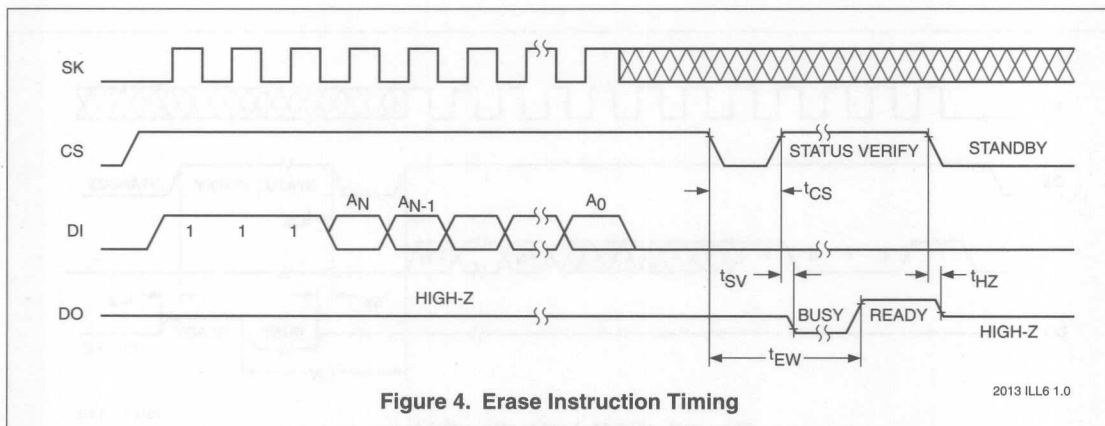
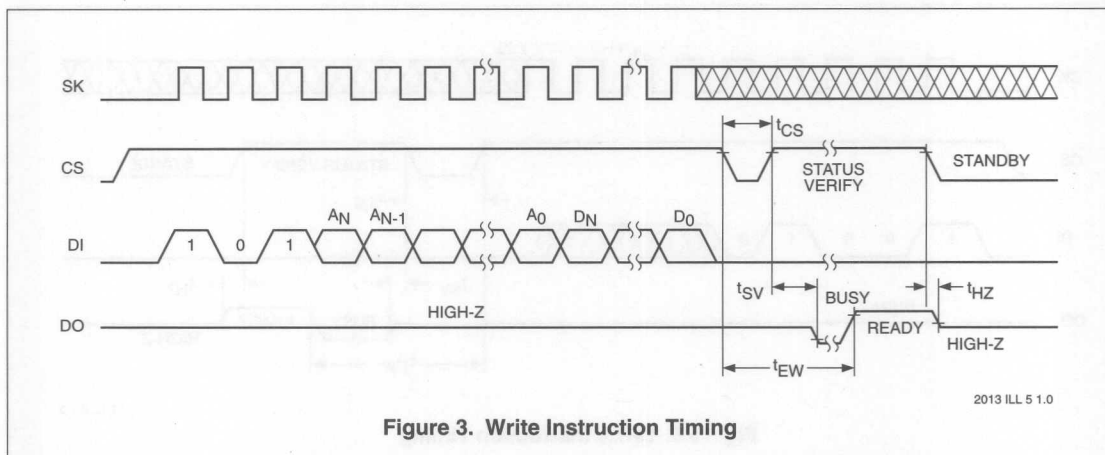
93WD662 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 9-bit byte address immediately followed by the first byte of data to be written. The host can then continue clocking in 8-bit bytes of data with each byte to be written to the next higher address. Internally the address pointer is incremented after receiving each group of eight clocks; however, once the address counter reaches x xxx 1111 it will roll over to x xxx 0000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

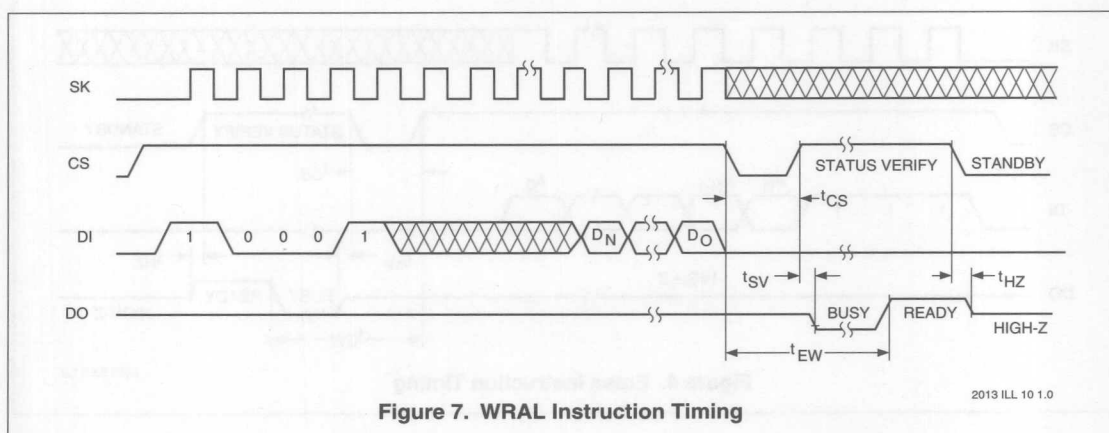
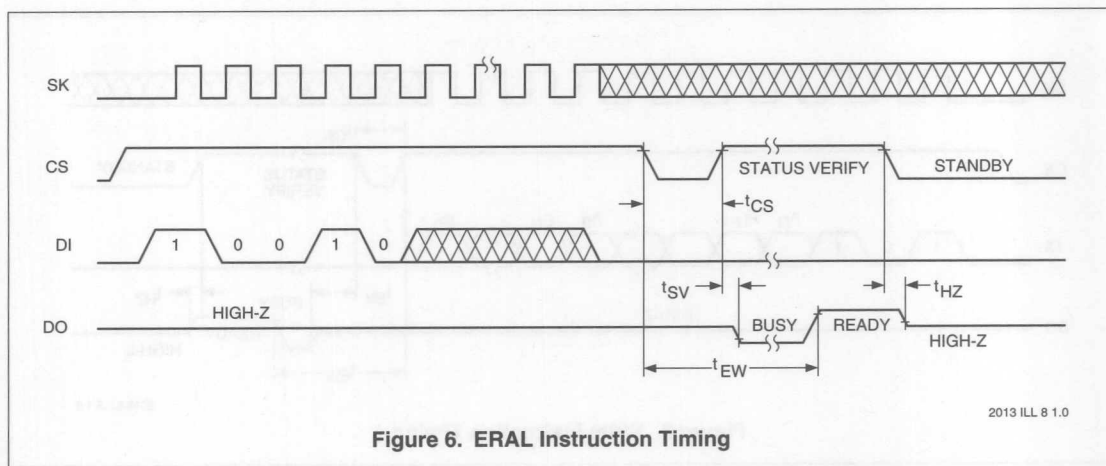
93WD663 - Assume WEN has been issued. The host will then take CS high, and begin clocking in the start bit, write command and 8-bit byte address immediately followed by the first 16-bit word of data to be written. The host can then continue clocking in 16-bit words of data with each word to be written to the next higher

address. Internally the address pointer is incremented after receiving each group of sixteen clocks; however, once the address counter reaches xxxx x111 it will roll over to xxxx x000 with the next clock. After the last bit is clocked in no internal write operation will occur until CS is brought low.

Continuous Read

This begins just like a standard read with the host issuing a read instruction and clocking out the data byte [word]. If the host then keeps CS high and continues generating clocks on SK, the S93WD662/WD663 will output data from the next higher address location. The S93WD662/WD663 will continue incrementing the address and outputting data so long as CS stays high. If the highest address is reached, the address counter will roll over to address 0000. CS going low will reset the instruction register and any subsequent read must be initiated in the normal manner of issuing the command and address.





INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A8-A0	A7-A0			Read Address AN-A0
ERASE	1	11	A8-A0	A7-A0			Clear Address AN-A0
WRITE	1	01	A8-A0	A7-A0	D7-D0	D15-D0	Write Address AN-A0
EWEN	1	00	11xxx xxxx	11xxx xxx			Write Enable
EWDS	1	00	00xxx xxxx	00xxx xxx			Write Disable
ERAL	1	00	10xxx xxxx	10xxx xxx			Clear All Addresses
WRAL	1	00	01xxx xxxx	01xxx xxx	D7-D0	D15-D0	Write All Addresses

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**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground ⁽¹⁾	-2.0V to +V _{CC} +2.0V
V _{CC} with Respect to Ground	-2.0V to +7.0V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽²⁾	100 mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
NEND ⁽³⁾	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
TDR ⁽³⁾	Data Retention	100		Years	MIL-STD-883, Test Method 1008
VZAP ⁽³⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
ILTH ⁽³⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

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D.C. OPERATING CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I _{CC}	Power Supply Current (Operating)			3	mA	DI = 0.0V, f _{SK} = 1MHz V _{CC} = 5.0V, CS = 5.0V, Output Open
I _{SB}	Power Supply Current (Standby)			50	μA	CS = 0V Reset Outputs Open
I _{LI}	Input Leakage Current			2	μA	V _{IN} = 0V to V _{CC}
I _{LO}	Output Leakage Current (Including ORG pin)			10	μA	V _{OUT} = 0V to V _{CC} , CS = 0V
V _{IL1} V _{IH1}	Input Low Voltage Input High Voltage	-0.1 2		0.8 V _{CC} +1	V V	4.5V ≤ V _{CC} < 5.5V
V _{IL2} V _{IH2}	Input Low Voltage Input High Voltage	0 V _{CC} X0.7		V _{CC} X0.2 V _{CC} +1	V V	1.8V ≤ V _{CC} < 2.7V
V _{OL1} V _{OH1}	Output Low Voltage Output High Voltage	2.4		0.4	V V	4.5V ≤ V _{CC} < 5.5V I _{OL} = 2.1mA I _{OH} = -400μA
V _{OL2} V _{OH2}	Output Low Voltage Output High Voltage	V _{CC} -0.2		0.2	V V	1.8V ≤ V _{CC} < 2.7V I _{OL} = 1mA I _{OH} = -100μA

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Note:

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.



PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C _{OUT} ⁽¹⁾	OUTPUT CAPACITANCE (DO)	5	pF	V _{OUT} =OV
C _{IN} ⁽¹⁾	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V _{IN} =OV

Note:

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(1) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

SYMBOL	PARAMETER	Limits				UNITS	Test Conditions
		V _{CC} =2.7V-4.5V		V _{CC} =4.5V-5.5V			
		Min.	Max.	Min.	Max.		
t _{CSS}	CS Setup Time	100		50		ns	C _L = 100pF
t _{CSH}	CS Hold Time	0		0		ns	
t _{DIS}	DI Setup Time	200		100		ns	
t _{DIH}	DI Hold Time	200		100		ns	
t _{PD1}	Output Delay to 1		0.5		0.25	μs	
t _{PD0}	Output Delay to 0		0.5		0.25	μs	
t _{HZ} ⁽¹⁾	Output Delay to High-Z		200		100	ns	
t _{EW}	Program/Erase Pulse Width		10		10	ms	
t _{CSMIN}	Minimum CS Low Time	0.5		0.25		μs	
t _{SKHI}	Minimum SK High Time	0.5		0.25		μs	
t _{SKLOW}	Minimum SK Low Time	0.5		0.25		μs	
t _{SV}	Output Delay to Status Valid		0.5		0.25	μs	
SK _{MAX}	Maximum Clock Frequency	DC	500	DC	1000	KHZ	

Note:

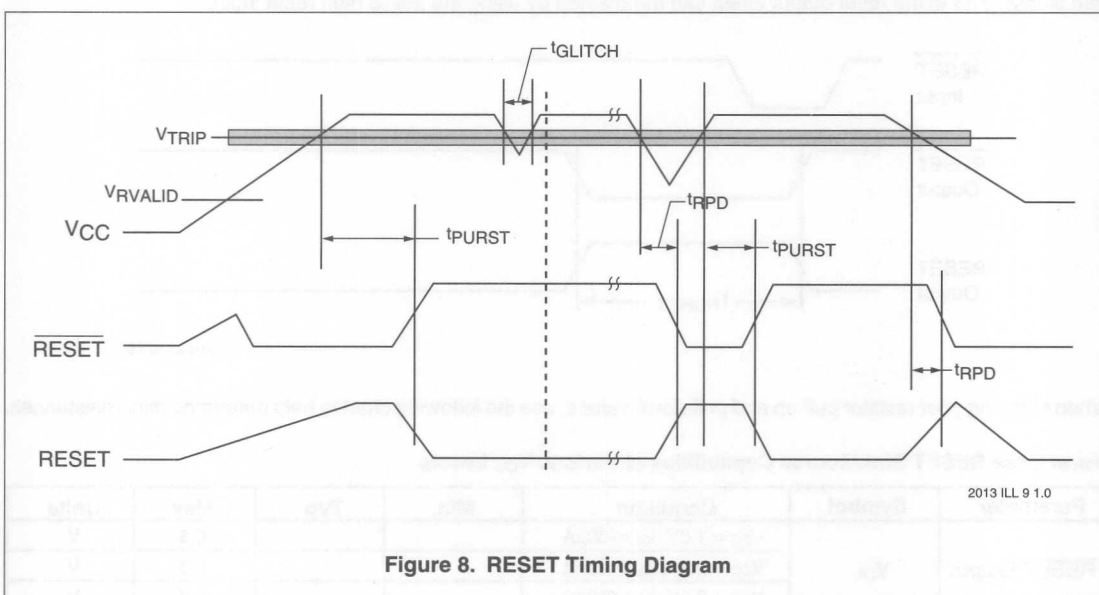
2013 PGM T6 1.0

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	2.7		5 Volt-A		5 Volt-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.50	4.75	V
tpURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
trPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage $I_{OL}=1\text{mA}$		0.4		0.4		0.4	V
VOHRS	RESET Output High I_{OH}	$V_{CC}-75$		$V_{CC}-75$		$V_{CC}-75$		V

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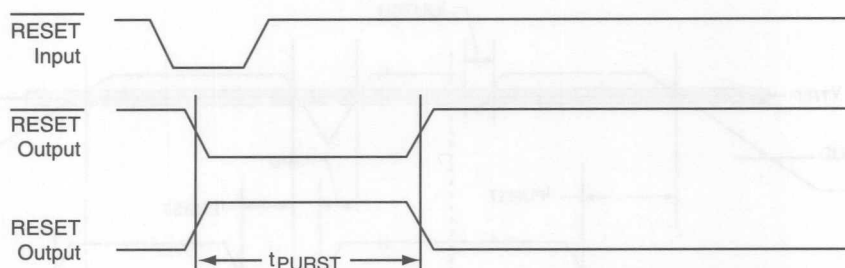


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Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S93WD662/WD663 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



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When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL} = 100\mu A$			0.3	V
		$V_{CC} = 1.2V, I_{OL} = 100\mu A$			0.3	V
		$V_{CC} = 3.0V, I_{OL} = 500\mu A$			0.3	V
		$V_{CC} = 3.6V, I_{OL} = 500\mu A$			0.3	V
		$V_{CC} = 4.5V, I_{OL} = 750\mu A$			0.3	V
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL} = 100\mu A$			0.4	V
		$V_{CC} = 1.2V, I_{OL} = 150\mu A$			0.4	V
		$V_{CC} = 3.0V, I_{OL} = 750\mu A$			0.4	V
		$V_{CC} = 3.6V, I_{OL} = 1mA$			0.4	V
		$V_{CC} = 4.5V, I_{OL} = 1mA$			0.4	V
RESET Output Voltage	V_{OH}	$V_{CC} = 1.0V, I_{OH} = 400\mu A$	$V_{CC} - 0.75$			V
		$V_{CC} = 1.2V, I_{OH} = 800\mu A$	$V_{CC} - 0.75$			V
		$V_{CC} = 3.0V, I_{OH} = 800\mu A$	$V_{CC} - 0.5$			V
		$V_{CC} = 3.6V, I_{OH} = 800\mu A$	$V_{CC} - 0.5$			V
		$V_{CC} = 4.5V, I_{OH} = 800\mu A$	$V_{CC} - 0.5$			V

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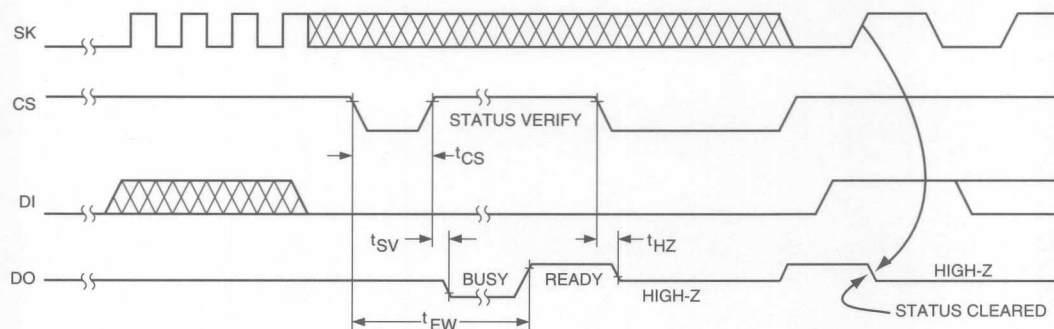


Ready/Busy Status

During the internal write operation the S93WD662/WD663 memory array is inaccessible. After starting the write operation (taking CS low) the host can implement a 10ms timeout routine or alternatively it can employ a polling routine that tests the state of the DO pin.

After starting the write, testing for the status is easily accomplished by taking CS high and testing the state of DO. If it is low the device is still busy with the internal write. If it is high the write operation has completed.

For the polling routine the host has the option of toggling CS for each test of DO, or it can place CS high and then intermittently test DO. SK is not required for any of these operations. Once the device is ready, it will continue to drive DO high whenever the S93WD662/WD663 is selected. The ready state of DO can be cleared by clocking in a start bit; this start bit can either be the beginning of a new command sequence or it can be a dummy start bit with CS returning low before the host issues a new command.



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SECTION 6 **Voltage Supervisory Circuits Integrated with a I²C Nonvolatile Memory**

S4242 Voltage Supervisor with 4K-bit E ² PROM Memory	6-3
S42WD42 Voltage Supervisor and Watchdog with 4K-bit E ² PROM Memory	6-17
S4261 Voltage Supervisor with 16K-bit E ² PROM Memory	6-31
S42WD61 Voltage Supervisor and Watchdog with 16K-bit E ² PROM Memory	6-45



SECTION 3	Voltage Supervisory Circuitry Integrated with a 1°C Nonvolatile Memory
3-1	3-1.1 Voltage Supervisor with 16-bit 1°C Nonvolatile Memory
3-2	3-1.2 Voltage Supervisor with 16-bit 1°C Nonvolatile Memory
3-3	3-1.3 Voltage Supervisor with 16-bit 1°C Nonvolatile Memory
3-4	3-1.4 Voltage Supervisor with 16-bit 1°C Nonvolatile Memory

**Precision Voltage Supervisory Circuit
and 4K I²C Memory**

3 and 5 Volt Systems

FEATURES

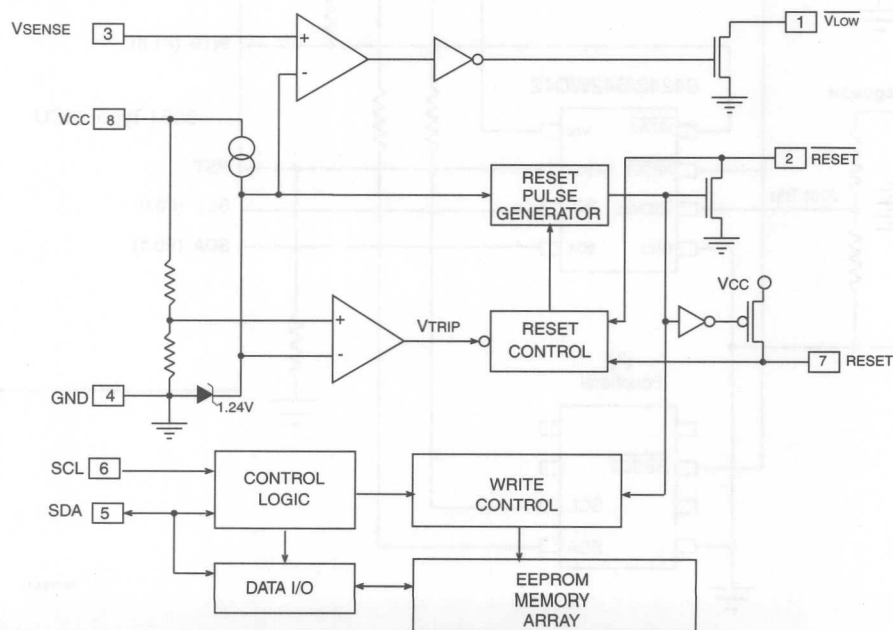
- **Precision Dual Voltage Monitor**
 - Automatic V_{CC} Supply Monitor
 - Dual reset outputs for complex microcontroller systems
 - Integrated memory write lockout function
 - No external components required
- **Second voltage monitor output**
 - Separate V_{LOW} output
 - Generates interrupt to MCU
 - Generates RESET for dual supply systems
 - Guaranteed output assertion to V_{CC} ≤ 1V
- **Memory Internally Organized 512K X 8**
 - Two Wire Serial Interface (I²C™)
- **High Reliability**
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: 100 years
- **8-Pin PDIP or SOIC Packages**

OVERVIEW

The S4242 is a precision power supervisory circuit. It automatically monitors the device's V_{CC} level (3V or 5V) and will generate a reset output on two complementary open drain outputs. In addition to the V_{CC} monitoring, the S4242 also provides a second voltage comparator input. This input has an independent open drain output that can be wire-OR'ed with the RESET I/O or it can be used as a system interrupt.

The S4242 also has an integrated 4K-bit nonvolatile memory. The memory conforms to the industry standard two-wire serial interface.

BLOCK DIAGRAM

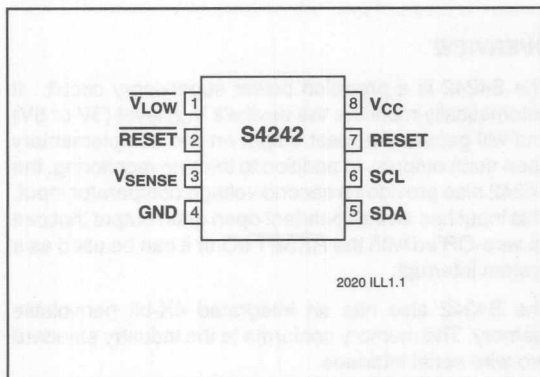


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S4242

PIN CONFIGURATIONS



PIN NAMES

Symbol	Pin	Description
$\overline{V_{LOW}}$	1	Open Drain Output Active When V_{SENSE} is < 1.24V
RESET	2	Active Low RESET Input/Output
V_{SENSE}	3	Second Monitor Voltage Input. When less than 1.24V the $\overline{V_{LOW}}$ output will be driven
V_{SS}	4	Analog and Digital Ground
SDA	5	Serial Memory Input/Output data line
SCL	6	Serial Memory clock input
RESET	7	Active High RESET Input/Output
V_{CC}	8	Supply Voltage

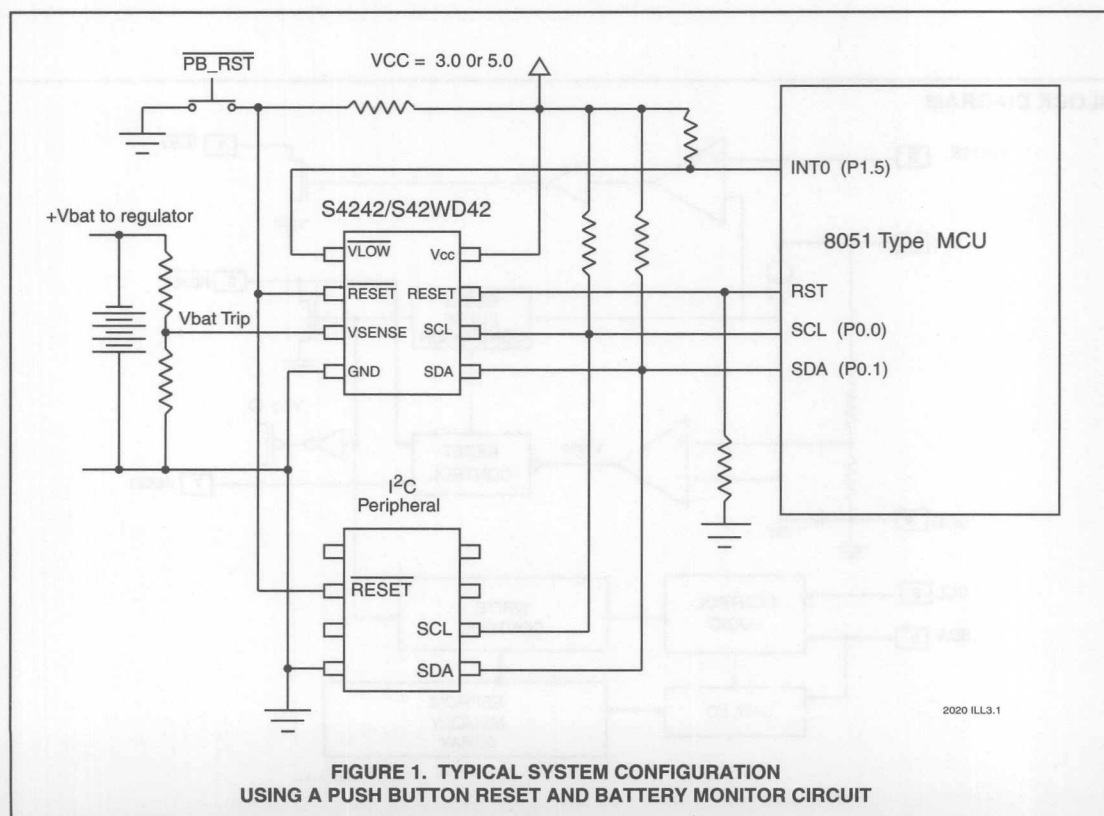


FIGURE 1. TYPICAL SYSTEM CONFIGURATION
USING A PUSH BUTTON RESET AND BATTERY MONITOR CIRCUIT

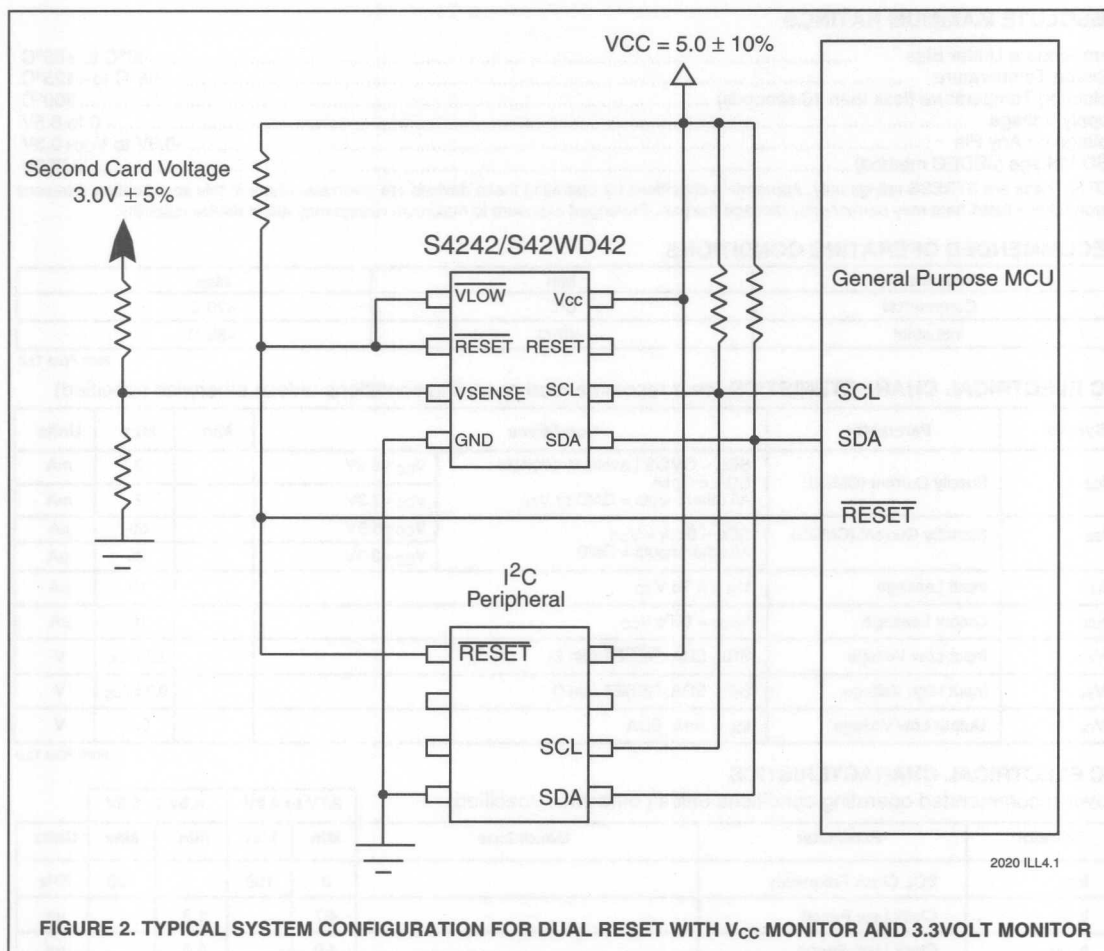


FIGURE 2. TYPICAL SYSTEM CONFIGURATION FOR DUAL RESET WITH V_{CC} MONITOR AND 3.3VOLT MONITOR

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SS}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	SCL, SDA, RESET (pin 2)		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	SCL, SDA, RESET (pin 7)		$0.7 \times V_{CC}$	V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$ SDA		0.4	V

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AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

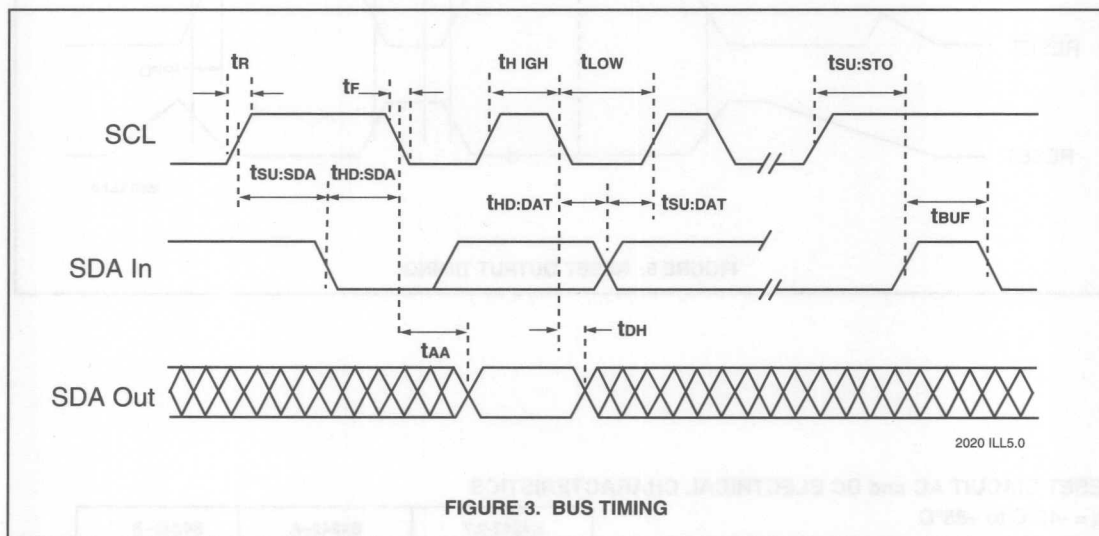
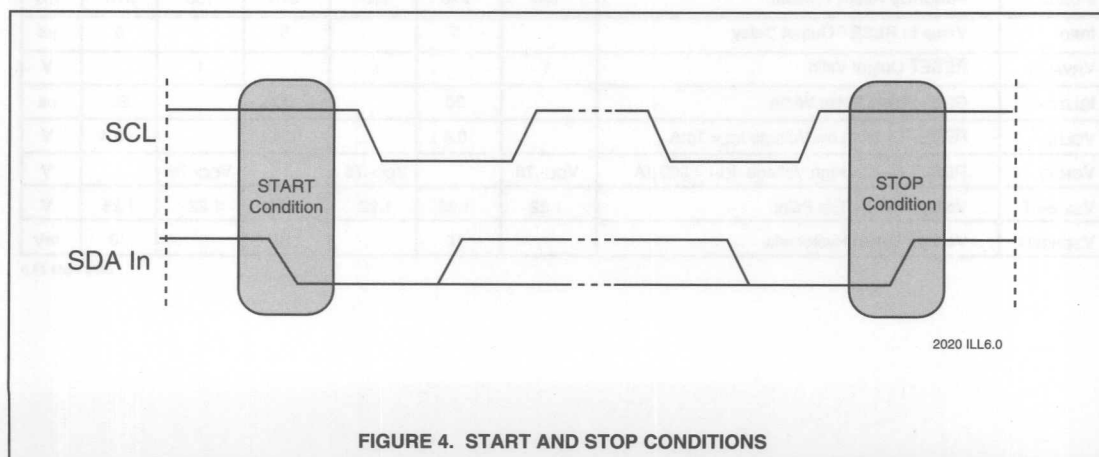
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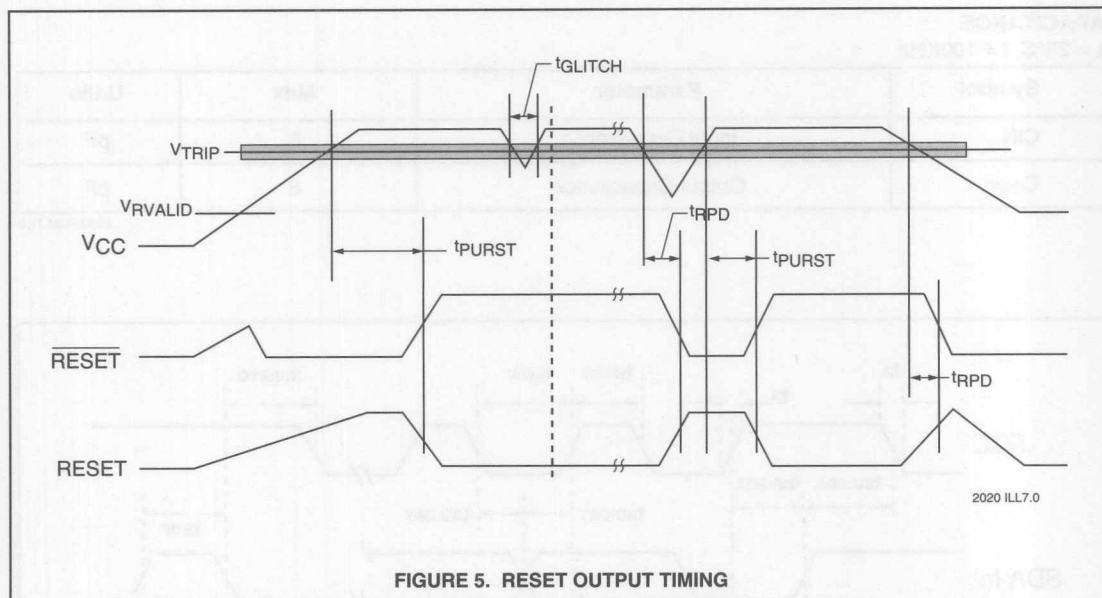
**CAPACITANCE**

TA = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
CIN	Input Capacitance	5	pF
COUT	Output Capacitance	8	pF

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**FIGURE 3. BUS TIMING****FIGURE 4. START AND STOP CONDITIONS**

**FIGURE 5. RESET OUTPUT TIMING****RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS** $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$

Symbol	Parameter	S4242-2.7		S4242-A		S4242-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
tPURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
tRPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage $I_{OL} = 1\text{mA}$		0.4		0.4		0.4	V
VOHRS	RESET Output High Voltage $I_{OH} = 800\text{ }\mu\text{A}$	$V_{CC} - .75$		$V_{CC} - .75$		$V_{CC} - .75$		V
VSENSET	Voltage Sense Trip Point	1.22	1.25	1.22	1.25	1.22	1.25	V
VSENSEH	Voltage Sense Hysteresis		10		10		10	mV

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PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wired ORed with any number of open-drain or open-collector outputs.

RESET - RESET is an active low open-drain output. It should be tied high through a pull-up resistor connected to V_{CC} . RESET is an I/O, therefore it may also be used to condition a RESET signal generated by another device; it can also be used to debounce a pushbutton input.

RESET - RESET is an active high open drain (PFET) output. It should be tied low through a pull-down resistor connected to ground. RESET is an I/O, therefore it may also be used to condition a RESET signal generated by another device.

V_{SENSE} - The V_{SENSE} input is used as a second voltage sensing input. The pin is tied to a comparator that uses the precision internal 1.24V reference.

V_{LOW} - The V_{LOW} output is an open drain which is driven low whenever the V_{SENSE} input is less than 1.24V. For correct operation this output should be tied high through a pull-up resistor connected to V_{CC} .

ENDURANCE AND DATA RETENTION

The S4242 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

Reset Controller Description

The S4242 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output. For proper operation pin 7 should be tied low through a pull-down resistor while pin 2 should be tied high through a resistor connected to V_{CC} .

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP} . The RESET outputs will be valid so long as V_{CC} is $> 1.0V$. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP} .

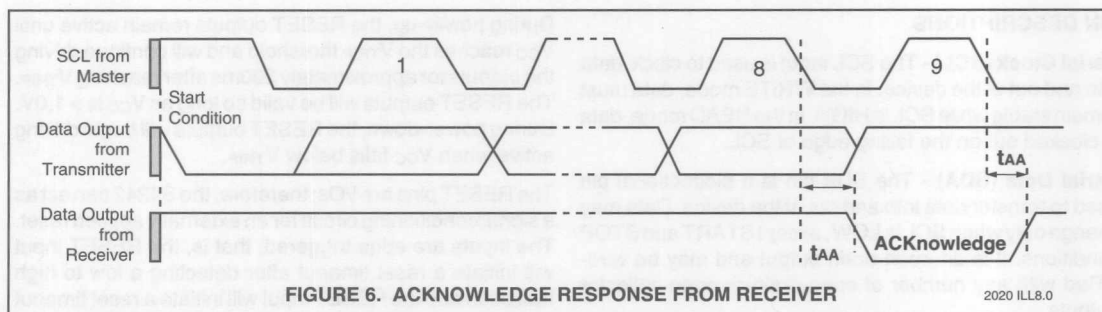
The RESET pins are I/Os; therefore, the S4242 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the RESET input will initiate a reset timeout after detecting a high to low transition. Refer to the applications information section for more details on device operation as a reset conditioning circuit.

Voltage Sensor Description

The S4242 provides an additional voltage sensor which is internally compared to the internal 1.24 volt reference voltage. Whenever the V_{SENSE} input is below 1.24 volts, the V_{LOW} output will be driven low. An external resistor divider is used to set the desired system trip voltage.

This input can be used in two manners. The first example might be to sense unregulated DC or battery voltage in a battery powered application and to generate an interrupt in the case of either a low voltage from the battery or the failure of power in the system. The system power supply can then be designed to insure that the output capacitance is high enough to provide sufficient time to perform housekeeping tasks, such as the storing of the system status in the E²PROM, prior to the assertion of the RESET signal. (Figure 1)

The second use for this input might be to sense a second power supply level, such as 3.3 volts in a dual voltage system. In this case, the V_{LOW} output could be connected to the RESET output to generate a reset condition whenever either supply is not valid. (Figure 2)



CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition, refer to Figure 4.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 4).

DEVICE OPERATION

The S4242 is a 16K-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S4242 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver

will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 6).

The S4242 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S4242 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S4242 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S4242 will continue to transmit data. If an ACKnowledge is not detected, the S4242 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

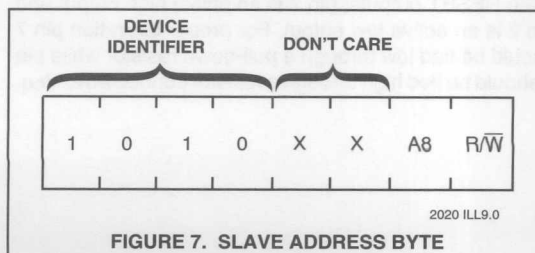
Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 7). For the S4242 this is fixed as 1010[B].

Word Address

The next two bits are don't care. The next bit is an extension of the array's address and is concatenated with the eight bits of address in the word address field, providing direct access to the 512 X 8 array.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.





WRITE OPERATIONS

The S4242 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 512 words in the array.

Upon receipt of the word address, the S4242 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S4242 begins the internal write cycle.

While the internal write cycle is in progress, the S4242 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S4242 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S4242 will respond with an ACKnowledge.

The S4242 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

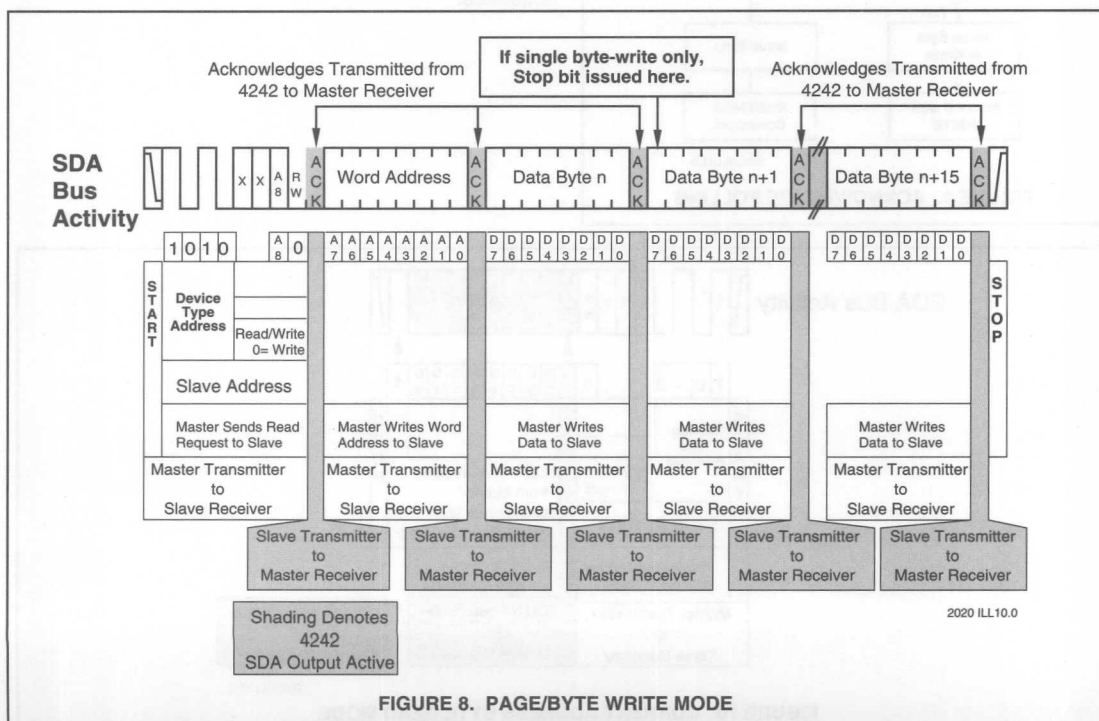


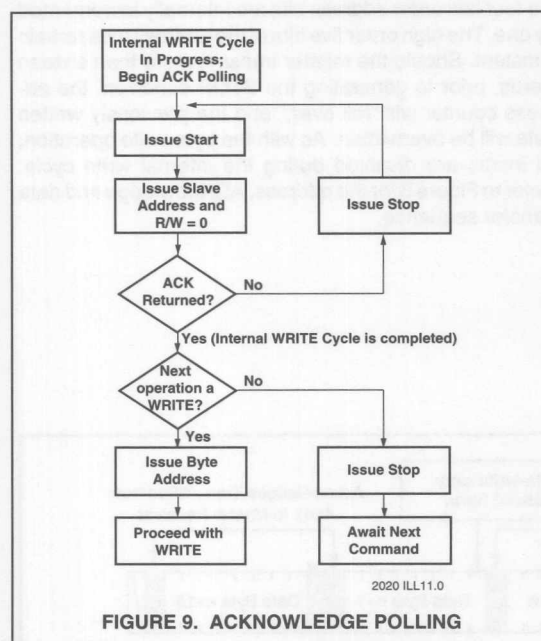
FIGURE 8. PAGE/Byte WRITE MODE



Acknowledge Polling

When the S4242 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).



READ OPERATIONS

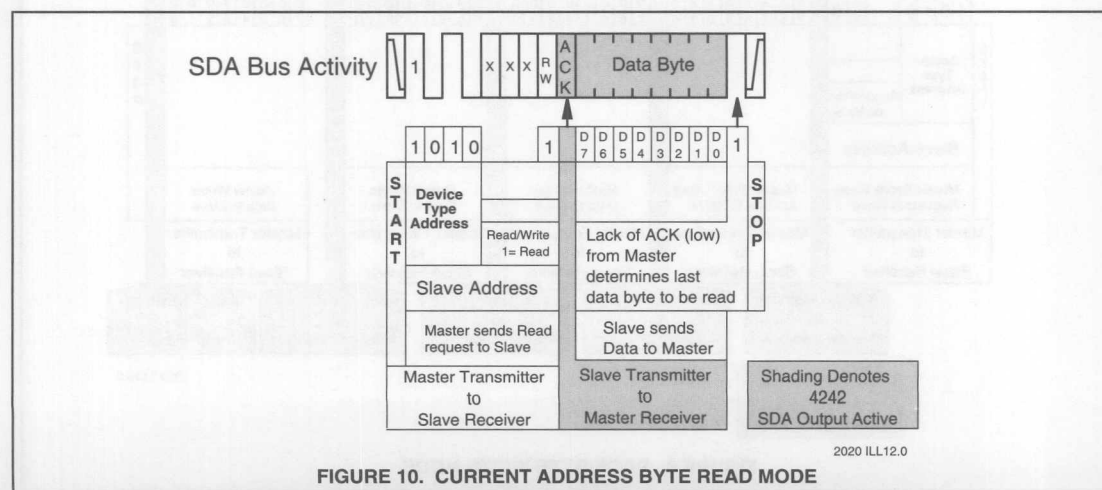
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S4242 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n , the next read operation would access data from address location $n+1$ and increment the current address pointer. When the S4242 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location $n+1$.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S4242 discontinues data transmission. See Figure 10 for the address acknowledge and data transfer sequence.

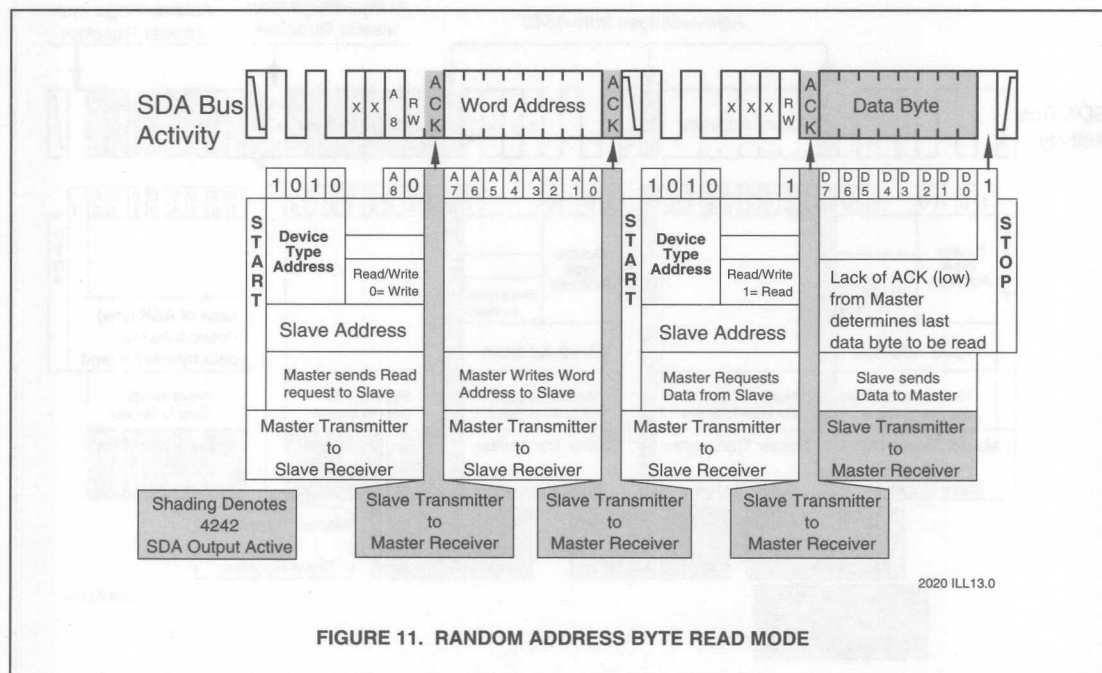




Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S4242 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S4242 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S4242 discontinues data transmission and reverts to its standby power mode. See Figure 11 for the address, acknowledge and data transfer sequence.

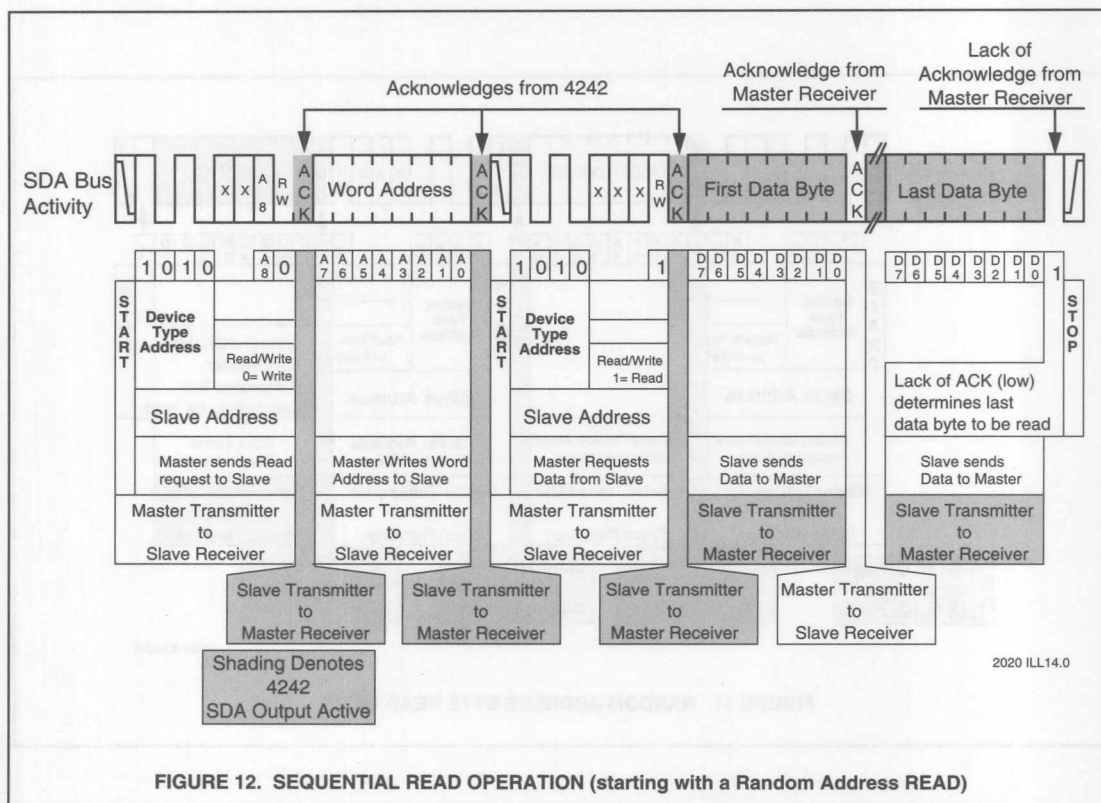




Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S4242. The S4242 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

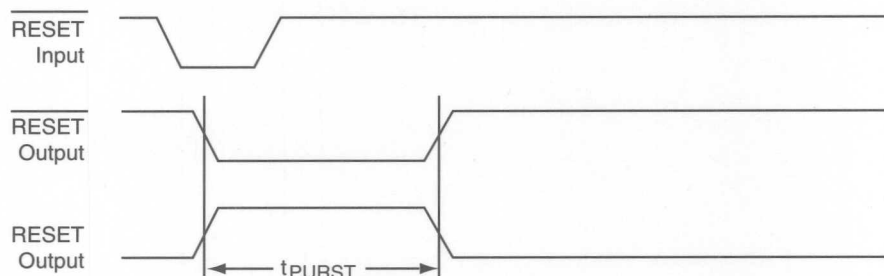
During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 12 for the address, acknowledge and data transfer sequence.





Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S4242 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



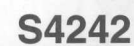
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When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL} = 100\mu A$			0.3	V
		$V_{CC} = 1.2V, I_{OL} = 100\mu A$			0.3	V
		$V_{CC} = 3.0V, I_{OL} = 500\mu A$			0.3	V
		$V_{CC} = 3.6V, I_{OL} = 500\mu A$			0.3	V
		$V_{CC} = 4.5V, I_{OL} = 750\mu A$			0.3	V
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL} = 100\mu A$			0.4	V
		$V_{CC} = 1.2V, I_{OL} = 150\mu A$			0.4	V
		$V_{CC} = 3.0V, I_{OL} = 750\mu A$			0.4	V
		$V_{CC} = 3.6V, I_{OL} = 1mA$			0.4	V
		$V_{CC} = 4.5V, I_{OL} = 1mA$			0.4	V
RESET Output Voltage	V_{OH}	$V_{CC} = 1.0V, I_{OH} = 400\mu A$	$V_{CC} - 0.75$			V
		$V_{CC} = 1.2V, I_{OH} = 800\mu A$	$V_{CC} - 0.75$			V
		$V_{CC} = 3.0V, I_{OH} = 800\mu A$	$V_{CC} - 0.5$			V
		$V_{CC} = 3.6V, I_{OH} = 800\mu A$	$V_{CC} - 0.5$			V
		$V_{CC} = 4.5V, I_{OH} = 800\mu A$	$V_{CC} - 0.5$			V

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Precision Voltage Supervisory Circuit With Watchdog Timer and 4K I²C Memory

3 and 5 Volt Systems

FEATURES

- Precision Dual Voltage Monitor
 - Automatic V_{CC} Supply Monitor
 - Dual reset outputs for complex microcontroller systems
 - Integrated memory write lockout function
 - No external components required
- Second voltage monitor output
 - Separate V_{LOW} output
 - Generates interrupt to MCU
 - Generates RESET for dual supply systems
 - Guaranteed output assertion to V_{CC} ≤ 1V
- Watchdog Timer
 - Nominal 1.6 second Timeout
- Memory Internally Organized 512K X 8
 - Two Wire Serial Interface (I²C™)
- High Reliability
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: 100 years
- 8-Pin PDIP or SOIC Packages

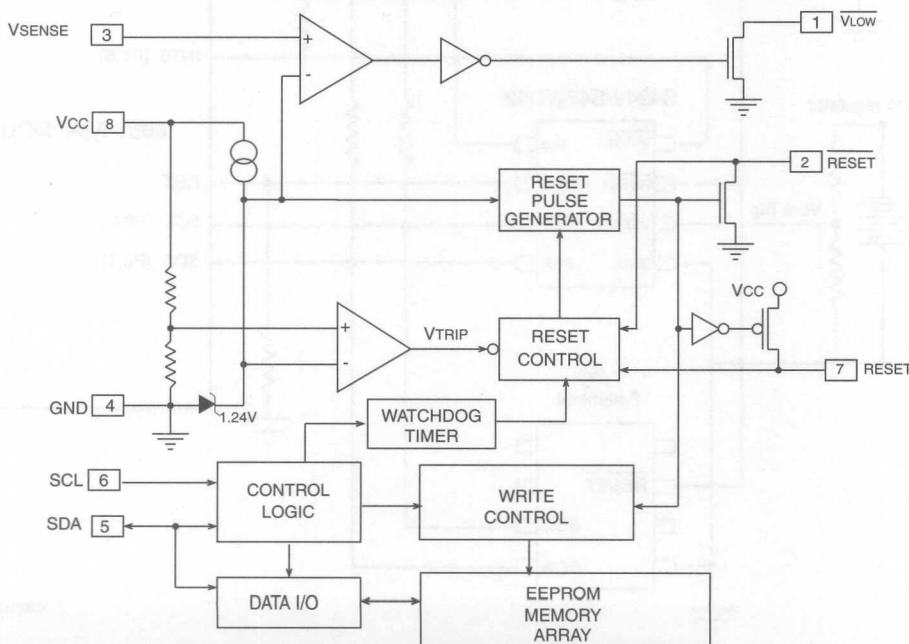
OVERVIEW

The S42WD42 is a precision power supervisory circuit. It automatically monitors the device's V_{CC} level (3V or 5V) and will generate a reset output on two complementary open drain outputs. In addition to the V_{CC} monitoring, the S42WD42 also provides a second voltage comparator input. This input has an independent open drain output that can be wire-OR'ed with the RESET I/O or it can be used as a system interrupt.

In addition to the reset circuitry, the S42WD42 also has a watchdog timer. The nominal timeout period is 1.6 seconds. If the watchdog is not cleared within 1.6 seconds it will generate a reset condition.

The S42WD42 also has an integrated 4K-bit nonvolatile memory. The memory conforms to the industry standard two-wire serial interface.

BLOCK DIAGRAM

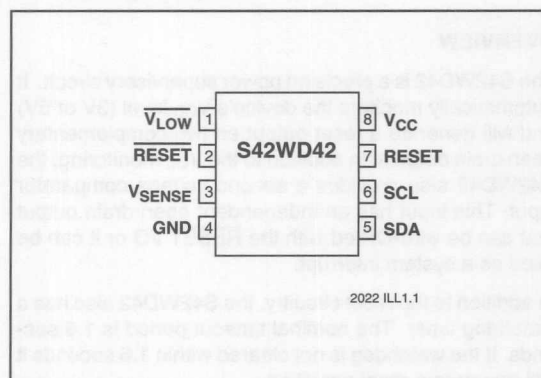


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S42WD42

PIN CONFIGURATIONS



PIN NAMES

Symbol	Pin	Description
$\overline{V_{LOW}}$	1	Open Drain Output Active When V_{SENSE} is < 1.24V
\overline{RESET}	2	Active Low \overline{RESET} Input/Output
V_{SENSE}	3	Second Monitor Voltage Input. When less than 1.24V the $\overline{V_{LOW}}$ output will be driven
GND	4	Analog and Digital Ground
SDA	5	Serial Memory Input/Output data line
SCL	6	Serial Memory clock input
RESET	7	Active High \overline{RESET} Input/Output
V_{CC}	8	Supply Voltage

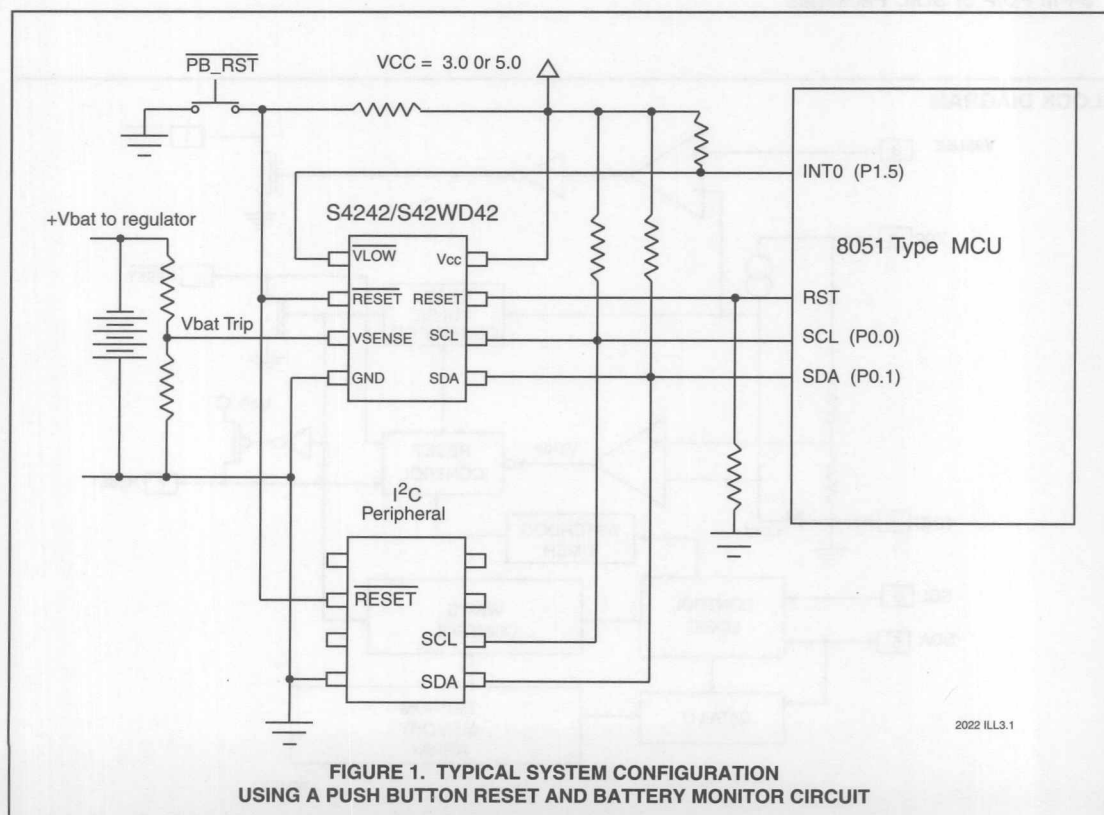
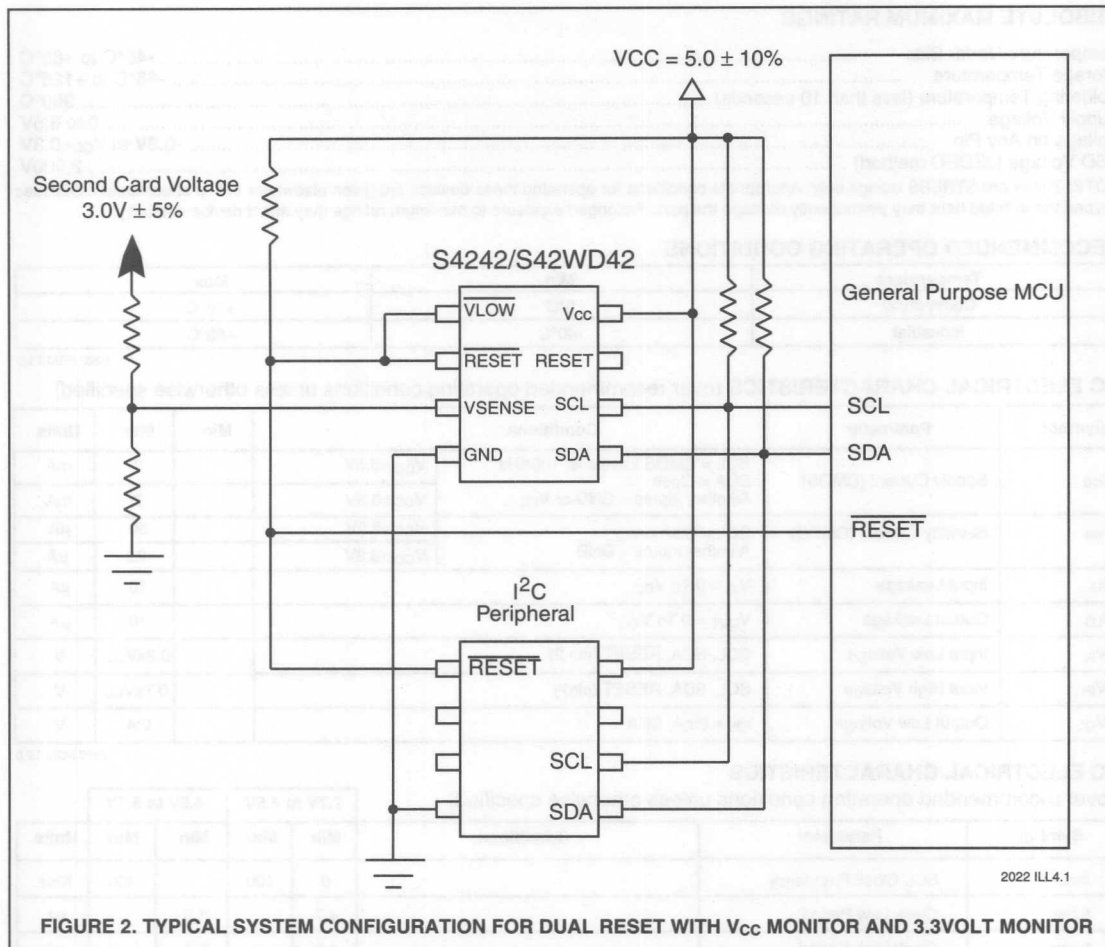


FIGURE 1. TYPICAL SYSTEM CONFIGURATION
USING A PUSH BUTTON RESET AND BATTERY MONITOR CIRCUIT



2022 ILL4.1

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I _{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V _{CC}	V _{CC} = 5.5V	3	mA
			V _{CC} = 3.3V	2	mA
I _{SB}	Standby Current (CMOS)	SCL = SDA = V _{CC} All other inputs = GND	V _{CC} = 5.5V	50	μA
			V _{CC} = 3.3V	25	μA
I _{LI}	Input Leakage	V _{IN} = 0 To V _{CC}		10	μA
I _{LO}	Output Leakage	V _{OUT} = 0 To V _{CC}		10	μA
V _{IL}	Input Low Voltage	SCL, SDA, RESET (pin 2)		0.3xV _{CC}	V
V _{IH}	Input High Voltage	SCL, SDA, RESET (pin7)		0.7xV _{CC}	V
V _{OL}	Output Low Voltage	I _{OL} = 3mA SDA		0.4	V

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AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

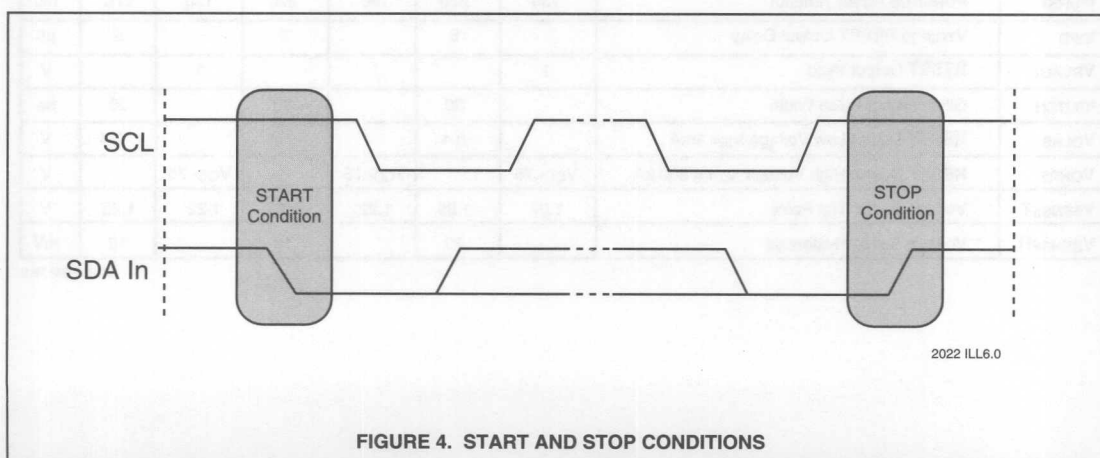
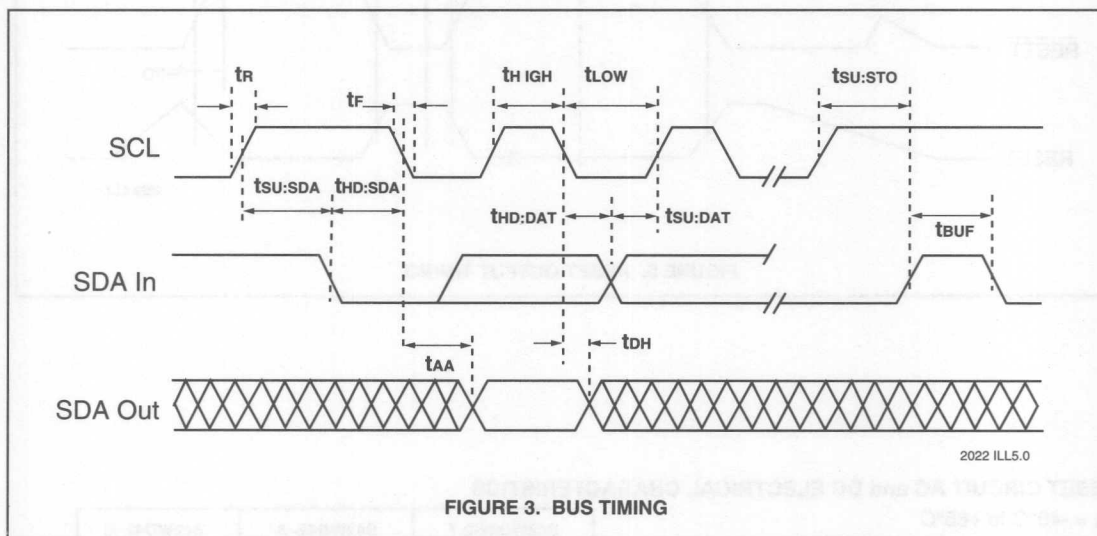
Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f _{SCL}	SCL Clock Frequency		0	100		400	KHz
t _{LOW}	Clock Low Period		4.7		1.3		μs
t _{HIGH}	Clock High Period		4.0		0.6		μs
t _{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
t _{SU:STA}	Start Condition Setup Time		4.7		0.6		μs
t _{HD:STA}	Start Condition Hold Time		4.0		0.6		μs
t _{SU:STO}	Stop Condition Setup Time		4.7		0.6		μs
t _{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t _{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t _R	SCL and SDA Rise Time			1000		300	ns
t _F	SCL and SDA Fall Time			300		300	ns
t _{SU:DAT}	Data In Setup Time		250		100		ns
t _{HD:DAT}	Data In Hold Time		0		0		ns
T _I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t _{WR}	Write Cycle Time			10		10	ms

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**CAPACITANCE** $T_A = 25^{\circ}\text{C}$, $f = 100\text{KHz}$

Symbol	Parameter	Max	Units
CIN	Input Capacitance	5	pF
COUT	Output Capacitance	8	pF

2022 PGM T4.0



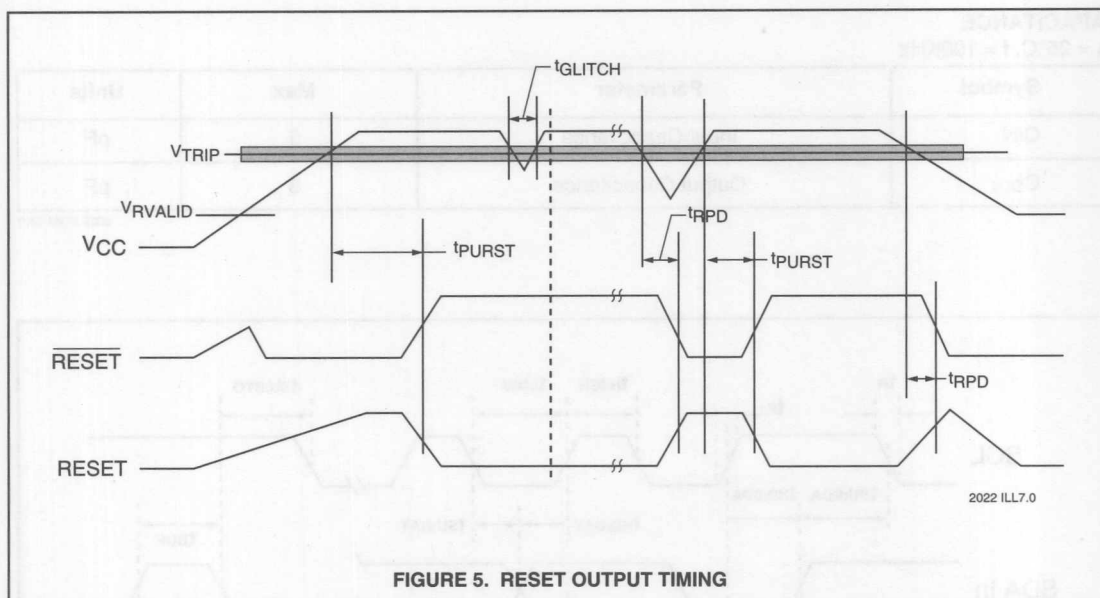


FIGURE 5. RESET OUTPUT TIMING

RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85°C

Symbol	Parameter	S42WD42-2.7		S42WD42-A		S42WD42-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
tpURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
trPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage IOL = 1mA		0.4		0.4		0.4	V
VOHRS	RESET Output High Voltage IOH = 800 μA	VCC-.75		VCC-.75		VCC-.75		V
VSENSET	Voltage Sense Trip Point	1.22	1.25	1.22	1.25	1.22	1.25	V
VSENSEH	Voltage Sense Hysteresis		10		10		10	mV

2022 PGM T5.0



PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wired with any number of open-drain or open-collector outputs.

RESET - RESET is an active low open-drain output. It should be tied high through a pull-up resistor connected to V_{CC} . RESET is an I/O, therefore it may also be used to condition a RESET signal generated by another device; it can also be used to debounce a pushbutton input.

RESET - RESET is an active high open drain (PFET) output. It should be tied low through a pull-down resistor connected to ground. RESET is an I/O, therefore it may also be used to condition a RESET signal generated by another device.

VSENSE - The VSENSE input is used as a second voltage sensing input. The pin is tied to a comparator that uses the precision internal 1.24V reference.

VLOW - The VLOW output is an open drain which is driven low whenever the VSENSE input is less than 1.24V. For correct operation this output should be tied high through a pull-up resistor connected to V_{CC} .

ENDURANCE AND DATA RETENTION

The S42WD42 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

Reset Controller Description

The S42WD42 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output. For proper operation pin 7 should be tied low through a pull-down resistor while pin 2 should be tied high through a resistor connected to V_{CC} .

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP} . The RESET outputs will be valid so long as V_{CC} is $> 1.0V$. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP} .

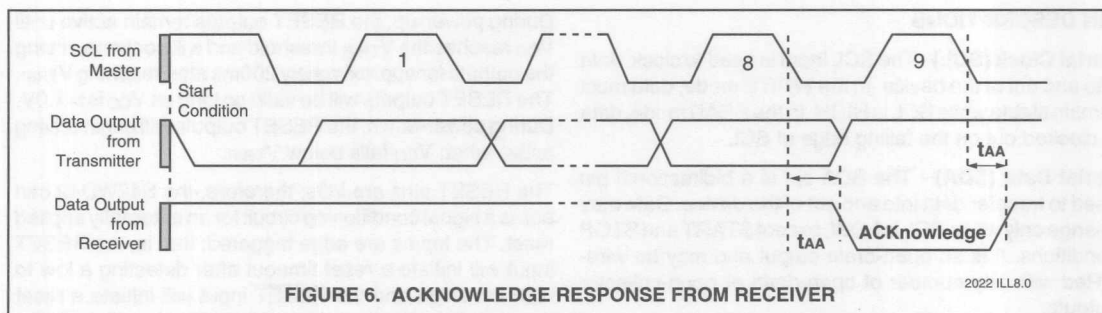
The RESET pins are I/Os; therefore, the S42WD42 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the RESET input will initiate a reset timeout after detecting a high to low transition. Refer to the applications information section for more details on device operation as a reset conditioning circuit.

Voltage Sensor Description

The S42WD42 provides an additional voltage sensor which is internally compared to the internal 1.24 volt reference voltage. Whenever the VSENSE input is below 1.24 volts, the VLOW output will be driven low. An external resistor divider is used to set the desired system trip voltage.

This input can be used in two manners. The first example might be to sense unregulated DC or battery voltage in a battery powered application and to generate an interrupt in the case of either a low voltage from the battery or the failure of power in the system. The system power supply can then be designed to insure that the output capacitance is high enough to provide sufficient time to perform housekeeping tasks, such as the storing of the system status in the E²PROM, prior to the assertion of the RESET signal. (Figure 1)

The second use for this input might be to sense a second power supply level, such as 3.3 volts in a dual voltage system. In this case, the VLOW output could be connected to the RESET output to generate a reset condition whenever either supply is not valid. (Figure 2)



CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition, refer to Figure 4.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 4).

DEVICE OPERATION

The S42WD42 is a 16K-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S42WD42 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver

will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 6).

The S42WD42 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S42WD42 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S42WD42 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S42WD42 will continue to transmit data. If an ACKnowledge is not detected, the S42WD42 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

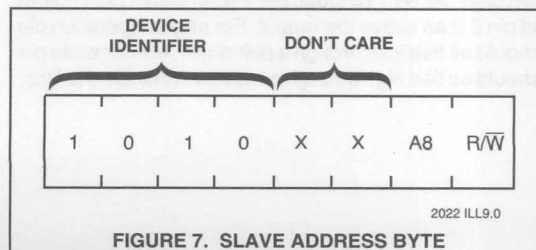
Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 7). For the S42WD42 this is fixed as 1010[B].

Word Address

The next two bits are don't care. The next bit is an extension of the array's address and is concatenated with the eight bits of address in the word address field, providing direct access to the 512 X 8 array.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.





WRITE OPERATIONS

The S42WD42 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 512 words in the array.

Upon receipt of the word address, the S42WD42 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S42WD42 begins the internal write cycle.

While the internal write cycle is in progress, the S42WD42 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S42WD42 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S42WD42 will respond with an ACKnowledge.

The S42WD42 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

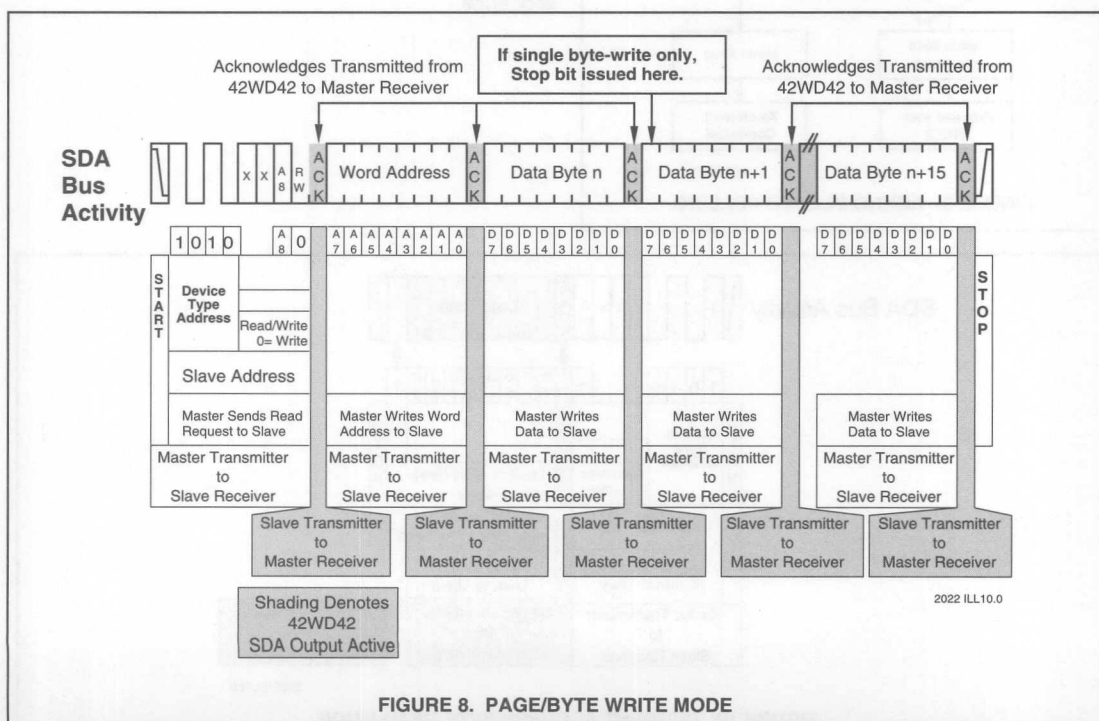


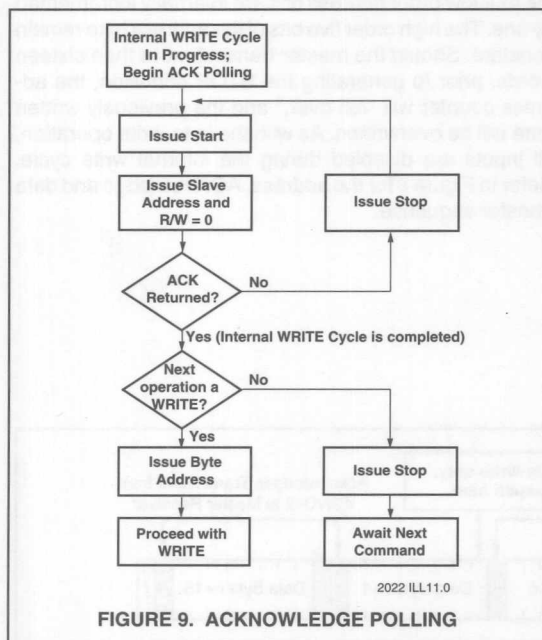
FIGURE 8. PAGE/BYTE WRITE MODE



Acknowledge Polling

When the S42WD42 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).



READ OPERATIONS

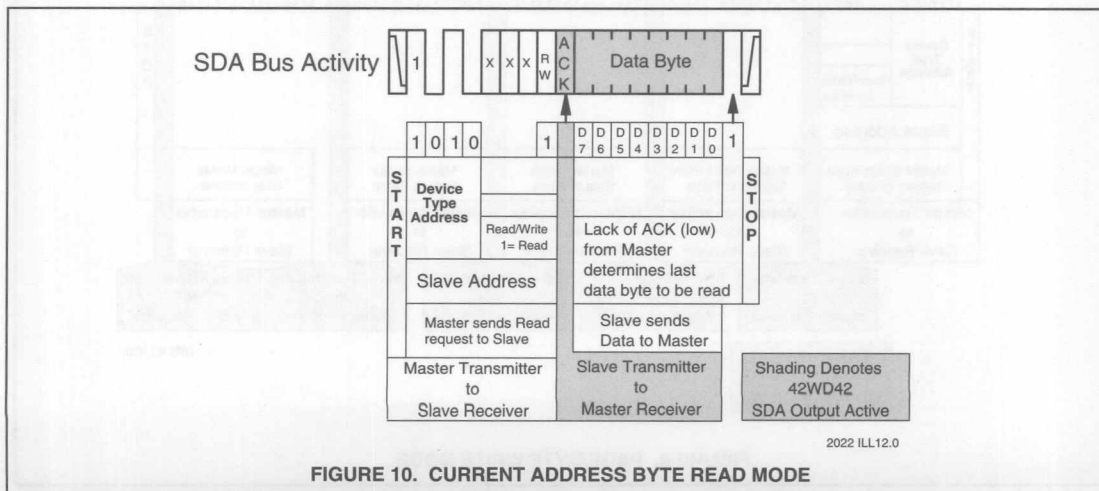
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S42WD42 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n , the next read operation would access data from address location $n+1$ and increment the current address pointer. When the S42WD42 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location $n+1$.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S42WD42 discontinues data transmission. See Figure 10 for the address acknowledge and data transfer sequence.





Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S42WD42 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S42WD42 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S42WD42 discontinues data transmission and reverts to its standby power mode. See Figure 11 for the address, acknowledge and data transfer sequence.

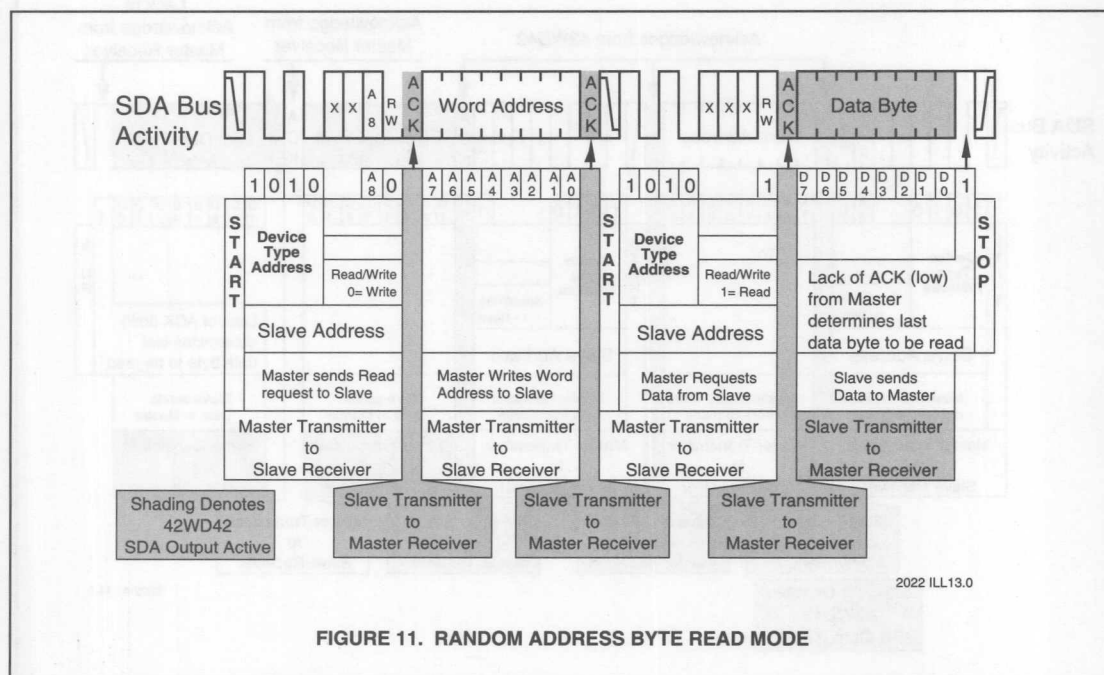


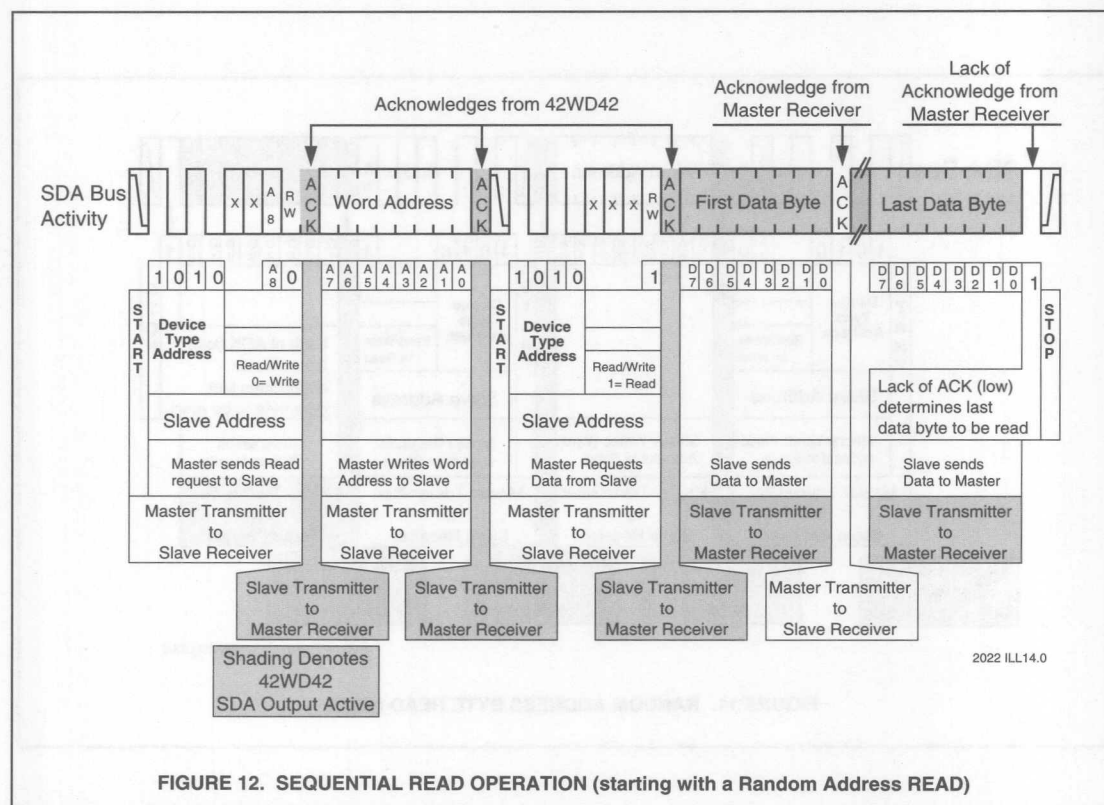
FIGURE 11. RANDOM ADDRESS BYTE READ MODE



Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S42WD42. The S42WD42 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 12 for the address, acknowledge and data transfer sequence.

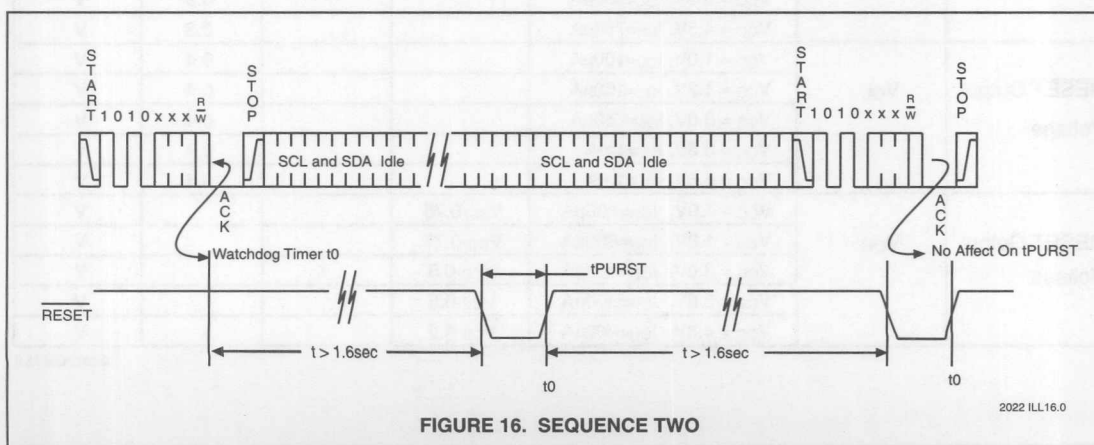
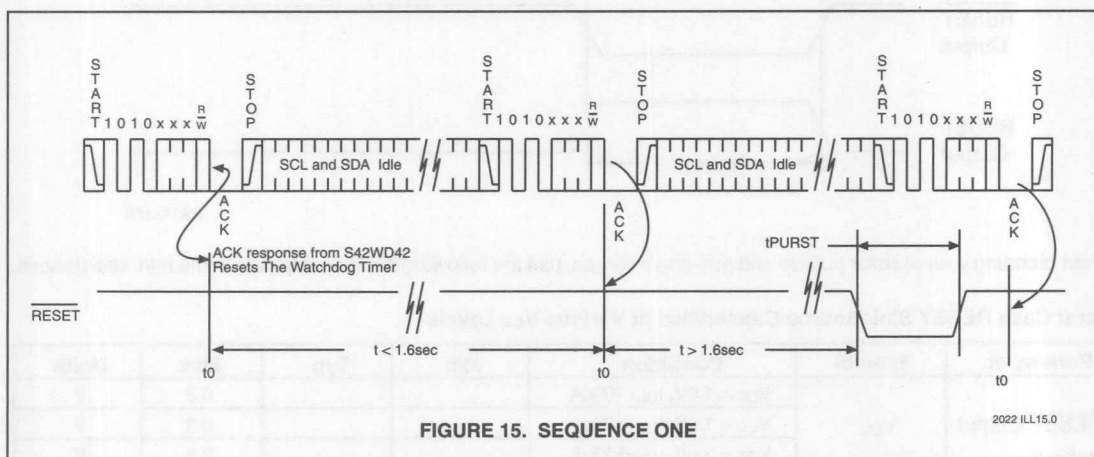




The S42WD42 has a watchdog timer with a nominal timeout period of 1.6 seconds. Whenever the watchdog times out it will generate a reset output on both $\overline{\text{RESET}}$ and RESET. The watchdog timer will reset to t_0 whenever the S42WD42 issues an ACKnowledge. Therefore, the host system will need to issue a start condition, followed by a valid address and command. It can be a normal command as in the sequence of reading or writing to the memory, or it can be a dummy command issued solely for the purpose of resetting the watchdog timer. Refer to Figure 15 for detailed sequence of operations.

If either reset input is asserted the watchdog timer will be reset and remain in the reset condition until either t_{PWRST} has expired or the reset input is released, whichever is longer.

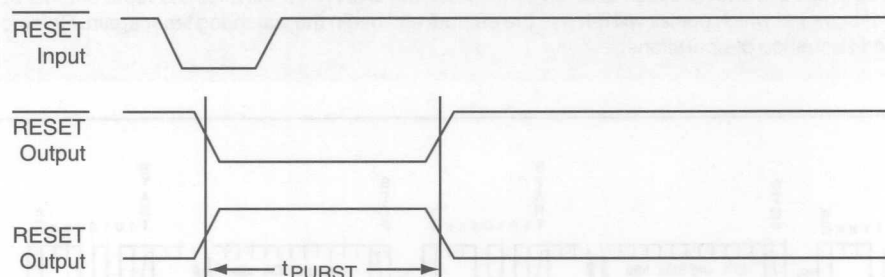
If the watchdog times out and no action is taken by the host, the S42WD42 will drive the reset outputs active for the duration of t_{PWRST} at which point it will release the outputs and begin the watchdog timer again. Refer to Figure 16 for detailed sequence of operations.





Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S42WD42 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



2022 ILL17.0

When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 1.2V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 3.0V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 3.6V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 4.5V, I_{OL}=750\mu A$			0.3	V
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.4	V
		$V_{CC} = 1.2V, I_{OL}=150\mu A$			0.4	V
		$V_{CC} = 3.0V, I_{OL}=750\mu A$			0.4	V
		$V_{CC} = 3.6V, I_{OL}=1mA$			0.4	V
		$V_{CC} = 4.5V, I_{OL}=1mA$			0.4	V
RESET Output Voltage	V_{OH}	$V_{CC} = 1.0V, I_{OH}=400\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 1.2V, I_{OH}=800\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 3.0V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 3.6V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 4.5V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V

2022 PGM T6.0

Precision Voltage Supervisory Circuit and 16K I²C Memory

3 and 5 Volt Systems

FEATURES

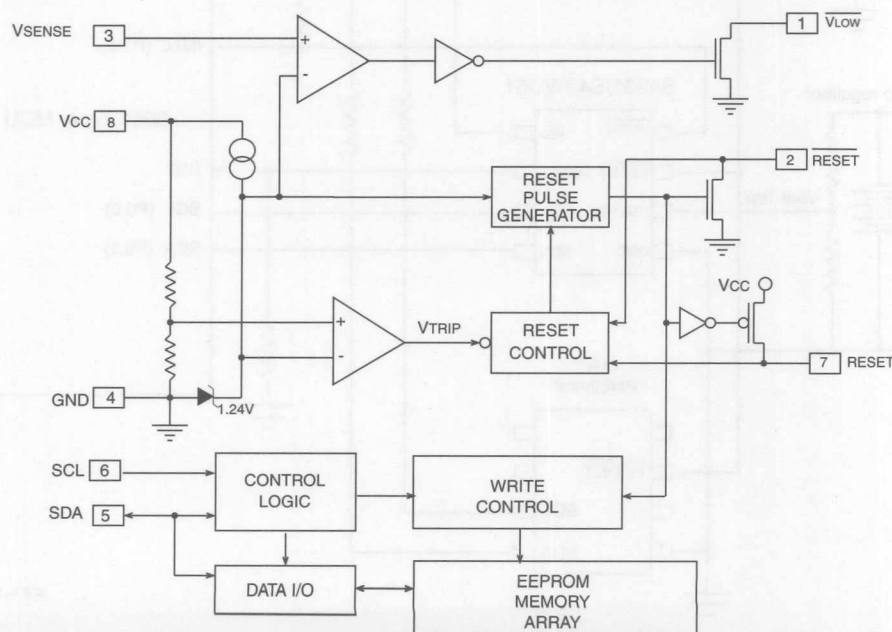
- Precision Dual Voltage Monitor
 - Automatic V_{CC} Supply Monitor
 - Dual reset outputs for complex microcontroller systems
 - Integrated memory write lockout function
 - No external components required
- Second voltage monitor output
 - Separate V_{LOW} output
 - Generates interrupt to MCU
 - Generates RESET for dual supply systems
 - Guaranteed output assertion to V_{CC} ≤ 1V
- Memory Internally Organized 2K X 8
 - Two Wire Serial Interface (I²C™)
- High Reliability
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: 100 years
- 8-Pin PDIP or SOIC Packages

OVERVIEW

The S4261 is a precision power supervisory circuit. It automatically monitors the device's V_{CC} level (3V or 5V) and will generate a reset output on two complementary open drain outputs. In addition to the V_{CC} monitoring, the S4261 also provides a second voltage comparator input. This input has an independent open drain output that can be wire-OR'ed with the $\overline{\text{RESET}}$ I/O or it can be used as a system interrupt.

The S4261 also has an integrated 16K-bit nonvolatile memory. The memory conforms to the industry standard two-wire serial interface.

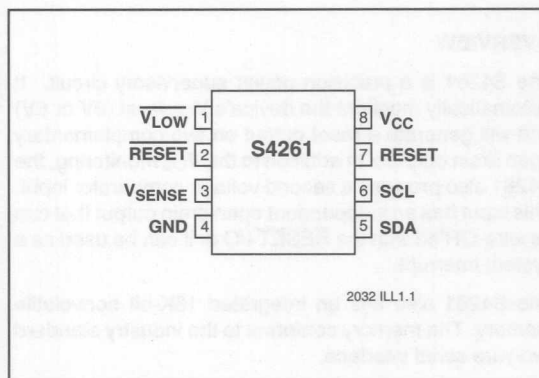
BLOCK DIAGRAM



2032 ILL2.0



PIN CONFIGURATIONS



PIN NAMES

Symbol	Pin	Description
$\overline{V_{LOW}}$	1	Open Drain Output Active When V_{SENSE} is $< 1.24V$
\overline{RESET}	2	Active Low \overline{RESET} Input/Output
V_{SENSE}	3	Second Monitor Voltage Input. When less than 1.24V the $\overline{V_{LOW}}$ output will be driven
GND	4	Analog and Digital Ground
SDA	5	Serial Memory Input/Output data line
SCL	6	Serial Memory clock input
RESET	7	Active High \overline{RESET} Input/Output
V_{CC}	8	Supply Voltage

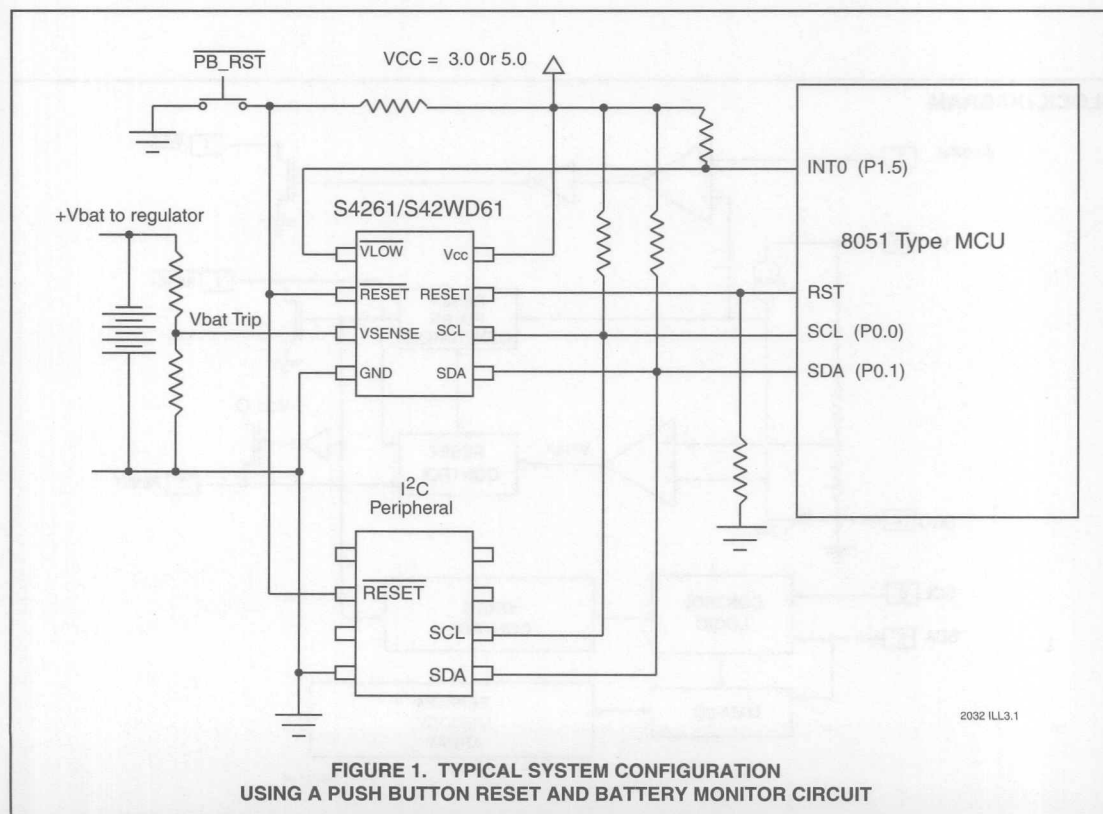
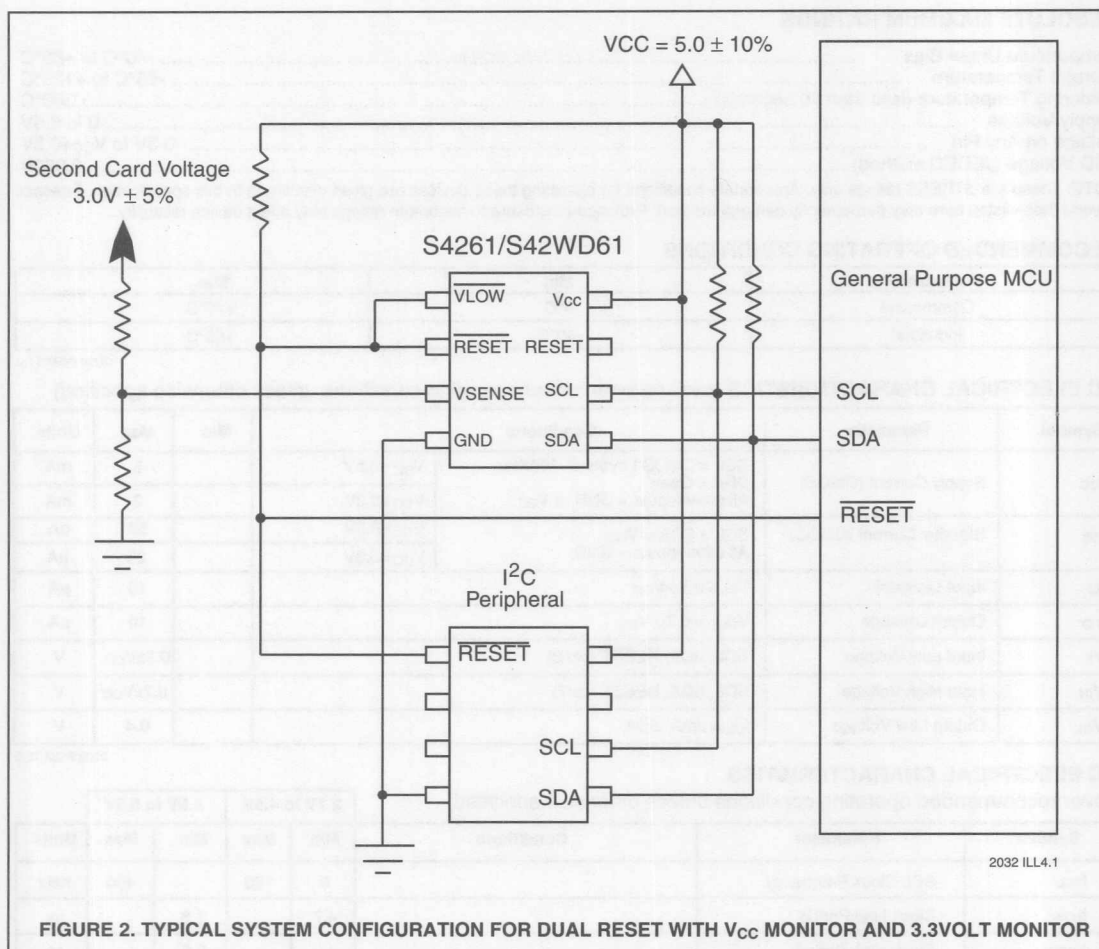


FIGURE 1. TYPICAL SYSTEM CONFIGURATION
USING A PUSH BUTTON RESET AND BATTERY MONITOR CIRCUIT



2032 ILL4.1

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

2032 PGM T1.0

DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	SCL, SDA, RESET (pin 2)		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	SCL, SDA, RESET (pin7)		$0.7 \times V_{CC}$	V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$ SDA		0.4	V

2032 PGM T2.0

AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

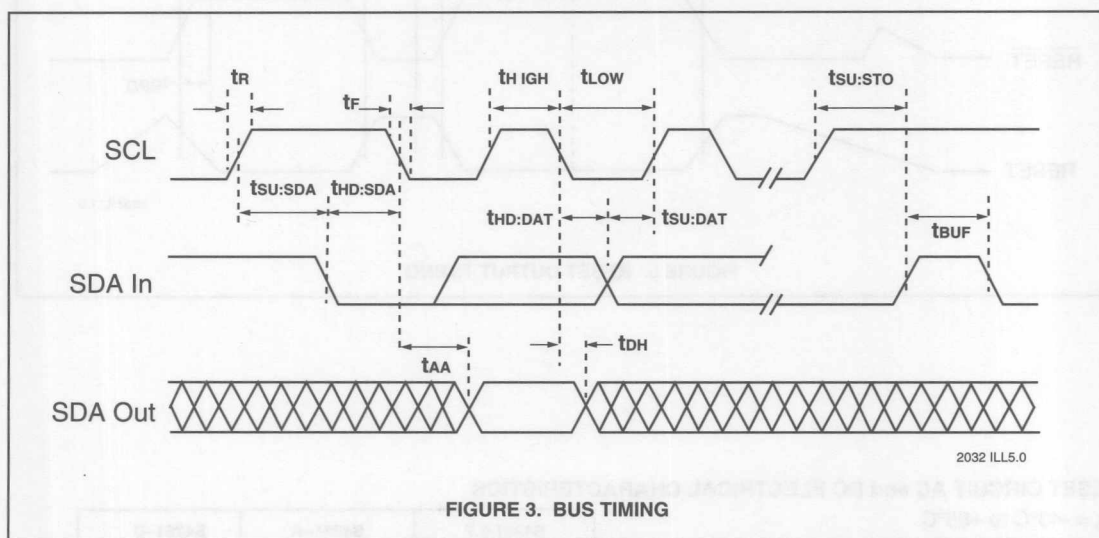
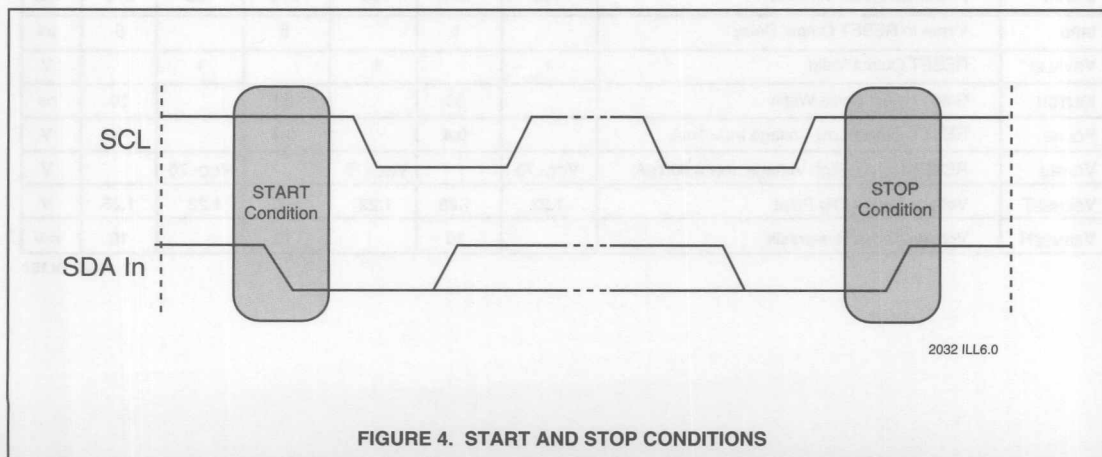
Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

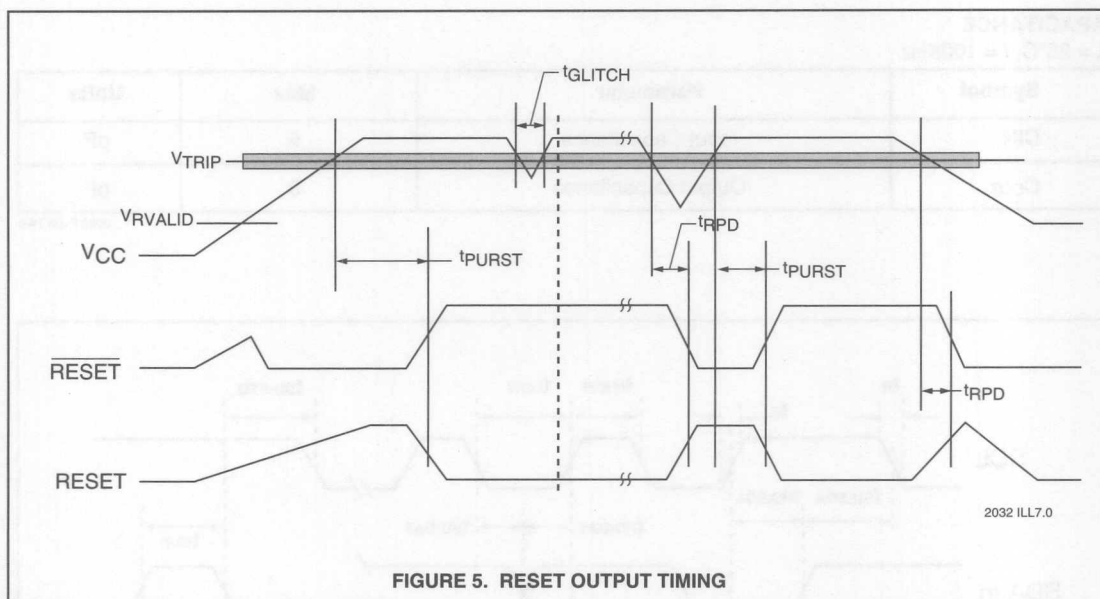
2032 PGM T3.0

**CAPACITANCE** $T_A = 25^\circ\text{C}$, $f = 100\text{KHz}$

Symbol	Parameter	Max	Units
CIN	Input Capacitance	5	pF
COUT	Output Capacitance	8	pF

2032 PGM T4.0

**FIGURE 3. BUS TIMING****FIGURE 4. START AND STOP CONDITIONS**

**RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS**T_A = -40°C to +85°C

Symbol	Parameter	S4261-2.7		S4261-A		S4261-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
tPURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
tRPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage I _{OL} = 1mA		0.4		0.4		0.4	V
VOHRS	RESET Output High Voltage I _{OH} = 800 μA	V _{CC} -.75		V _{CC} -.75		V _{CC} -.75		V
VSENSET	Voltage Sense Trip Point	1.22	1.25	1.22	1.25	1.22	1.25	V
VSENSEH	Voltage Sense Hysteresis		10		10		10	mV

2032 PGM T5.0



PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

RESET - RESET is an active low open-drain output. It should be tied high through a pull-up resistor connected to V_{CC} . RESET is an I/O, therefore it may also be used to condition a RESET signal generated by another device; it can also be used to debounce a pushbutton input.

RESET - RESET is an active high open drain (PFET) output. It should be tied low through a pull-down resistor connected to ground. RESET is an I/O, therefore it may also be used to condition a RESET signal generated by another device.

VSENSE - The VSENSE input is used as a second voltage sensing input. The pin is tied to a comparator that uses the precision internal 1.24V reference.

VLOW - The VLOW output is an open drain which is driven low whenever the VSENSE input is less than 1.24V. For correct operation this output should be tied high through a pull-up resistor connected to V_{CC} .

ENDURANCE AND DATA RETENTION

The S4261 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

Reset Controller Description

The S4261 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output. For proper operation pin 7 should be tied low through a pull-down resistor while pin 2 should be tied high through a resistor connected to V_{CC} .

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP} . The RESET outputs will be valid so long as V_{CC} is $> 1.0V$. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP} .

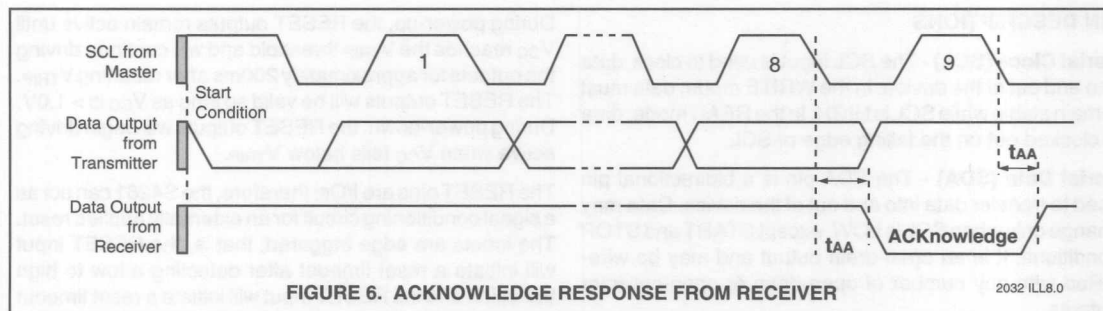
The RESET pins are I/Os; therefore, the S4261 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the RESET input will initiate a reset timeout after detecting a high to low transition. Refer to the applications information section for more details on device operation as a reset conditioning circuit.

Voltage Sensor Description

The S4261 provides an additional voltage sensor which is internally compared to the internal 1.24 volt reference voltage. Whenever the VSENSE input is below 1.24 volts, the VLOW output will be driven low. An external resistor divider is used to set the desired system trip voltage.

This input can be used in two manners. The first example might be to sense unregulated DC or battery voltage in a battery powered application and to generate an interrupt in the case of either a low voltage from the battery or the failure of power in the system. The system power supply can then be designed to insure that the output capacitance is high enough to provide sufficient time to perform housekeeping tasks, such as the storing of the system status in the E²PROM, prior to the assertion of the RESET signal. (Figure 1)

The second use for this input might be to sense a second power supply level, such as 3.3 volts in a dual voltage system. In this case, the VLOW output could be connected to the RESET output to generate a reset condition whenever either supply is not valid. (Figure 2)



CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition, refer to Figure 4.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 4).

DEVICE OPERATION

The S4261 is a 16K-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S4261 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver

will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 6).

The S4261 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S4261 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S4261 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S4261 will continue to transmit data. If an ACKnowledge is not detected, the S4261 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

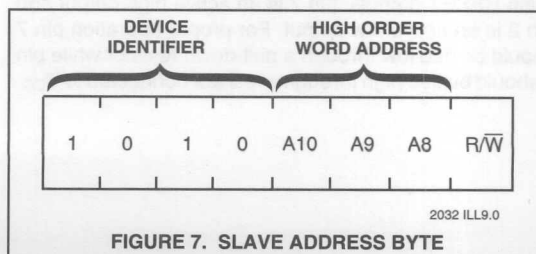
Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 7). For the S4261 this is fixed as 1010[B].

Word Address

The next three bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the 2,048 X 8 array.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.





WRITE OPERATIONS

The S4261 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 2,048 words in the array.

Upon receipt of the word address, the S4261 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S4261 begins the internal write cycle.

While the internal write cycle is in progress, the S4261 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S4261 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S4261 will respond with an ACKnowledge.

The S4261 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

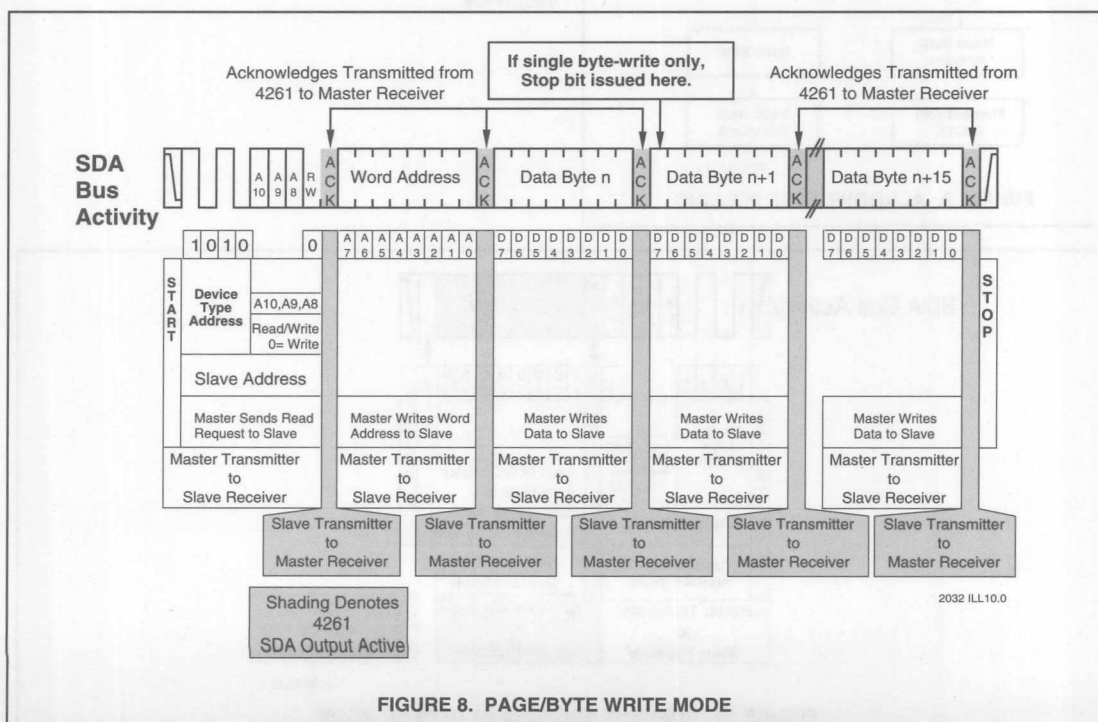
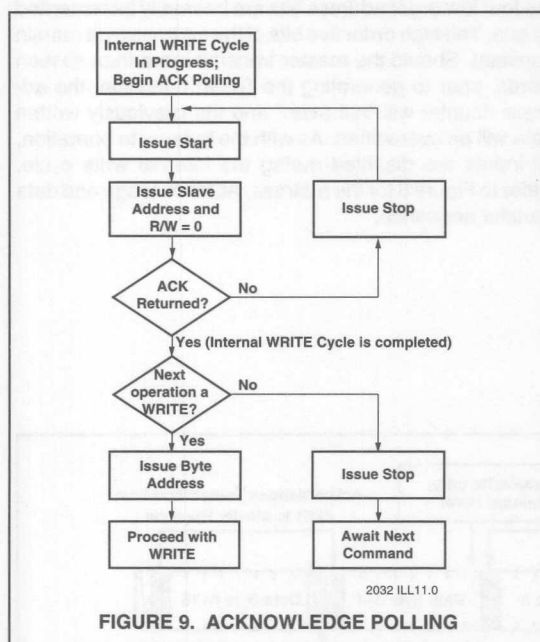


FIGURE 8. PAGE/BYTE WRITE MODE

**Acknowledge Polling**

When the S4261 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).

**READ OPERATIONS**

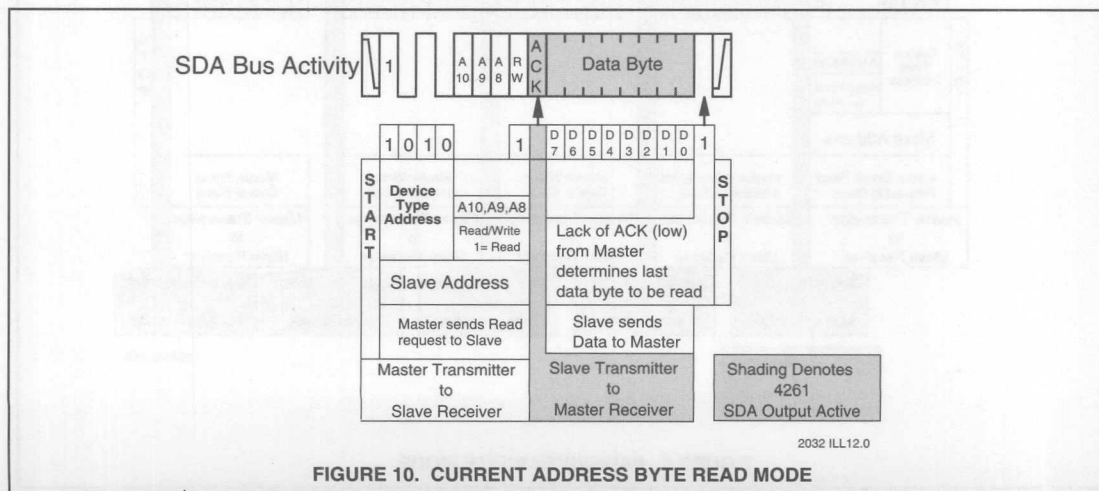
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S4261 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n , the next read operation would access data from address location $n+1$ and increment the current address pointer. When the S4261 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location $n+1$.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S4261 discontinues data transmission. See Figure 10 for the address acknowledge and data transfer sequence.

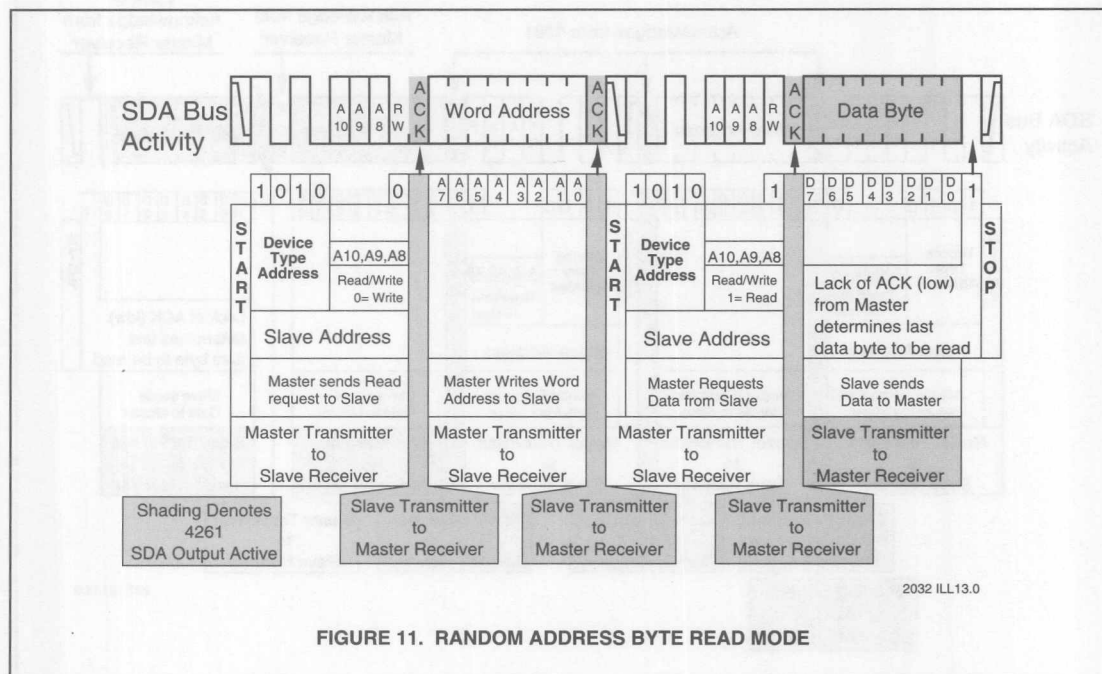




Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S4261 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S4261 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S4261 discontinues data transmission and reverts to its standby power mode. See Figure 11 for the address, acknowledge and data transfer sequence.





Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S4261. The S4261 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 12 for the address, acknowledge and data transfer sequence.

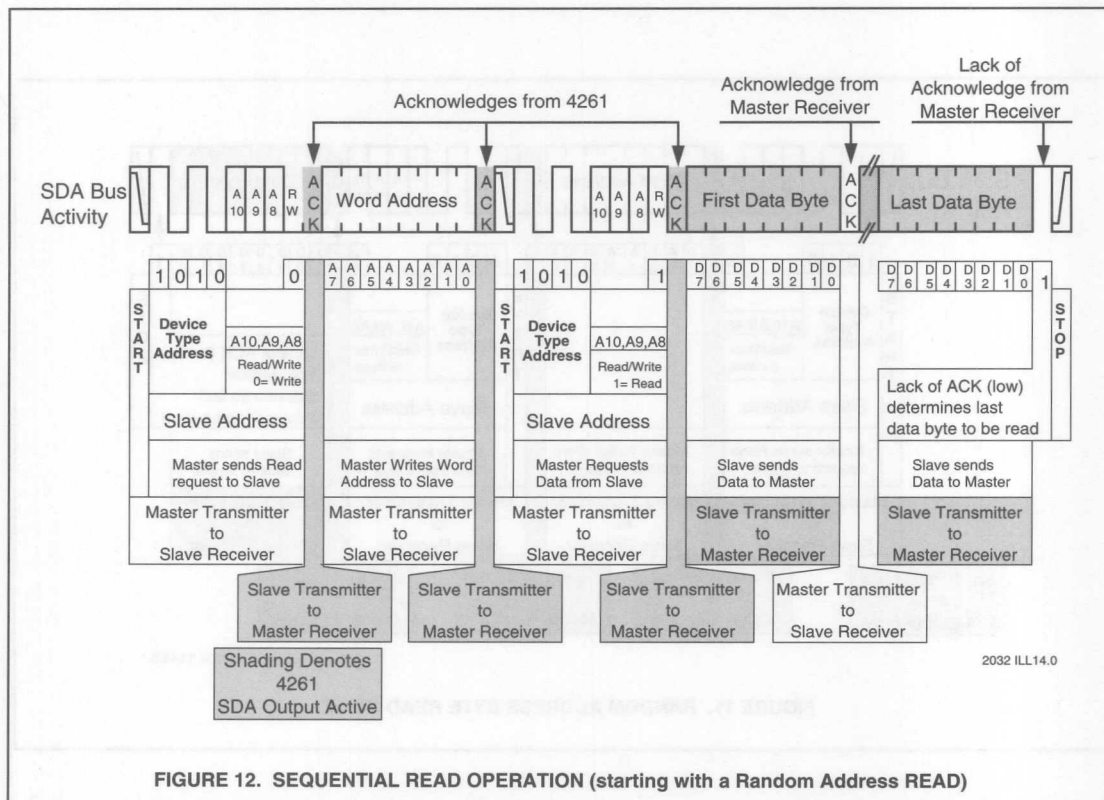
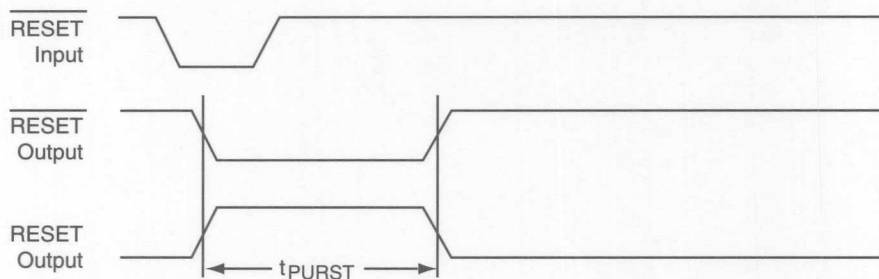


FIGURE 12. SEQUENTIAL READ OPERATION (starting with a Random Address READ)



Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S4261 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



2032 ILL15.0

When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 1.2V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 3.0V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 3.6V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 4.5V, I_{OL}=750\mu A$			0.3	V
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.4	V
		$V_{CC} = 1.2V, I_{OL}=150\mu A$			0.4	V
		$V_{CC} = 3.0V, I_{OL}=750\mu A$			0.4	V
		$V_{CC} = 3.6V, I_{OL}=1mA$			0.4	V
		$V_{CC} = 4.5V, I_{OL}=1mA$			0.4	V
RESET Output Voltage	V_{OH}	$V_{CC} = 1.0V, I_{OH}=400\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 1.2V, I_{OH}=800\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 3.0V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 3.6V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 4.5V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V

2032 PGM T6.0



The S4261 is a 16-bit, 100-MHz, 1.5-V, 1.8-V, and 2.5-V CMOS logic device. It is designed to be used in a wide range of applications, including digital signal processing, data conversion, and control systems. The device is available in a variety of packages, including 16-pin DIP, 28-pin DIP, 48-pin DIP, 64-pin DIP, 100-pin DIP, 144-pin DIP, 160-pin DIP, 208-pin DIP, 256-pin DIP, 320-pin DIP, 384-pin DIP, 448-pin DIP, 512-pin DIP, 576-pin DIP, 640-pin DIP, 704-pin DIP, 768-pin DIP, 832-pin DIP, 896-pin DIP, 960-pin DIP, 1024-pin DIP, 1088-pin DIP, 1152-pin DIP, 1216-pin DIP, 1280-pin DIP, 1344-pin DIP, 1408-pin DIP, 1472-pin DIP, 1536-pin DIP, 1600-pin DIP, 1664-pin DIP, 1728-pin DIP, 1792-pin DIP, 1856-pin DIP, 1920-pin DIP, 1984-pin DIP, 2048-pin DIP, 2112-pin DIP, 2176-pin DIP, 2240-pin DIP, 2304-pin DIP, 2368-pin DIP, 2432-pin DIP, 2496-pin DIP, 2560-pin DIP, 2624-pin DIP, 2688-pin DIP, 2752-pin DIP, 2816-pin DIP, 2880-pin DIP, 2944-pin DIP, 3008-pin DIP, 3072-pin DIP, 3136-pin DIP, 3200-pin DIP, 3264-pin DIP, 3328-pin DIP, 3392-pin DIP, 3456-pin DIP, 3520-pin DIP, 3584-pin DIP, 3648-pin DIP, 3712-pin DIP, 3776-pin DIP, 3840-pin DIP, 3904-pin DIP, 3968-pin DIP, 4032-pin DIP, 4096-pin DIP, 4160-pin DIP, 4224-pin DIP, 4288-pin DIP, 4352-pin DIP, 4416-pin DIP, 4480-pin DIP, 4544-pin DIP, 4608-pin DIP, 4672-pin DIP, 4736-pin DIP, 4800-pin DIP, 4864-pin DIP, 4928-pin DIP, 4992-pin DIP, 5056-pin DIP, 5120-pin DIP, 5184-pin DIP, 5248-pin DIP, 5312-pin DIP, 5376-pin DIP, 5440-pin DIP, 5504-pin DIP, 5568-pin DIP, 5632-pin DIP, 5696-pin DIP, 5760-pin DIP, 5824-pin DIP, 5888-pin DIP, 5952-pin DIP, 6016-pin DIP, 6080-pin DIP, 6144-pin DIP, 6208-pin DIP, 6272-pin DIP, 6336-pin DIP, 6400-pin DIP, 6464-pin DIP, 6528-pin DIP, 6592-pin DIP, 6656-pin DIP, 6720-pin DIP, 6784-pin DIP, 6848-pin DIP, 6912-pin DIP, 6976-pin DIP, 7040-pin DIP, 7104-pin DIP, 7168-pin DIP, 7232-pin DIP, 7296-pin DIP, 7360-pin DIP, 7424-pin DIP, 7488-pin DIP, 7552-pin DIP, 7616-pin DIP, 7680-pin DIP, 7744-pin DIP, 7808-pin DIP, 7872-pin DIP, 7936-pin DIP, 8000-pin DIP, 8064-pin DIP, 8128-pin DIP, 8192-pin DIP, 8256-pin DIP, 8320-pin DIP, 8384-pin DIP, 8448-pin DIP, 8512-pin DIP, 8576-pin DIP, 8640-pin DIP, 8704-pin DIP, 8768-pin DIP, 8832-pin DIP, 8896-pin DIP, 8960-pin DIP, 9024-pin DIP, 9088-pin DIP, 9152-pin DIP, 9216-pin DIP, 9280-pin DIP, 9344-pin DIP, 9408-pin DIP, 9472-pin DIP, 9536-pin DIP, 9600-pin DIP, 9664-pin DIP, 9728-pin DIP, 9792-pin DIP, 9856-pin DIP, 9920-pin DIP, 9984-pin DIP, 10048-pin DIP, 10112-pin DIP, 10176-pin DIP, 10240-pin DIP, 10304-pin DIP, 10368-pin DIP, 10432-pin DIP, 10496-pin DIP, 10560-pin DIP, 10624-pin DIP, 10688-pin DIP, 10752-pin DIP, 10816-pin DIP, 10880-pin DIP, 10944-pin DIP, 11008-pin DIP, 11072-pin DIP, 11136-pin DIP, 11200-pin DIP, 11264-pin DIP, 11328-pin DIP, 11392-pin DIP, 11456-pin DIP, 11520-pin DIP, 11584-pin DIP, 11648-pin DIP, 11712-pin DIP, 11776-pin DIP, 11840-pin DIP, 11904-pin DIP, 11968-pin DIP, 12032-pin DIP, 12096-pin DIP, 12160-pin DIP, 12224-pin DIP, 12288-pin DIP, 12352-pin DIP, 12416-pin DIP, 12480-pin DIP, 12544-pin DIP, 12608-pin DIP, 12672-pin DIP, 12736-pin DIP, 12800-pin DIP, 12864-pin DIP, 12928-pin DIP, 12992-pin DIP, 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**Precision Voltage Supervisory Circuit
With Watchdog Timer and 16K I²C Memory**

3 and 5 Volt Systems

FEATURES

- **Precision Dual Voltage Monitor**
 - Automatic V_{CC} Supply Monitor
 - Dual reset outputs for complex microcontroller systems
 - Integrated memory write lockout function
 - No external components required
- **Second voltage monitor output**
 - Separate V_{LOW} output
 - Generates interrupt to MCU
 - Generates RESET for dual supply systems
 - Guaranteed output assertion to V_{CC} ≤ 1V
- **Watchdog Timer**
 - Nominal 1.6 second Timeout
- **Memory Internally Organized 2K X 8**
 - Two Wire Serial Interface (I²C™)
- **High Reliability**
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: 100 years
- **8-Pin PDIP or SOIC Packages**

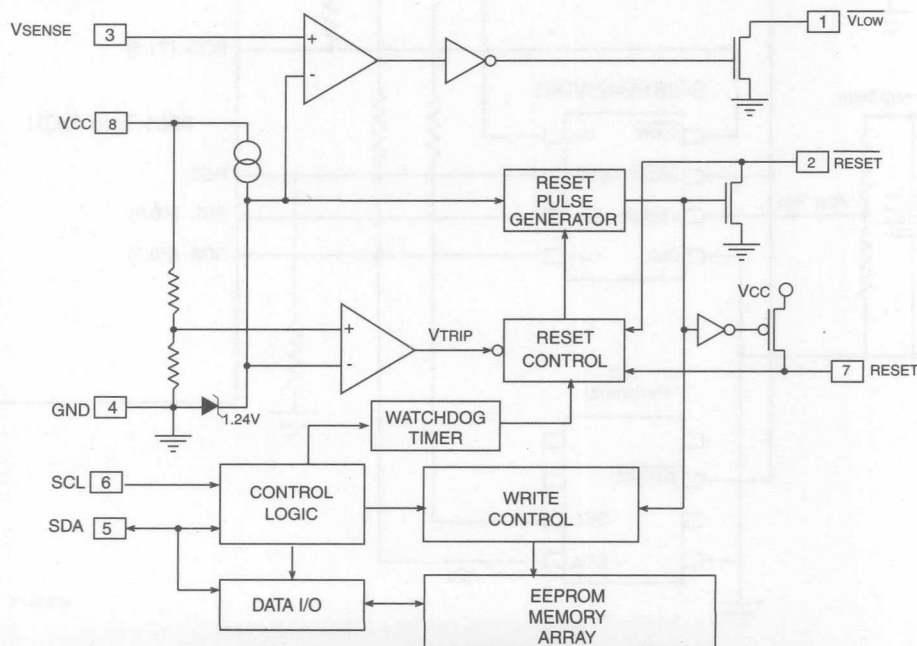
OVERVIEW

The S42WD61 is a precision power supervisory circuit. It automatically monitors the device's V_{CC} level (3V or 5V) and will generate a reset output on two complementary open drain outputs. In addition to the V_{CC} monitoring, the S42WD61 also provides a second voltage comparator input. This input has an independent open drain output that can be wire-OR'ed with the RESET I/O or it can be used as a system interrupt.

In addition to the reset circuitry, the S42WD61 also has a watchdog timer. The nominal timeout period is 1.6 seconds. If the watchdog is not cleared within 1.6 seconds it will generate a reset condition.

The S42WD61 also has an integrated 16K-bit nonvolatile memory. The memory conforms to the industry standard two-wire serial interface.

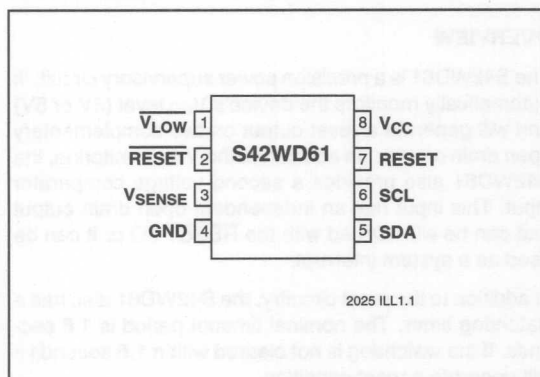
BLOCK DIAGRAM





S42WD61

PIN CONFIGURATIONS



PIN NAMES

Symbol	Pin	Description
$\overline{V_{LOW}}$	1	Open Drain Output Active When V_{SENSE} is < 1.24V
RESET	2	Active Low RESET Input/Output
V_{SENSE}	3	Second Monitor Voltage Input. When less than 1.24V the $\overline{V_{LOW}}$ output will be driven
GND	4	Analog and Digital Ground
SDA	5	Serial Memory Input/Output data line
SCL	6	Serial Memory clock input
RESET	7	Active High RESET Input/Output
V _{CC}	8	Supply Voltage

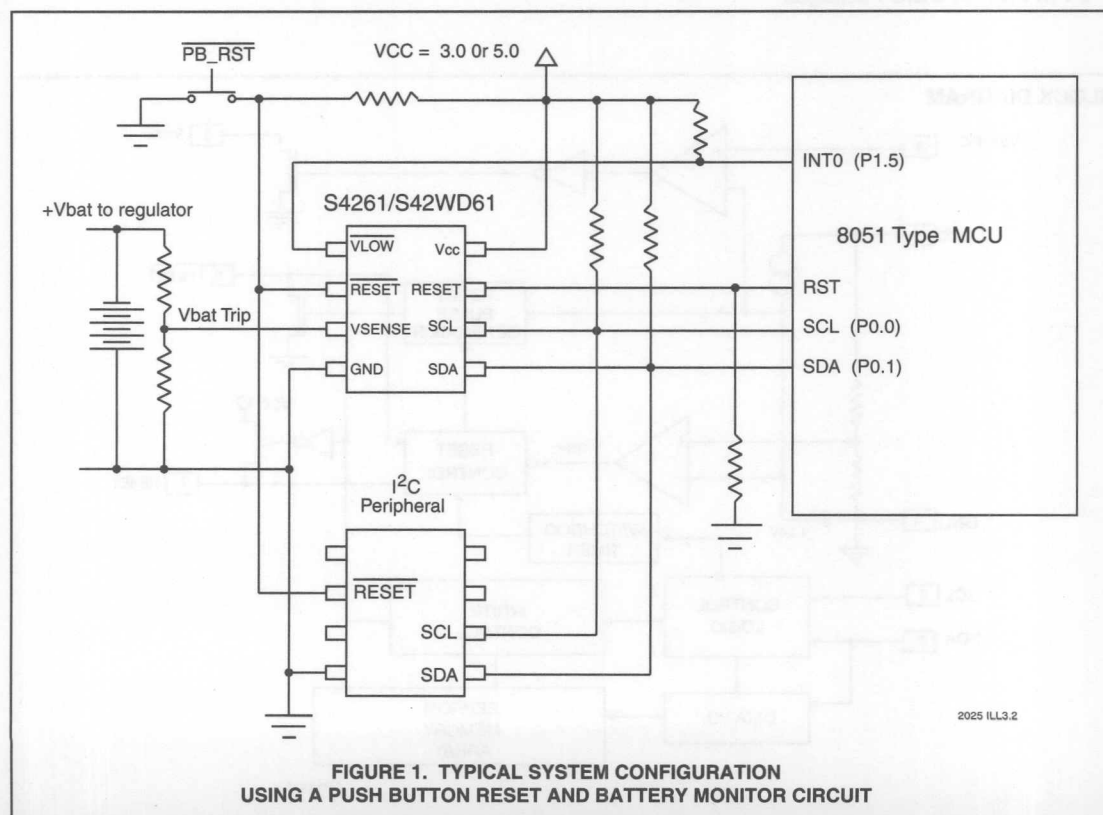


FIGURE 1. TYPICAL SYSTEM CONFIGURATION USING A PUSH BUTTON RESET AND BATTERY MONITOR CIRCUIT



**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

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DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	SCL, SDA, RESET (pin 2)		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	SCL, SDA, RESET (pin 7)		$0.7 \times V_{CC}$	V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$ SDA		0.4	V

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AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

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CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 100\text{KHz}$

Symbol	Parameter	Max	Units
CIN	Input Capacitance	5	pF
COUT	Output Capacitance	8	pF

2025 PGM T4.0

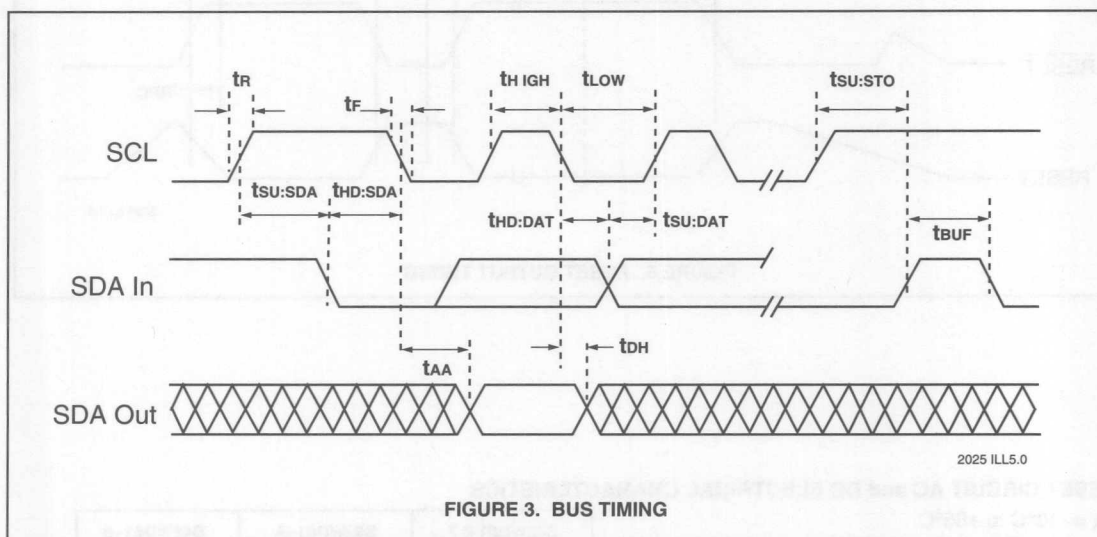


FIGURE 3. BUS TIMING

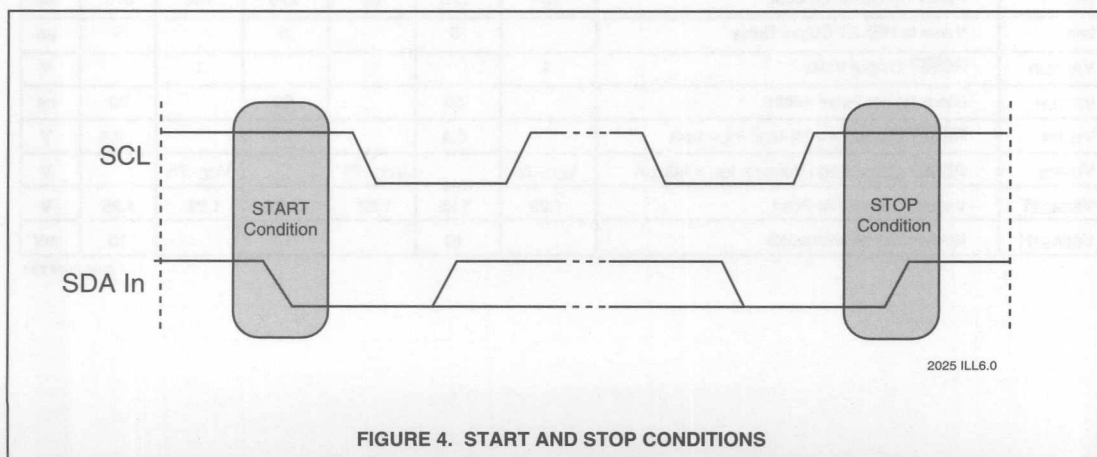
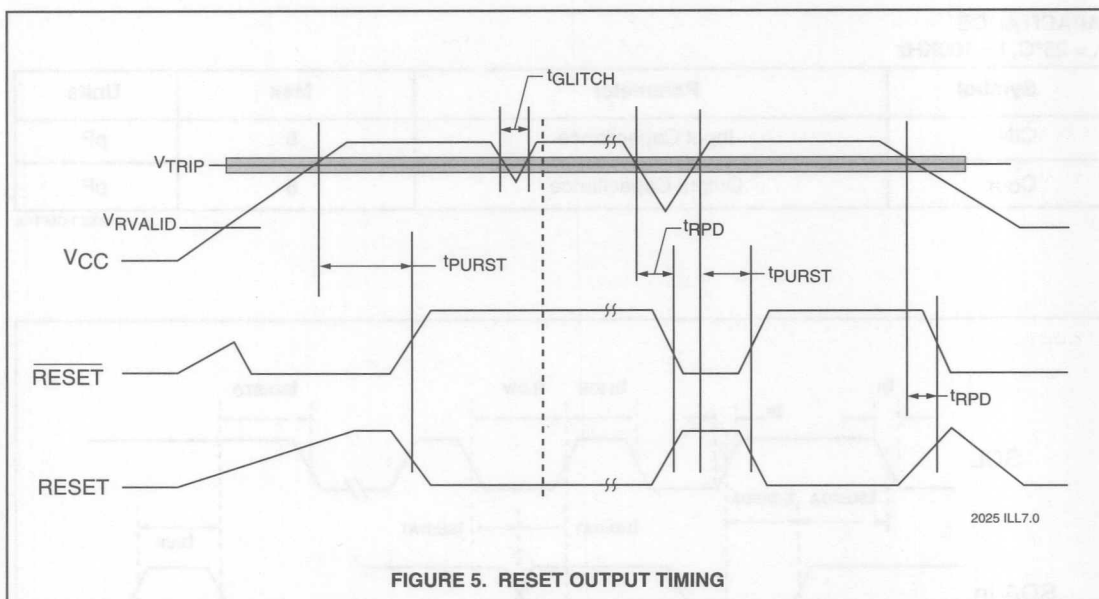


FIGURE 4. START AND STOP CONDITIONS

**FIGURE 5. RESET OUTPUT TIMING****RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS**

TA = -40°C to +85°C

Symbol	Parameter	S42WD61-2.7		S42WD61-A		S42WD61-B		Unit
		Min	Max	Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
tpURST	Power-Up Reset Timeout	130	270	130	270	130	270	ms
trPD	VTRIP to RESET Output Delay		5		5		5	μs
VRVALID	RESET Output Valid	1		1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30		30	ns
VOLRS	RESET Output Low Voltage IOL = 1mA		0.4		0.4		0.4	V
VOHRS	RESET Output High Voltage IOH = 800 μA	VCC-.75		VCC-.75		VCC-.75		V
VSENSET	Voltage Sense Trip Point	1.22	1.25	1.22	1.25	1.22	1.25	V
VSENSEH	Voltage Sense Hysteresis		10		10		10	mV

2025 PGM T5.1



PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

RESET - $\overline{\text{RESET}}$ is an active low open-drain output. It should be tied high through a pull-up resistor connected to V_{CC} . $\overline{\text{RESET}}$ is an I/O, therefore it may also be used to condition a RESET signal generated by another device; it can also be used to debounce a pushbutton input.

RESET - RESET is an active high open drain (PFET) output. It should be tied low through a pull-down resistor connected to ground. RESET is an I/O, therefore it may also be used to condition a RESET signal generated by another device.

VSENSE - The V_{SENSE} input is used as a second voltage sensing input. The pin is tied to a comparator that uses the precision internal 1.24V reference.

V_{LOW} - The V_{LOW} output is an open drain which is driven low whenever the V_{SENSE} input is less than 1.24V. For correct operation this output should be tied high through a pull-up resistor connected to V_{CC} .

ENDURANCE AND DATA RETENTION

The S42WD61 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

Reset Controller Description

The S42WD61 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output. For proper operation pin 7 should be tied low through a pull-down resistor while pin 2 should be tied high through a resistor connected to V_{CC} .

During power-up, the RESET outputs remain active until V_{CC} reaches the V_{TRIP} threshold and will continue driving the outputs for approximately 200ms after reaching V_{TRIP} . The RESET outputs will be valid so long as V_{CC} is $> 1.0V$. During power-down, the RESET outputs will begin driving active when V_{CC} falls below V_{TRIP} .

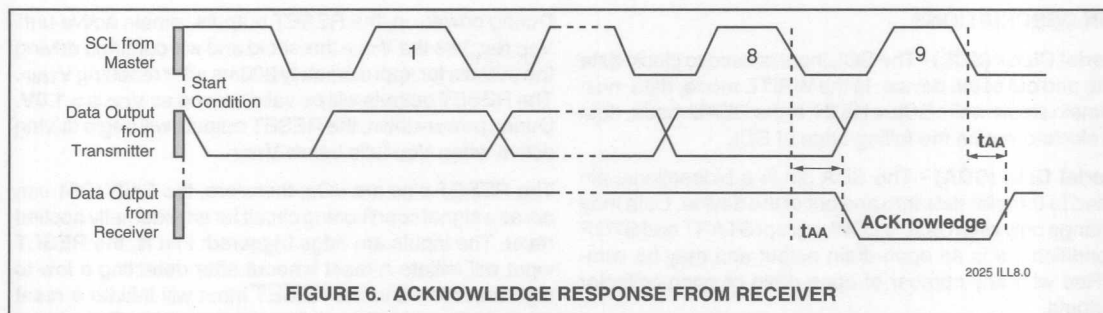
The RESET pins are I/Os; therefore, the S42WD61 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the RESET input will initiate a reset timeout after detecting a high to low transition. Refer to the applications information section for more details on device operation as a reset conditioning circuit.

Voltage Sensor Description

The S42WD61 provides an additional voltage sensor which is internally compared to the internal 1.24 volt reference voltage. Whenever the V_{SENSE} input is below 1.24 volts, the V_{LOW} output will be driven low. An external resistor divider is used to set the desired system trip voltage.

This input can be used in two manners. The first example might be to sense unregulated DC or battery voltage in a battery powered application and to generate an interrupt in the case of either a low voltage from the battery or the failure of power in the system. The system power supply can then be designed to insure that the output capacitance is high enough to provide sufficient time to perform housekeeping tasks, such as the storing of the system status in the E^2 PROM, prior to the assertion of the RESET signal. (Figure 1)

The second use for this input might be to sense a second power supply level, such as 3.3 volts in a dual voltage system. In this case, the V_{LOW} output could be connected to the $\overline{\text{RESET}}$ output to generate a reset condition whenever either supply is not valid. (Figure 2)



CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition, refer to Figure 4.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 4).

DEVICE OPERATION

The S42WD61 is a 16K-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S42WD61 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver

will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 6).

The S42WD61 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S42WD61 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S42WD61 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S42WD61 will continue to transmit data. If an ACKnowledge is not detected, the S42WD61 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

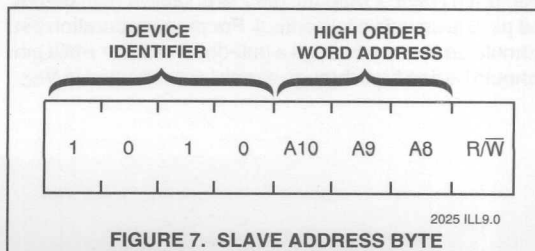
Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 7). For the S42WD61 this is fixed as 1010[B].

Word Address

The next three bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the 2,048 X 8 array.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.





WRITE OPERATIONS

The S42WD61 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 2,048 words in the array.

Upon receipt of the word address, the S42WD61 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S42WD61 begins the internal write cycle.

While the internal write cycle is in progress, the S42WD61 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S42WD61 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S42WD61 will respond with an ACKnowledge.

The S42WD61 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 8 for the address, ACKnowledge and data transfer sequence.

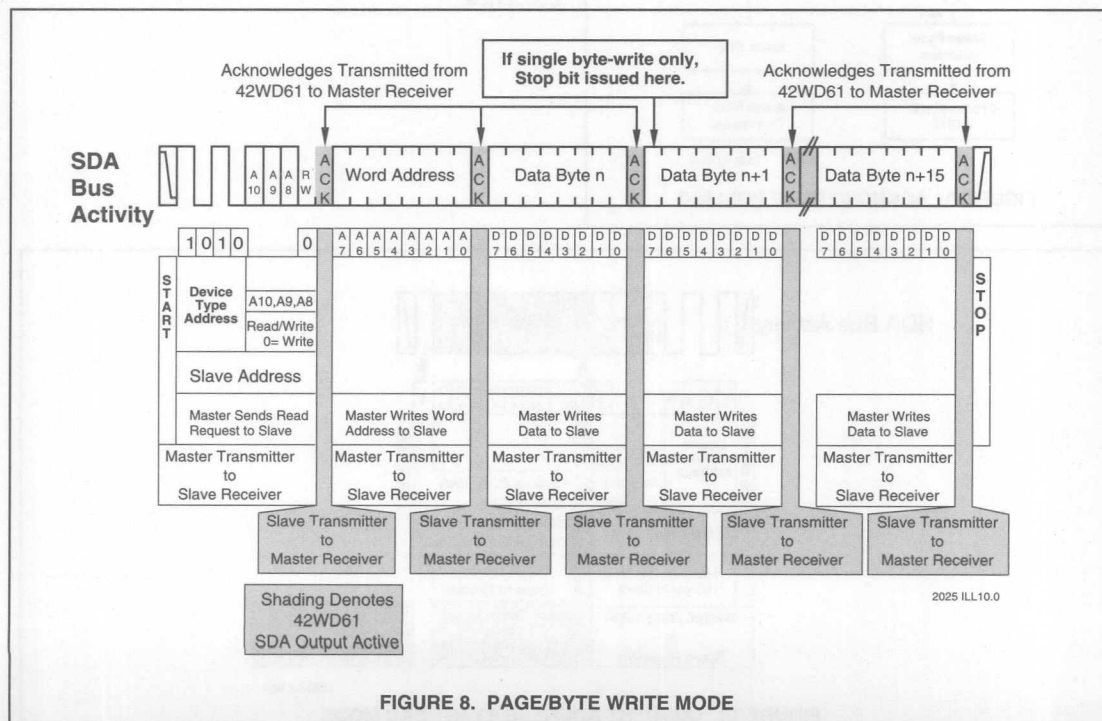


FIGURE 8. PAGE/BYTE WRITE MODE



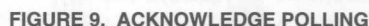
READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S42WD61 discontinues data transmission. See Figure 10 for the address acknowledge and data transfer sequence.

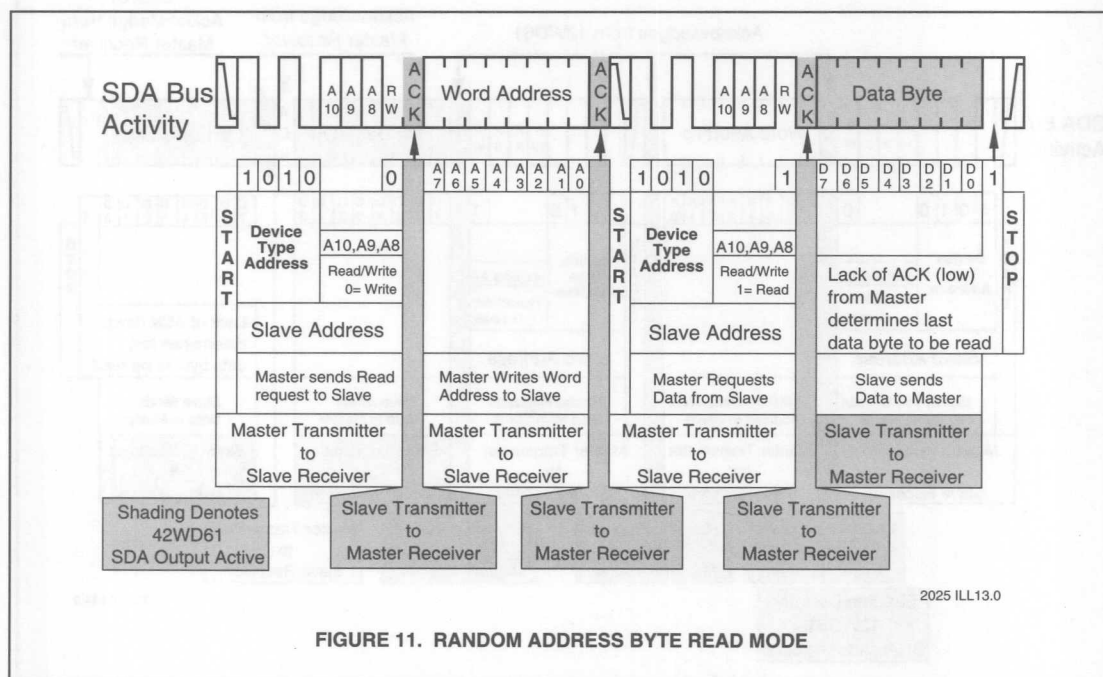




Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S42WD61 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S42WD61 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S42WD61 discontinues data transmission and reverts to its standby power mode. See Figure 11 for the address, acknowledge and data transfer sequence.





Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S42WD61. The S42WD61 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 12 for the address, acknowledge and data transfer sequence.

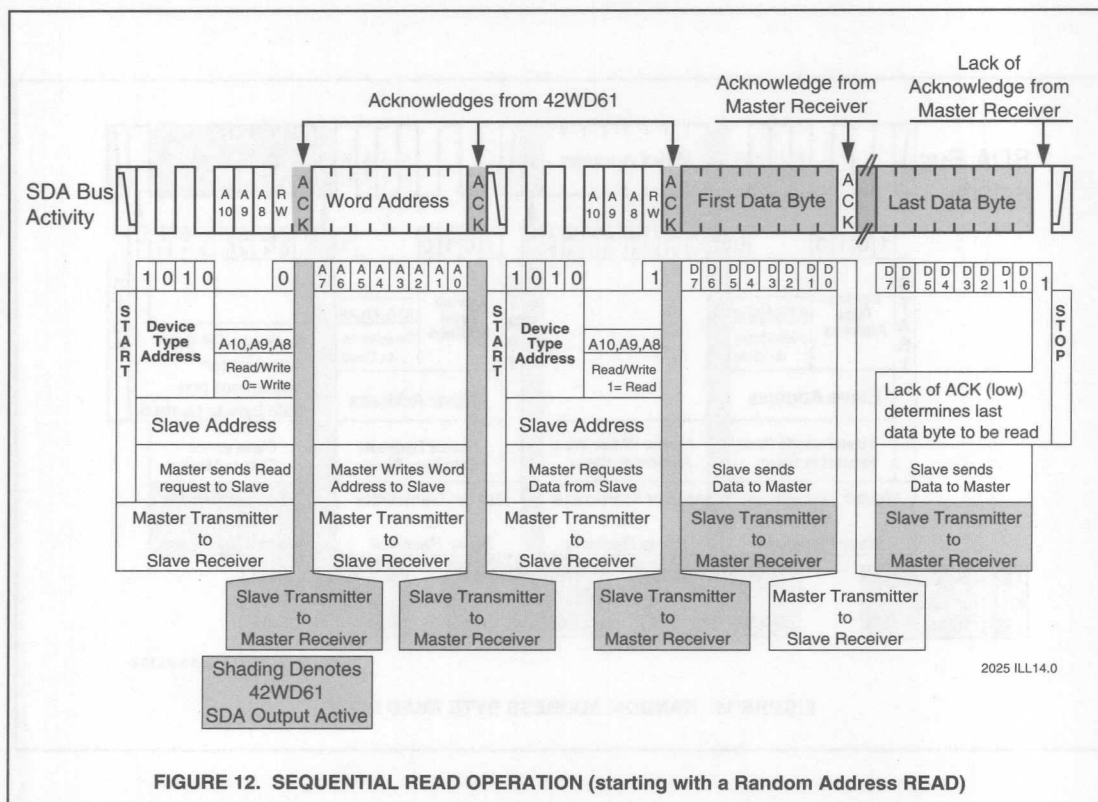


FIGURE 12. SEQUENTIAL READ OPERATION (starting with a Random Address READ)



Watchdog Timer Operation

The S42WD61 has a watchdog timer with a nominal timeout period of 1.6 seconds. Whenever the watchdog times out it will generate a reset output on both $\overline{\text{RESET}}$ and RESET. The watchdog timer will reset to t_0 whenever the S42WD61 issues an ACKnowledge. Therefore, the host system will need to issue a start condition, followed by a valid address and command. It can be a normal command as in the sequence of reading or writing to the memory, or it can be a dummy command issued solely for the purpose of resetting the watchdog timer. Refer to Figure 15 for detailed sequence of operations.

The watchdog timer will be held in the reset state during power-on while V_{CC} is less than V_{TRIP} . Once V_{CC} exceeds V_{TRIP} , the watchdog will continue to be held in a reset state for the duration of t_{PURST} . After t_{PURST} , the timer will be released and begin counting.

If either reset input is asserted the watchdog timer will be reset and remain in the reset condition until either t_{PURST} has expired or the reset input is released, whichever is longer.

If the watchdog times out and no action is taken by the host, the S42WD61 will drive the reset outputs active for the duration of t_{PURST} at which point it will release the outputs and begin the watchdog timer again. Refer to Figure 16 for detailed sequence of operations.

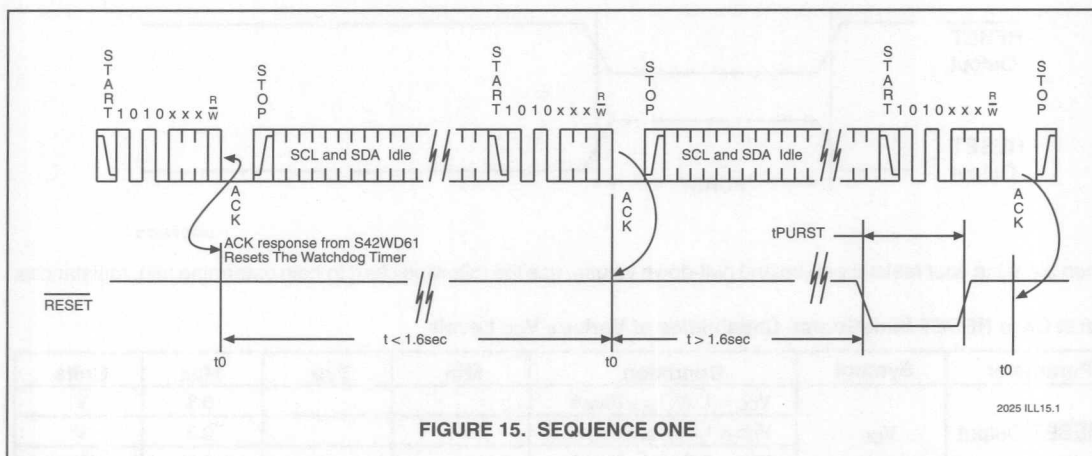


FIGURE 15. SEQUENCE ONE

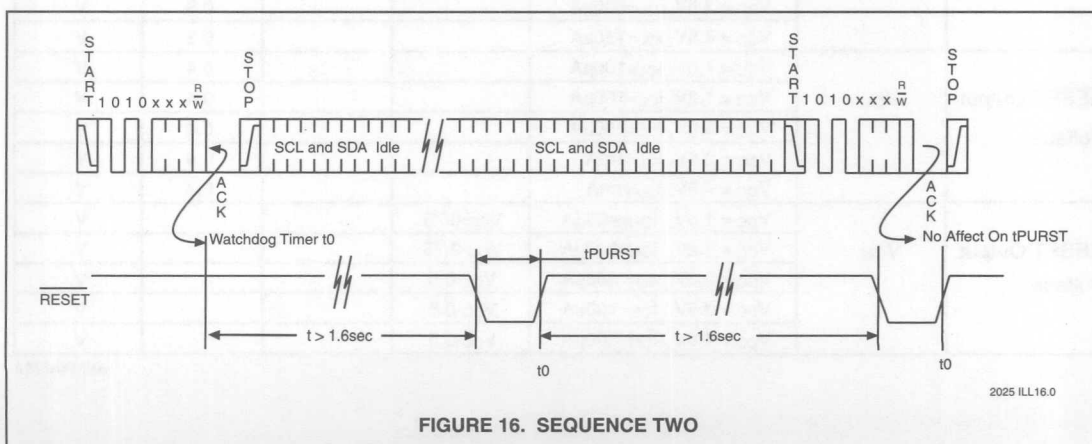
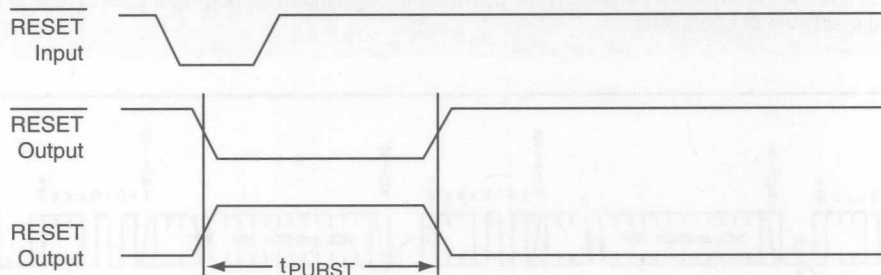


FIGURE 16. SEQUENCE TWO



Frequently the reset controller will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the S42WD61 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than t_{PURST} . The same reset output affect can be attained by using the active high reset input.



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When planning your resistor pull-up and pull-down values, use the following chart to help determine min. resistances.

Worst Case RESET Sink/Source Capabilities at Various V_{CC} Levels

Parameter	Symbol	Condition	Min	Typ	Max	Units
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 1.2V, I_{OL}=100\mu A$			0.3	V
		$V_{CC} = 3.0V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 3.6V, I_{OL}=500\mu A$			0.3	V
		$V_{CC} = 4.5V, I_{OL}=750\mu A$			0.3	V
RESET Output Voltage	V_{OL}	$V_{CC} = 1.0V, I_{OL}=100\mu A$			0.4	V
		$V_{CC} = 1.2V, I_{OL}=150\mu A$			0.4	V
		$V_{CC} = 3.0V, I_{OL}=750\mu A$			0.4	V
		$V_{CC} = 3.6V, I_{OL}=1mA$			0.4	V
		$V_{CC} = 4.5V, I_{OL}=1mA$			0.4	V
RESET Output Voltage	V_{OH}	$V_{CC} = 1.0V, I_{OH}=400\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 1.2V, I_{OH}=800\mu A$	$V_{CC}-0.75$			V
		$V_{CC} = 3.0V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 3.6V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V
		$V_{CC} = 4.5V, I_{OH}=800\mu A$	$V_{CC}-0.5$			V

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SECTION 7 **Voltage Supervisory Circuits**

SMS1223 Voltage Supervisory Circuit	7-3
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Virginia Department of Transportation

Section

Section

**+5V and +3V Low Power Voltage Supervisory Circuits
with Adjustable Secondary Sense Circuit and Watchdog**

Advance Information

FEATURES

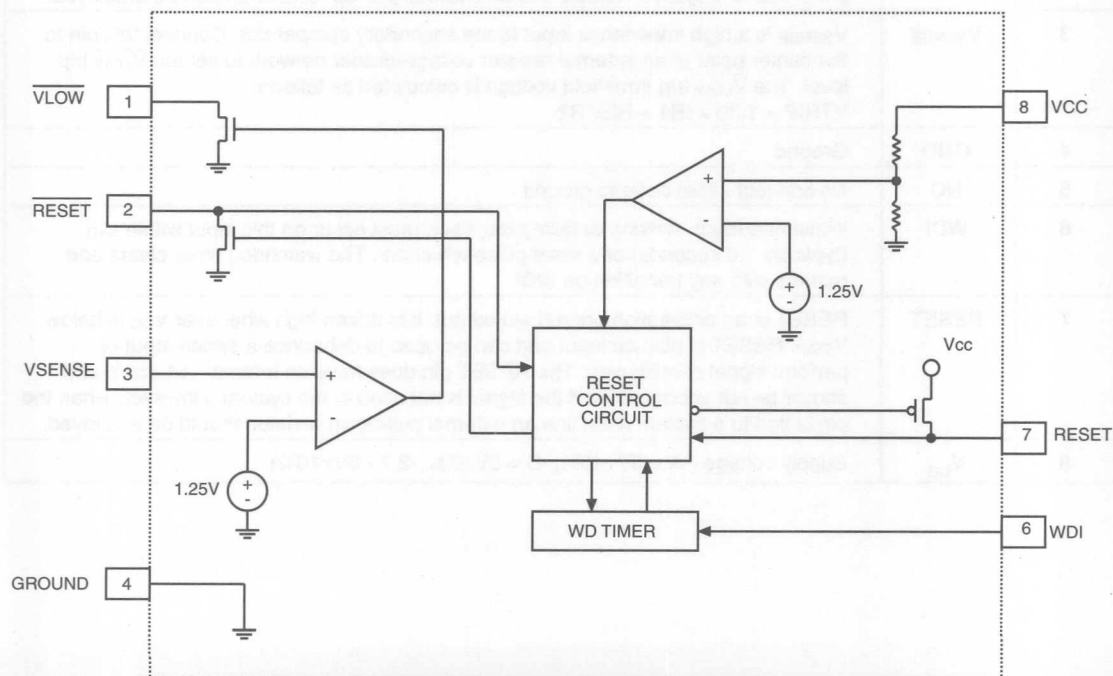
- Precision V_{CC} Monitor Circuit
- Three Operating Voltage Options
 - +5V \pm 10% Supply
 - +5V \pm 5% Supply
 - +3V \pm 10% Supply
- Complementary reset outputs
- Guaranteed assertion of reset outputs at or above $V_{CC}=1V$
- Secondary user adjustable monitor
- Comparator reference 1.25V
- Open drain output
- Watchdog timeout period 1.6 seconds

OVERVIEW

The SMS1223 voltage supervisory circuit provides monitor and control activities for a MPU's or MCU's supply voltage, either a 5V or 3V supply. Whenever V_{CC} is below V_{TRIP} the SMS1223 will drive the complementary reset outputs.

Additional features include a watchdog and a second user adjustable voltage monitor input. The output from this second sensor can either be wire-OR'ed with the RESET I/O or tied to a system interrupt.

FUNCTIONAL BLOCK DIAGRAM



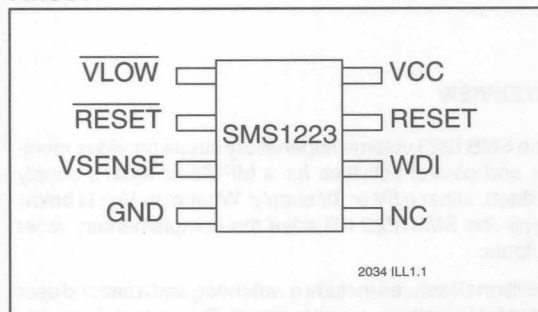
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SMS1223

Advance Information

PINOUT



PIN NAMES

Pin	Name	Function
1	$\overline{V_{LOW}}$	$\overline{V_{LOW}}$ is an active low open drain output. It is driven low whenever the V_{SENSE} input is less than 1.25V. $\overline{V_{LOW}}$ does have an internal pull-up resistor
2	\overline{RESET}	\overline{RESET} is an active low open drain output. It is driven low whenever V_{CC} is below V_{TRIP} . \overline{RESET} is also an input and can be used to debounce a switch input or perform signal conditioning. The \overline{RESET} pin does have an internal pull-up and should be left unconnected if the signal is not used in the system. However, when the pin is tied to a system \overline{RESET} line an external pull-up resistor should be employed.
3	V_{SENSE}	V_{SENSE} is a high impedance input to the secondary comparator. Connect this pin to the center point of an external resistor voltage-divider network to set the $\overline{V_{LOW}}$ trip level. The $\overline{V_{LOW}}$ trip threshold voltage is calculated as follows: $V_{TRIP} = 1.26 \times (R1 + R2) / R2$
4	GND	Ground
5	NC	No connect - float or tie to ground
6	WDI	Watchdog Input. A rising or falling transition must occur on this input within two (typically 1.6 seconds) or a reset pulse will occur. The watchdog timer clears and restarts with any transition on WDI.
7	RESET	RESET is an active high open drain output. It is driven high whenever V_{CC} is below V_{TRIP} . RESET is also an input and can be used to debounce a switch input or perform signal conditioning. The RESET pin does have an internal pull-down and should be left unconnected if the signal is not used in the system. However, when the pin is tied to a system reset line an external pull-down resistor should be employed.
8	V_{CC}	Supply voltage (-A = $5V \pm 10\%$, -B = $5V \pm 5\%$, -2.7 - $3V \pm 10\%$)



SECTION 8 **Data Conversion Products**

S9408 Quad 8-bit Nonvolatile DACPOT™	8-3
S9418 Quad 8-bit Nonvolatile DACPOT™ with a Mute Control Input	8-11
SMD1102/SMD1103 2-Channel and 3-Channel, 10-bit Auto-Monitor Data Acquisition System	8-19
S9318 Nonvolatile DACPOT™ Electronic Potentiometer with Up/Down Counter Interface 256 Step	8-27
SMP9317 Nonvolatile DACPOT™ Electronic Potentiometer with Up/Down Counter Interface 128 Step	8-33
S9518 Nonvolatile DACPOT™ Electronic Potentiometer with Debounce Push Button Interface 256 Step	8-39



SECTION 1	
The Convention Center	
1-1	General Description of the Project
1-2	Location and Surroundings
1-3	Site Plan
1-4	Site Map
1-5	Site Photographs
1-6	Site Description
1-7	Site History
1-8	Site Access
1-9	Site Easements
1-10	Site Zoning
1-11	Site Utilities
1-12	Site Environmental
1-13	Site Security
1-14	Site Safety
1-15	Site Maintenance
1-16	Site Management
1-17	Site Construction
1-18	Site Operation
1-19	Site Closure
1-20	Site Restoration

FEATURES

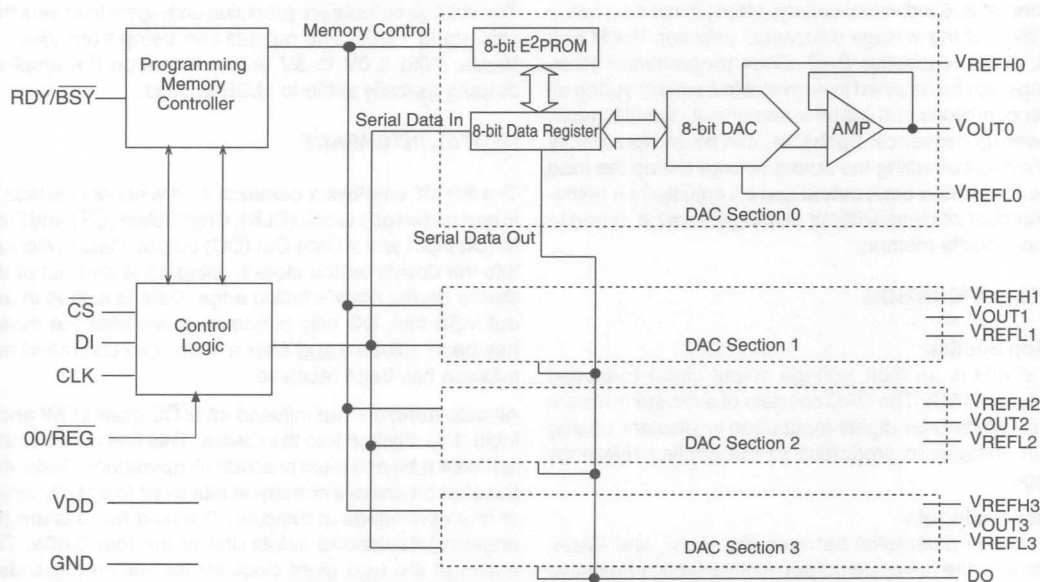
- Four 8-Bit DACs
 - Differential Non-linearity - $\pm 0.5\text{LSB}$
 - Integral Non-Linearity - $\pm 1\text{LSB}$
- Each DAC has Independent Reference Inputs
 - Output Buffer Amplifiers Swing Rail-to-Rail
 - Ground to V_{DD} Reference Input Range
- Each DAC's Digital Input Data Maintained in Nonvolatile EEPROM
- Power-On Reset Reloads Registers with Nonvolatile Data
- Simple Serial Interface for Reading and Writing DAC values, SPI™ and QSPI™ compatible.
- Fully operational from 2.7V to 5.5V

OVERVIEW

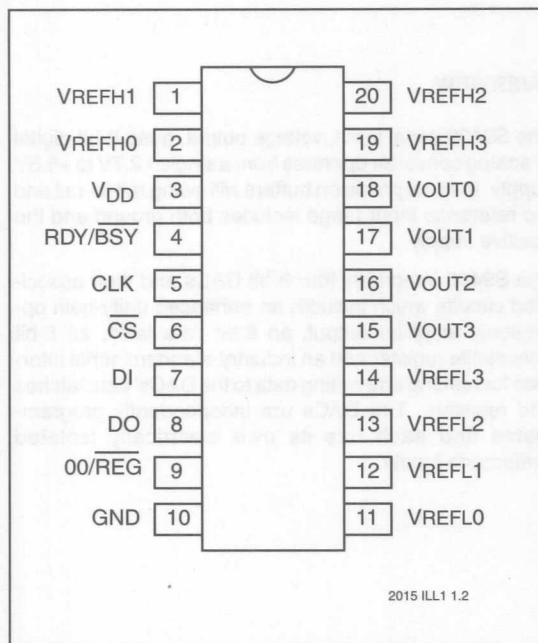
The S9408 serial input, voltage output, quad 8-bit digital to analog converter operates from a single +2.7V to +5.5V supply. Internal precision buffers will swing rail-to-rail and the reference input range includes both ground and the positive supply.

The S9408 integrates four 8-bit DACs and their associated circuits which include; an enhanced unity-gain operational amplifier output, an 8-bit data latch, an 8-bit nonvolatile register and an industry-standard serial interface for reading and writing data to the DACs' data latches and registers. The DACs are independently programmable and each has its own electrically isolated Vreference inputs.

FUNCTIONAL BLOCK DIAGRAM



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**PINOUT and SIGNAL DEFINITION**

Pin	Name	Function
1, 2 20, 19	VREFH	Vreference High: $V_{REFH} \leq V_{DD} > V_{REFL}$
3	VDD	Power Supply Voltage
4	RDY/BSY	Ready/Busy: open drain output indicating status of nonvolatile write operations
5	CLK	Clock Input Pin: used for serial data communication
6	\overline{CS}	Chip Select: When high deselects the device and places it in a low power mode
7	DI	Data Input: serial data input pin
8	DO	Data Output: serial data output pin
9	00/REG	Power On Recall Option Input
10	GND	Power Supply Ground
11, 12 13, 14	VREFL	Vreference Low: $V_{REFL} \geq GND < V_{REFH}$
15, 16 17, 18	VOUT	DAC Output: buffered D to A converter output

The analog outputs of the S9408 can be programmed to any one of 256 individual voltage steps. Each step value is $1/256^{\text{th}}$ of the voltage differential between V_{REFH} and V_{REFL} of the respective DAC. Once programmed these settings can be retained in nonvolatile memory during all power conditions and will be automatically recalled upon a power-up sequence. Each DAC can be independently read without affecting the output voltage during the read cycle. In addition each output can be adjusted an unlimited number of times without altering the value stored in the nonvolatile memory.

DEVICE OPERATION**Analog Section**

The S9804 is an 8-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage.

Reference inputs

The voltage differential between the V_{REFL} and V_{REFH} inputs sets the full-scale output voltage for its respective DAC. V_{REFL} must be equal to or greater than ground (positive voltage). V_{REFH} must be greater (more positive) than V_{REFL} and less than V_{DD} .

Output Buffer Amplifiers

The voltage outputs are precision unity-gain followers that slew up to $1V/\mu s$. The outputs can swing from V_{REFL} to V_{REFH} . With a 0V to 5V output transition the amplifier outputs typically settle to 1LSB in 50 μs .

DIGITAL INTERFACE

The S9408 employs a common 4-wire serial interface. It is comprised of a Clock (CLK), Chip Select (\overline{CS}) and Data In (DI) input and a Data Out (DO) output. Data is clocked into the device on the clock's rising edge and out of the device on the clock's falling edge. Data is shifted in and out MSB first. DO only becomes active after the device has been selected and after a valid read command and address has been received.

All data transfers are initiated after \overline{CS} goes LOW and a logic '1' is clocked into the device. This first data transfer is the start bit and must precede all operations. Following the start bit are two command bits used to specify which of four commands to execute. The next two bits are the address bits used to select one of the four DACs. The action of the next eight clock cycles will be dependent upon the command issued.



S	C _H	C _L	A _H	A _L	
1	0	0	A	A	NV Enable - Data Don't Care
1	0	1	A	A	Write Command - Data In
1	1	0	A	A	Read - Data Out
1	1	1	A	A	Recall -Data Don't Care

2015 PGM T1 1.0

TABLE 1. COMMAND FORMAT

Internally there are four DACs and associated with each are two registers. There is one data register that is used by the DAC to hold the digital value it converts. There is also one nonvolatile register that holds the default value that can be recalled into the data register during power-up or by executing the Recall command.

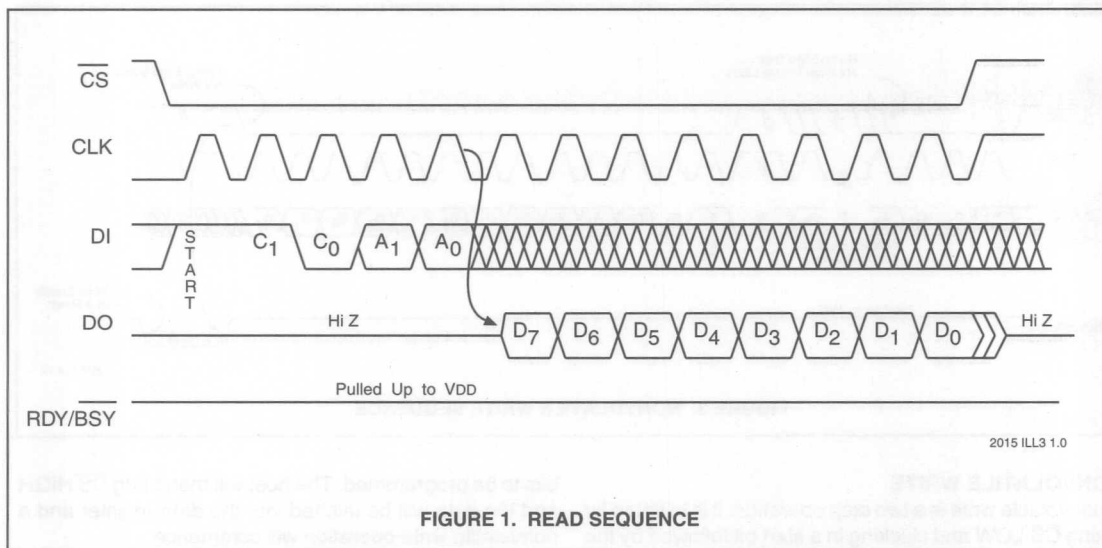
READ

Read operations are initiated by taking \overline{CS} LOW and clocking in a start bit followed by the read command and the address of the data register to be read. The next eight

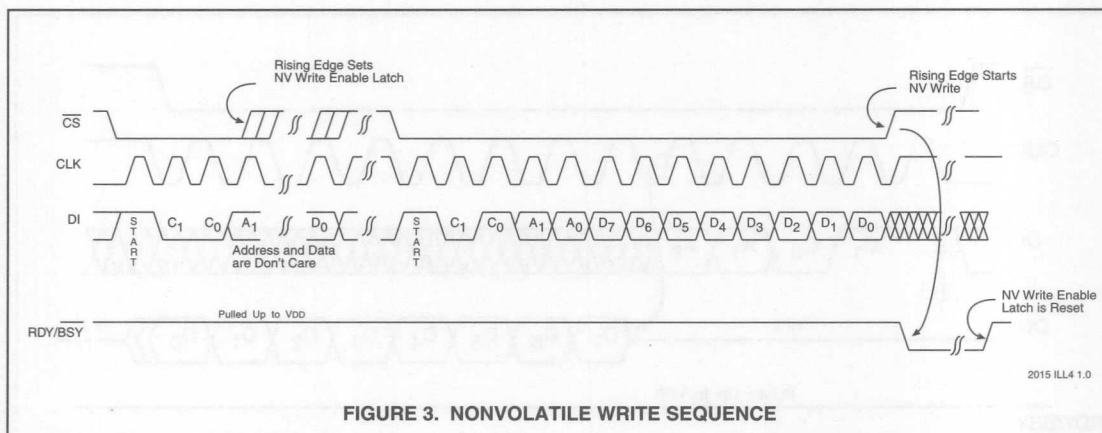
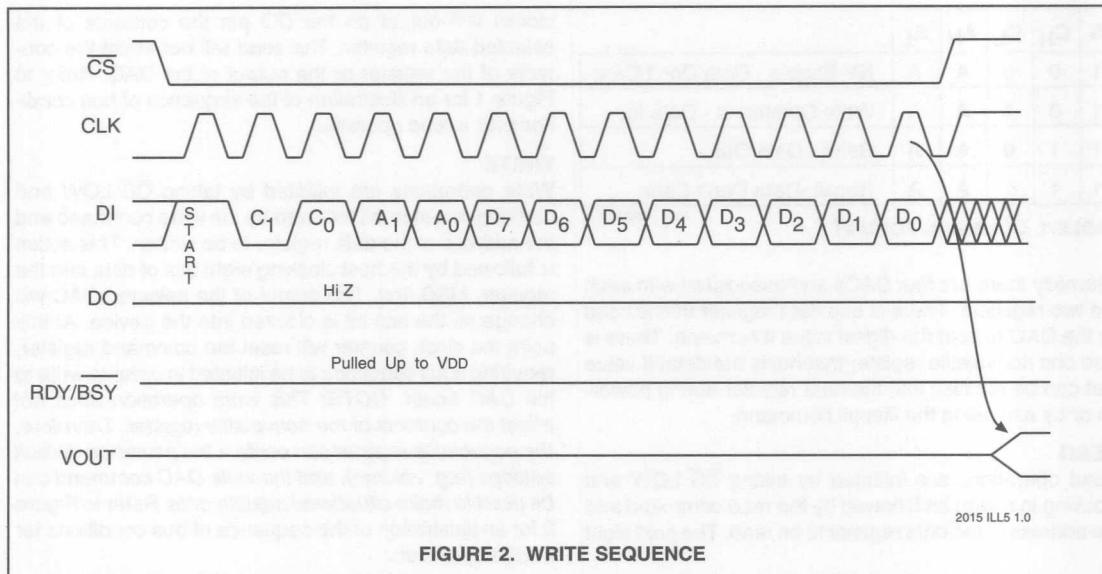
clocks will output on the DO pin the contents of the selected data register. This read will not affect the contents of the register or the output of the DAC. Refer to Figure 1 for an illustration of the sequence of bus conditions for a read operation.

WRITE

Write operations are initiated by taking \overline{CS} LOW and clocking in a start bit followed by the write command and the address of the data register to be written. This action is followed by the host clocking eight bits of data into the register, MSB first. The output of the selected DAC will change as the last bit is clocked into the device. At this point the clock counter will reset the command register, requiring a full sequence to be initiated in order to write to the DAC again. **NOTE:** This write operation does not affect the contents of the nonvolatile register. Therefore, the nonvolatile register can contain the power-on default settings (e.g. volume), and the write DAC command can be used to make situational adjustments. Refer to Figure 2 for an illustration of the sequence of bus conditions for a write operation.



2015 ILL3 1.0



NONVOLATILE WRITE

A nonvolatile write is a two step operation: it is initiated by taking $\overline{\text{CS}}$ LOW and clocking in a start bit followed by the NV Enable command. At this point the host can take $\overline{\text{CS}}$ back high or continue clocking in data. This data is don't care and will be ignored by the S9408. If any command other than write follows NV enable the NV latch will be cleared.

Next, the host takes $\overline{\text{CS}}$ LOW again and issues a write command and address and then clocks in the eight data

bits to be programmed. The host will then bring $\overline{\text{CS}}$ HIGH and the data will be latched into the data register and a nonvolatile write operation will commence.

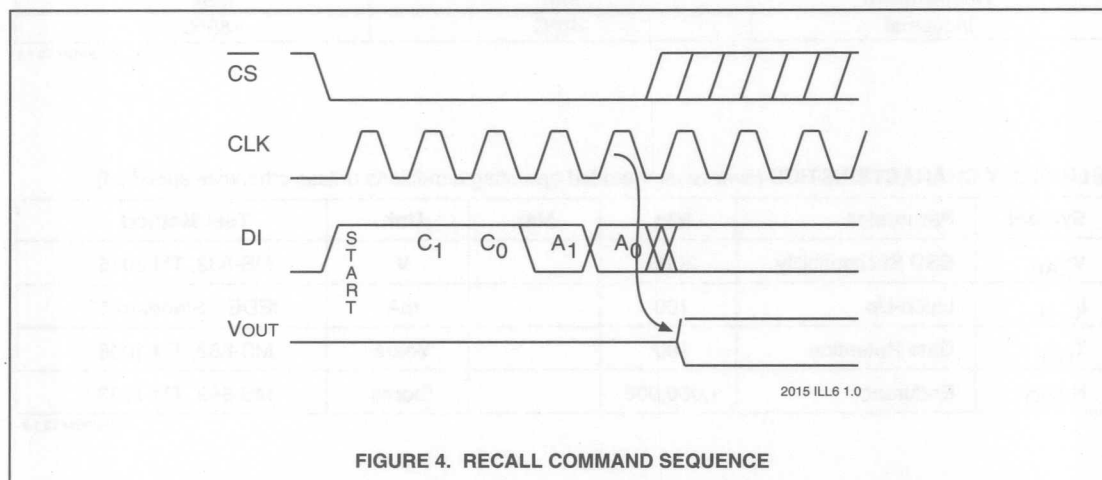
The status of the nonvolatile write can be monitored on the RDY/BSY pin. A logic low indicates the write is still in progress and the S9408 will not be accessible to the host; a logic high indicates the write has completed and the S9408 is ready for the next command. Refer to Figure 3 for an illustration of the sequence of bus conditions for a nonvolatile write operation.

**RECALL COMMAND**

The recall command will retrieve data from the selected nonvolatile register and write it into the data register of the associated DAC. This operation is initiated by taking \overline{CS} LOW and clocking in a start bit followed by the recall command and the address of the nonvolatile register to be recalled. The eight bits of data are don't care, so \overline{CS} can be taken high any time after the address bits are clocked in. Refer to Figure 4 for an illustration of the sequence of bus conditions for a Recall operation.

Power-on recall

Whenever the S9408 is powered on the DAC output values will be returned to the selected default setting. The default setting can be the nonvolatile register contents or all zeroes. The state of the 00/REG pin will determine which operation will be performed. If it is tied to ground (or left floating) the nonvolatile register contents will be recalled. Conversely, if it is tied to V_{DD} the S9408 will recall zeroes.



**ABSOLUTE MAXIMUM RATINGS**

V_{DD} to GND	-0.5V to +7V
Digital Inputs to GND	-0.5V to $V_{DD}+0.5V$
Analog Inputs to GND	-0.5V to $V_{DD}+0.5V$
Digital Outputs to GND	-0.5V to $V_{DD}+0.5V$
Analog Outputs to GND	-0.5V to $V_{DD}+0.5V$
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Soldering (10 Sec Max)	300°C

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Industrial	-40°C	+85°C

2015 PGM T2 1.1

RELIABILITY CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Min	Max	Unit	Test Method
V_{ZAP}	ESD Susceptibility	2000		V	MS-883, TM 3015
I_{LTH}	Latch-Up	100		mA	JEDEC Standard 17
T_{DR}	Data Retention	100		Years	MS-883, TM 1008
N_{END}	Endurance	1,000,000		Stores	MS-883, TM 1033

2015 PGM T3 1.2

DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{DD}	Supply Current (Excludes V_{REF})	Normal Operating		1	mA
I_{IH}	Input Leakage Current	$V_{IN} = V_{DD}$		10	μA
I_{IL}	Input Leakage Current	$V_{IN} = 0V$		-10	μA
V_{IH}	High Level Input Voltage		2	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400\mu A$	$V_{DD}-0.3$		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 1mA, V_{DD} = +5V$ $I_{OL} = 0.4mA, V_{DD} = +2.7V$		0.4 0.4	V V

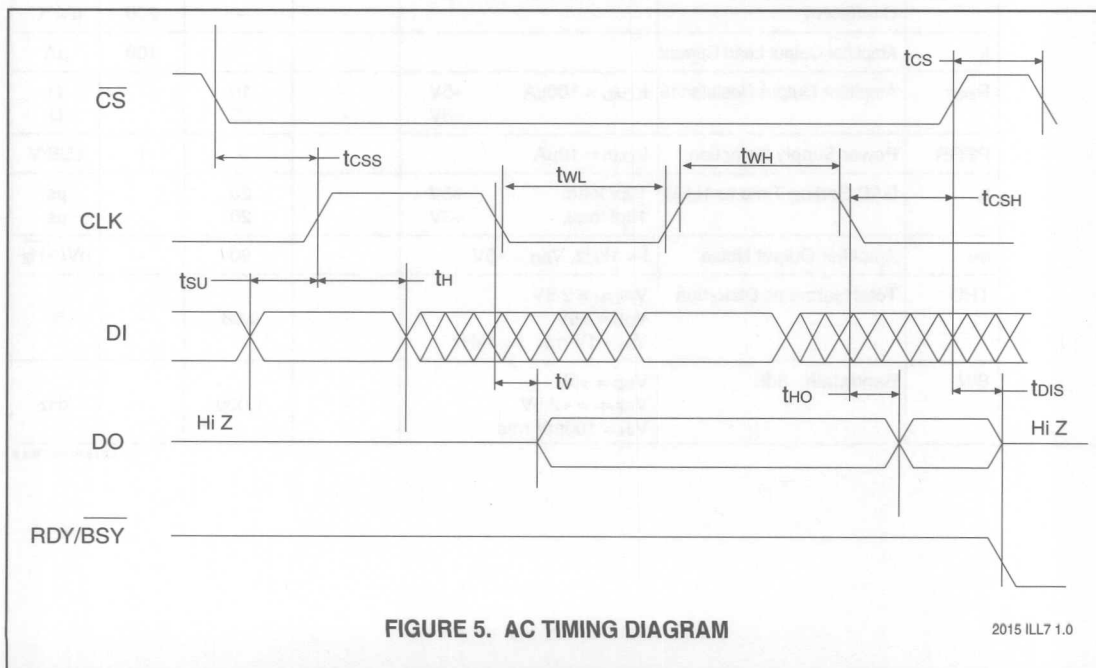
2015 PGM T4 1.3

**AC ELECTRICAL CHARACTERISTICS** $V_{DD} = +2.7V$ to $+5.5V$, $V_{REFH} = V_{DD}$, $V_{REFL} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_C	Clock Frequency		DC		1	MHz
t_{WH}	Minimum CLK High Time		500			ns
t_{WL}	Minimum CLK Low Time		300			ns
t_{CS}	Minimum CS High Time		150			ns
t_{CSS}	CS Setup Time		100			ns
t_{CSH}	CS Hold Time		0			ns
t_{SU}	Data In Setup Time	$C_L = 100pF$ See Note 1	50			ns
t_H	Data In Hold Time		50			ns
t_V	Output Valid Time				150	ns
t_{HO}	Data Out Hold Time		0			ns
t_{DIS}	Output Disable Time			400		ns
t_{BUSY}	Write Cycle Time			3.3	5	ms

Notes: 1. All timing measurements are defined at the point of signal crossing $V_{DD}/2$.

2015 PGM T5 1.1



2015 ILL7 1.0

**DAC DC ELECTRICAL CHARACTERISTICS**

$V_{DD} = +2.7V$ to $+5.5V$, $V_{refH} = V_{DD}$, $V_{refL} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless specified otherwise

	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Accuracy	INL	Integral Non-Linearity	$I_{LOAD} = 50\mu A$, $T_R = C$	-	0.6	± 1	LSB
			$T_R = I$	-	0.6	± 1	LSB
	DNL	Differential Non-Linearity	$I_{LOAD} = 100\mu A$, $T_R = C$	-	1.2	-	LSB
			$T_R = I$	-	1.2	-	LSB
References	V_{RH}	V_{refH} Input Voltage	$I_{LOAD} = 50\mu A$, $T_R = C$	-	0.25	± 0.5	LSB
			$T_R = I$	-	0.25	± 0.5	LSB
	V_{RL}	V_{refL} Input Voltage	$I_{LOAD} = 100\mu A$, $T_R = C$	-	0.5	-	LSB
			$T_R = I$	-	0.5	-	LSB
References	R_{IN}	V_{refH} to V_{refL} Resistance		-	38K	-	Ω
	TCR_{IN}	Temperature Coefficient of R_{IN}		-	700	-	ppm/ $^{\circ}C$
	ΔR_{IN}	Input Resistance Match		-	± 0.5	± 1	%
Analog Output	GE_{FS}	Full-Scale Gain Error	$D = FF$			± 1	LSB
	V_{OUTZS}	Output Offset Voltage	$D = 00$	0		20	mV
	TCV_{OUT}	V_{OUT} Temperature Coefficient	$V_{DD} = +5V$, $I_{LOAD} = 50\mu A$	-	-	200	$\mu V/^{\circ}C$
	I_L	Amplifier Output Load Current				100	μA
	R_{OUT}	Amplifier Output Resistance	$I_{LOAD} = 100\mu A$, $+5V$	-	10		Ω
			$+3V$	-	20		Ω
	PSRR	Power Supply Rejection	$I_{LOAD} = 10\mu A$	-	-	1	LSB/V
	t_s	DAC Setting Time to 1LSB	10pf load, $+5V$ 10pf load, $+3V$		20 20		μs μs
	e_N	Amplifier Output Noise	$f = 1kHz$, $V_{DD} = +5V$	-	90	-	nV/\sqrt{Hz}
	THD	Total Harmonic Distortion	$V_{REFH} = 2.5V$ $V_{DD} = +5V$ $V_{IN} = 1V$ rms, $f = 1kHz$	-	0.08	-	%
	BW	Bandwidth - 3dB	$V_{DD} = +5V$ $V_{REFH} = +2.5V$ $V_{IN} = 100mV$ rms	-	1,000	-	kHz

2015 PGM T6 1.6

**Quad 8-Bit Nonvolatile DACPOT™
With a Mute Control Input**

FEATURES

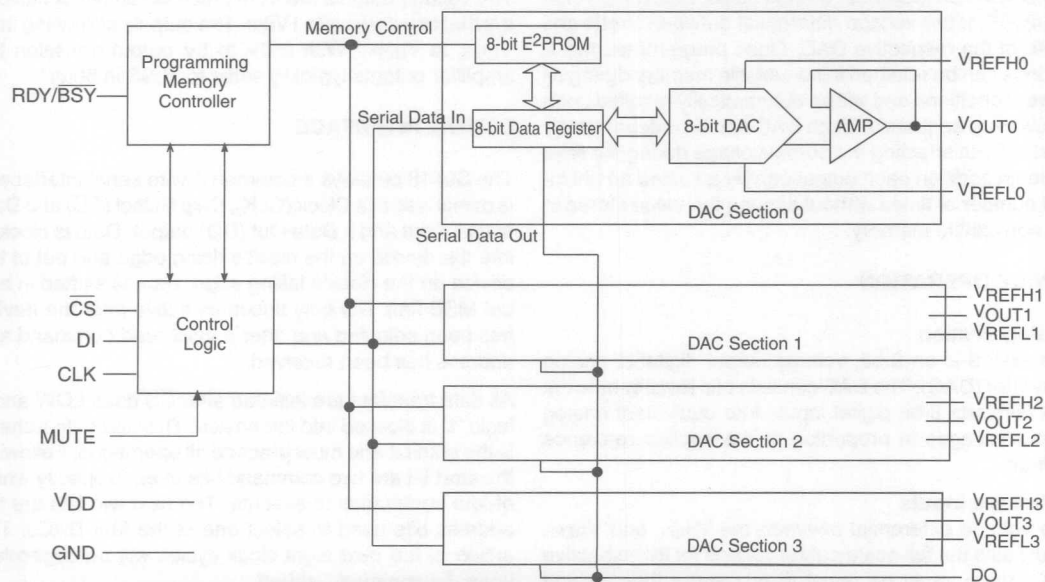
- **Four 8-Bit DACS**
 - Differential Non-linearity - $\pm 0.5\text{LSB}$
 - Integral Non-Linearity Error - $\pm 1\text{LSB}$
- **Each DAC has Independent Reference Inputs**
 - Output Buffer Amplifiers Swing Rail-to-Rail
 - Ground to V_{DD} Reference Input Range
- **Each DAC's Digital Inputs Maintained in EEPROM**
- **Power-On Reset Reloads Registers with Nonvolatile Data**
- **Simple Serial Interface for Reading and Writing DAC values, SPI™ and QSPI™ compatible.**
- **Fully operational from 2.7V to 5.5V**
- **Available in both Commercial and Industrial Temperature Ranges**

OVERVIEW

The S9418 serial input, voltage output, quad 8-bit digital to analog converter operates from a single +2.7V to +5.5V supply. Internal precision buffers will swing rail-to-rail and the reference input range includes both ground and the positive supply.

The S9418 integrates four 8-bit DACs and their associated circuits which include; an enhanced unity gain operational amplifier output, an 8-bit data latch, an 8-bit non-volatile register and an industry standard serial interface for reading and writing data to the DACs' data latches and registers. The DACs are independently programmable and each has its own electrically isolated Vreference inputs.

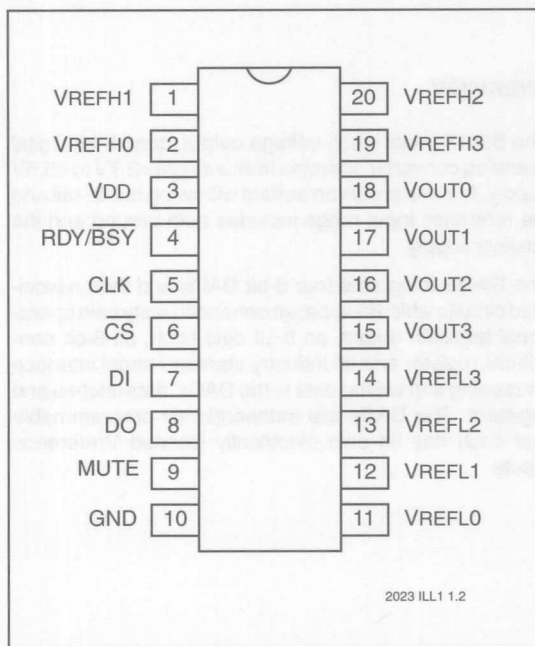
FUNCTIONAL BLOCK DIAGRAM



2023 ILL2 1.2



PINOUT and SIGNAL DEFINITION



Pin	Name	Function
1, 2 20, 19	VREFH	Vreference High: $V_{REFH} \leq V_{DD} > V_{REFL}$
3	VDD	Power Supply Voltage
4	RDY/BSY	Ready/Busy: open drain output indicating status of nonvolatile write operations
5	CLK	Clock Input Pin: used for serial data communication
6	\overline{CS}	Chip Select: When high deselects the device and places it in a low power mode
7	DI	Data Input: serial data input pin
8	DO	Data Output: serial data output pin
9	MUTE	When active forces V_{OUT} to V_{REFL}
10	GND	Power Supply Ground
11, 12 13, 14	VREFL	Vreference Low
15, 16 17, 18	VOUT	DAC Output: buffered D to A converter output

The analog outputs of the S9418 can be programmed to any one of 256 individual voltage steps. Each step value is $1/256^{th}$ of the voltage differential between V_{refH} and V_{refL} of the respective DAC. Once programmed these settings can be retained in nonvolatile memory during all power conditions and will be automatically recalled upon a power-up sequence. Each DAC can be independently read without affecting the output voltage during the read cycle. In addition each output can be adjusted an unlimited number of times without altering the value stored in the nonvolatile memory.

DEVICE OPERATION

Analog Section

The S9418 is an 8-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage.

Reference inputs

The voltage differential between the V_{REFL} and V_{REFH} inputs sets the full-scale output voltage for its respective DAC. V_{REFL} must be equal to or greater than ground (positive voltage). V_{REFH} must be greater (more positive) than V_{REFL} and less than V_{DD} .

Output Buffer Amplifiers

The voltage outputs are from precision unity-gain followers that can slew up to $1V/\mu s$. The outputs can swing from V_{REFL} to V_{REFH} . With a 0V to 5V output transition the amplifier outputs typically settle to 1LSB in $50\mu s$.

DIGITAL INTERFACE

The S9418 employs a common 4-wire serial interface. It is comprised of a Clock (CLK), Chip Select (\overline{CS}) and Data In (DI) input and a Data Out (DO) output. Data is clocked into the device on the clock's rising edge and out of the device on the clock's falling edge. Data is shifted in and out MSB first. DO only becomes active after the device has been selected and after a valid read command and address has been received.

All data transfers are initiated after \overline{CS} goes LOW and a logic '1' is clocked into the device. This first data transfer is the start bit and must precede all operations. Following the start bit are two command bits used to specify which of four commands to execute. The next two bits are the address bits used to select one of the four DACs. The action of the next eight clock cycles will be dependent upon the command issued.



S	CH	CL	AH	AL	
1	0	0	A	A	NV Enable - Data Don't Care
1	0	1	A	A	Write Command - Data In
1	1	0	A	A	Read - Data Out
1	1	1	A	A	Recall -Data Don't Care

2023 PGM T1 1.0

TABLE 1. COMMAND FORMAT

Internally there are four DACs and associated with each are two registers. There is one data register that is used by the DAC to hold the digital value it converts. There is also one nonvolatile register that holds the default value that can be recalled into the data register during power-up or by executing the Recall command.

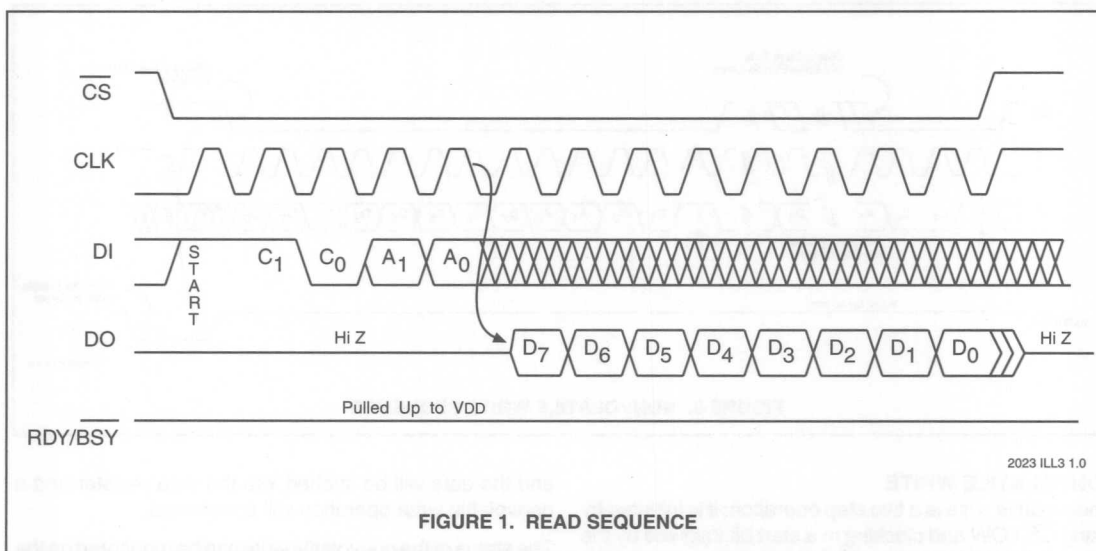
READ

Read operations are initiated by taking \overline{CS} LOW and clocking in a start bit followed by the read command and the address of the data register to be read. The next eight

clocks will output on the DO pin the contents of the selected data register. This read will not affect the contents of the register or the output of the DAC. Refer to Figure 1 for an illustration of the sequence of bus conditions for a read operation.

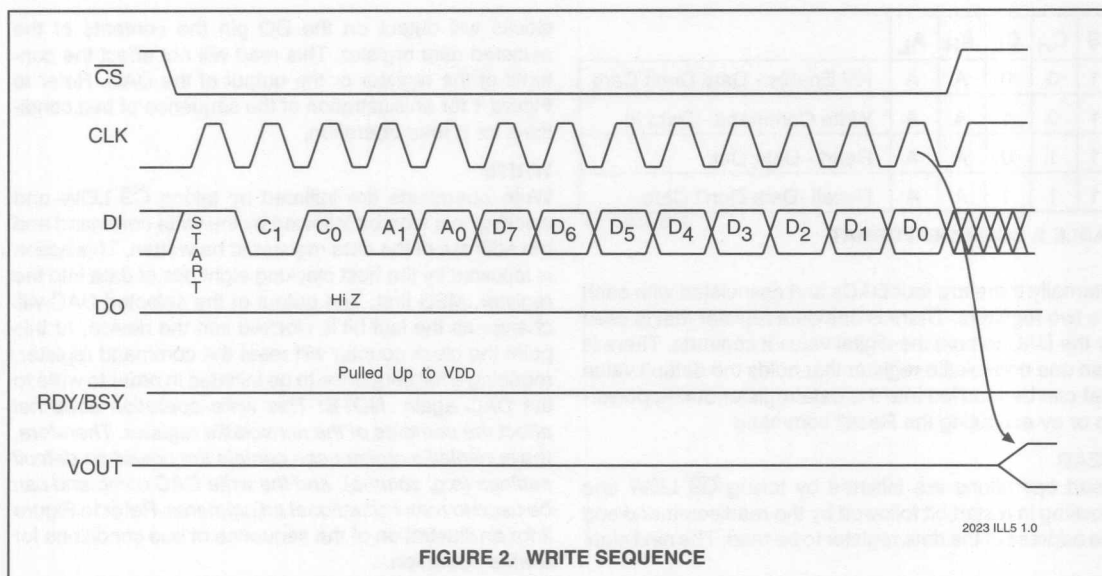
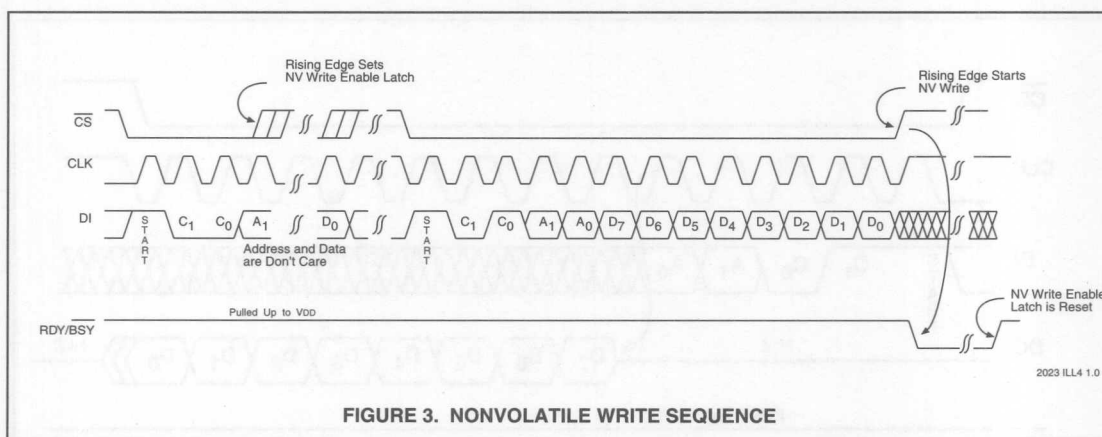
WRITE

Write operations are initiated by taking \overline{CS} LOW and clocking in a start bit followed by the write command and the address of the data register to be written. This action is followed by the host clocking eight bits of data into the register, MSB first. The output of the selected DAC will change as the last bit is clocked into the device. At this point the clock counter will reset the command register, requiring a full sequence to be initiated in order to write to the DAC again. **NOTE:** This write operation does not affect the contents of the nonvolatile register. Therefore, the nonvolatile register can contain the power-on default settings (e.g. volume), and the write DAC command can be used to make situational adjustments. Refer to Figure 2 for an illustration of the sequence of bus conditions for a write operation.



2023 ILL3 1.0

FIGURE 1. READ SEQUENCE

**FIGURE 2. WRITE SEQUENCE****FIGURE 3. NONVOLATILE WRITE SEQUENCE**

NONVOLATILE WRITE

A nonvolatile write is a two step operation: it is initiated by taking $\overline{\text{CS}}$ LOW and clocking in a start bit followed by the NV Write Enable command. At this point the host can take $\overline{\text{CS}}$ back high or continue clocking in data. This data is don't care and will be ignored by the S9418.

Next, the host takes $\overline{\text{CS}}$ LOW again and issues a write command and address and then clocks in the eight data bits to be programmed. The host will then bring $\overline{\text{CS}}$ HIGH

and the data will be latched into the data register and a nonvolatile write operation will commence.

The status of the nonvolatile write can be monitored on the RDY/BSY pin. A logic low indicates the write is still in progress and the S9418 will not be accessible to the host; a logic high indicates the write has completed and the S9418 is ready for the next command. Refer to Figure 3 for an illustration of the sequence of bus conditions for a nonvolatile write operation.

**RECALL COMMAND**

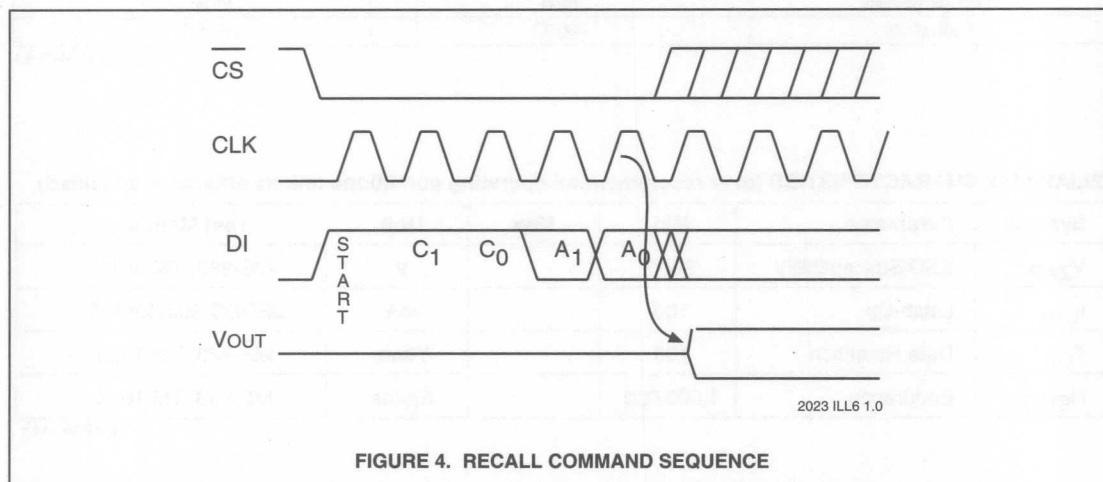
The recall command will retrieve data from the selected nonvolatile register and write it into the data register of the associated DAC. This operation is initiated by taking \overline{CS} LOW and clocking in a start bit followed by the recall command and the address of the nonvolatile register to be recalled. The eight bits of data are don't care, so \overline{CS} can be taken high any time after the address bits are clocked in. Refer to Figure 4 for an illustration of the sequence of bus conditions for a Recall operation.

Power-On Recall

Whenever the S9418 is powered on, the V_{OUT} values will be returned to the analog equivalent of the data byte stored in the nonvolatile register.

MUTE Operation

The MUTE input is active high. Whenever the input is low, the V_{OUT} will reflect the value in the data register. If MUTE is driven high the V_{OUT} outputs will be switched to V_{REFL} . Releasing the MUTE input returns the V_{OUT} outputs to the analog equivalent of the data register contents.



**ABSOLUTE MAXIMUM RATINGS**

V_{DD} to GND	-0.5V to +7V
Digital Inputs to Gnd	-0.5V to $V_{DD}+0.5V$
Analog Inputs to ground	-0.5V to $V_{DD}+0.5V$
Digital Outputs to Gnd	-0.5V to $V_{DD}+0.5V$
Analog Outputs to Gnd	-0.5V to $V_{DD}+0.5V$
Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Soldering (10 Sec Max)	300°C

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Industrial	-40°C	+85°C

2023 PGM T2 1.1

RELIABILITY CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Min	Max	Unit	Test Method
V_{ZAP}	ESD Susceptibility	2000		V	MS-883, TM 3015
I_{LTH}	Latch-Up	100		mA	JEDEC Standard 17
T_{DR}	Data Retention	100		Years	MS-883, TM 1008
N_{END}	Endurance	1,000,000		Stores	MS-883, TM 1033

2023 PGM T3 1.1

DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{DD}	Supply Current (Excludes V_{REF})	Normal Operating		1	mA
I_{IH}	Input Leakage Current	$V_{IN} = V_{DD}$		10	μA
I_{IL}	Input Leakage Current	$V_{IN} = 0V$		-10	μA
V_{IH}	High Level Input Voltage		2	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400\mu A$	$V_{DD}-0.3$		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 1mA, V_{DD} = +5V$ $I_{OL} = 0.4mA, V_{DD} = +2.7V$		0.4 0.4	V V

2023 PGM T4 1.1



$V_{DD} = +2.7V$ to $+5.5V$, $V_{REFH} = V_{DD}$, $V_{REFL} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise specified

Notes: 1. All timing measurements are defined at the point of signal crossing $V_{DD}/2$.

2023 PGM T5 1.1



**DAC ELECTRICAL CHARACTERISTICS** $V_{DD} = +2.7V$ to $+5.5V$, $V_{refH} = V_{DD}$, $V_{refL} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless specified otherwise

	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Accuracy	INL	Integral Non-Linearity	$I_{LOAD} = 50\mu A$, $T_R = C$	-	0.6	± 1	LSB
			$T_R = I$	-	0.6	± 1	LSB
	DNL	Differential Non-Linearity	$I_{LOAD} = 100\mu A$, $T_R = C$	-	1.2	-	LSB
			$T_R = I$	-	1.2	-	LSB
References	V _{refH}	V _{refH} Input Voltage	$I_{LOAD} = 50\mu A$, $T_R = C$	-	0.25	± 0.5	LSB
			$T_R = I$	-	0.25	± 0.5	LSB
	V _{refL}	V _{refL} Input Voltage	$I_{LOAD} = 100\mu A$, $T_R = C$	-	0.5	-	LSB
			$T_R = I$	-	0.5	-	LSB
	ΔR_{IN}	Input Resistance Match		-	± 0.5	± 1	%
Analog Output	GEFS	Full-Scale Gain Error	D = FF			1	LSB
	V _{OUTZS}	Output Offset Voltage	D = 00	0		20	mV
	TCV _{OUT}	V _{OUT} Temperature Coefficient	$V_{DD} = +5V$, $I_{LOAD} = 50\mu A$	-	-	200	$\mu V/^{\circ}C$
	I _L	Amplifier Output Load Current				100	μA
	R _{OUT}	Amplifier Output Resistance	$V_{DD} = V_{refH}$ +5V +3V	- -	10 20		Ω Ω
	PSRR	Power Supply Rejection	$I_{LOAD} = 10\mu A$	-	-	1	LSB/V
	t _s	DAC Setting Time to 1LSB	10pf 10pf +5V +3V		20 20		μs μs
	e _N	Amplifier Output Noise	f = 1kHz, $V_{DD} = +5V$	-	90	-	nV/ \sqrt{Hz}
	THD	Total Harmonic Distortion	V _{REFH} = 2.5V V _{DD} = +5V V _{IN} = 1V rms, f = 1kHz	-	0.08	-	%
	BW	Bandwidth - 3dB	V _{DD} = +5V V _{REFH} = +2.5V V _{IN} = 100mV rms	-	1,000	-	kHz

2023 PGM T6 1.4

**2-Channel and 3-Channel, 10-Bit
Auto-Monitor Data Acquisition Systems**

Preliminary

FEATURES

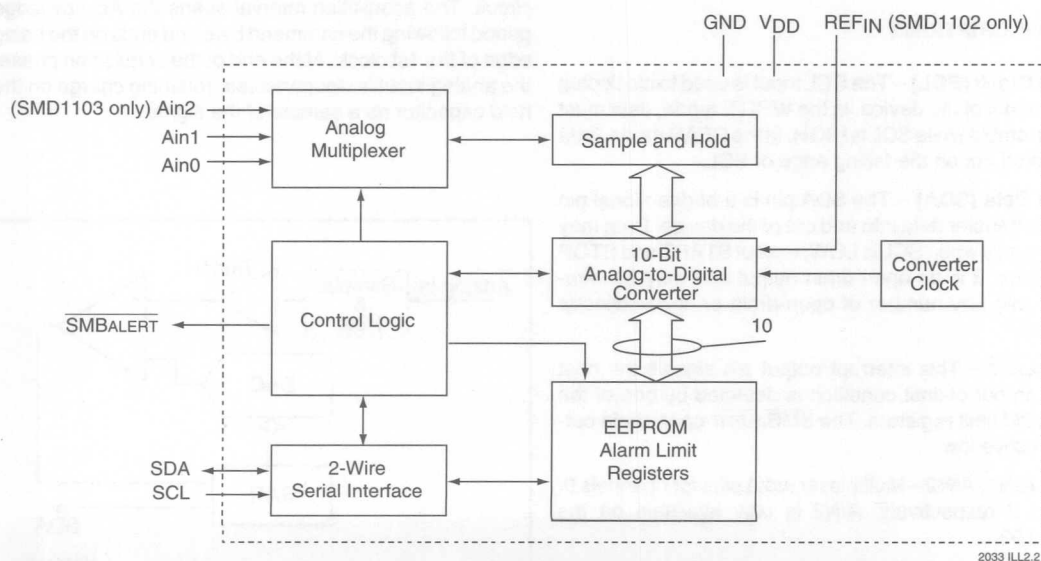
- Complete Data Acquisition System
 - 10-Bit A/D Converter Resolution
 - 26 μ s Acquisition plus Conversion Time
 - Input Voltage Range, GND to V_{DD}
 - User-Programmable, Nonvolatile EEPROM Alarm Limits for Each Input Channel
 - Auto-Increment of Input Channels
 - Two Wire I²C Serial Data Interface
 - System Management Bus (SMBus) Compatible
 - Auto-Monitor with SMBALERT Output
 - Low Quiescent Current, 25 μ A
 - Wide Supply Voltage Range, 2.7V to 5.5V
- SMD1102
 - 2-Channel Analog Input
 - External Voltage Reference Input Provided for Absolute Measurements
- SMD1103
 - 3-Channel Analog Input
 - Reference Voltage Input for the A/D Converter is Connected to V_{DD} for Ratiometric Measurements

OVERVIEW

The SMD1102 and SMD1103 each contain a 10-bit data acquisition system (DAS) with dedicated EEPROM alarm limit storage. Both devices communicate with the host μ P via a standard two-wire I²C serial interface. After programming at startup, the SMD1102/03 can automatically monitor one or more analog input channels, the SMD1102 and SMD1103 provide 2-channels and 3-channels respectively. If any input signal moves beyond its user-programmed limits, the host is notified by the SMBALERT output. Between A/D conversions the quiescent current falls to around 25 μ A making the SMD1102/03 ideal for battery-powered equipment, see table below. The SMD1102/03 are fabricated using Summit's advanced CMOS EEPROM technology and are suitable for 3V or 5V systems.

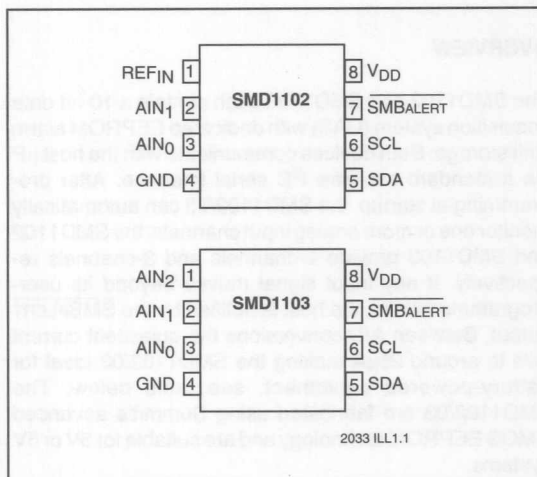
V_{DD}	Active @ 40ksps	Quiescent
5.25	2.5mA	25 μ A
3.6	1.5mA	25 μ A
2.7	1.2mA	25 μ A

2033 PGM T1.1

BLOCK DIAGRAM




PIN CONFIGURATIONS



PIN NAMES

SDA	Serial Data I/O
SCL	Serial Clock Input
AIN ₀ , AIN ₁ , AIN ₂	Analog Channel Inputs
GND	Analog and Digital Ground
SMBALERT	Interrupt Output
VDD	Supply Voltage
REFIN	Reference Input

PIN DESCRIPTIONS

Serial Clock (SCL) – The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) – The SDA pin is a bi-directional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

SMBALERT – This interrupt output pin signals the host when an out-of-limit condition is detected by one of the EEPROM limit registers. The SMBALERT open-drain output is active low.

AIN₀, AIN₁, AIN₂ – Multiplexer input pins for channels 0, 1, and 2 respectively. AIN₂ is only available on the SMD1103.

REFIN – Voltage reference input for 10-bit A/D converter, on SMD1102 only.

Endurance and Data Retention

The EEPROM memory array and registers are designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

DEVICE OPERATION

The SMD1102 and SMD1103 Data Acquisition Systems (DAS) are each comprised of: an analog input multiplexer, sample-and-hold circuit, 10-bit successive approximation Analog-to-Digital (A/D) Converter, and nonvolatile EEPROM memory to store upper and lower alarm-limits for each input channel. The user programs the alarm limits via the industry-standard I²C interface. An SMBALERT interrupt output signals if any of the analog inputs move outside these limits.

DAS Modes of Operation

The SMD1102/03 have four user-selectable modes of operation. These modes are: a single conversion of one channel, successive conversions on the same channel, sequential conversions on all three channels, or autonomous conversions of the same or all channels.

Sample-and-Hold Operation

The channel switching and sampling architecture of the A/D's comparator is illustrated in the equivalent input circuit diagram in Figure 1. During acquisition the selected channel charges a capacitor in the sample-and-hold circuit. The acquisition interval spans the Acknowledge period following the command byte and ends on the rising edge of the 1st clock. At the end of the acquisition phase, the analog input is disconnected, retaining charge on the hold capacitor as a sample of the signal.

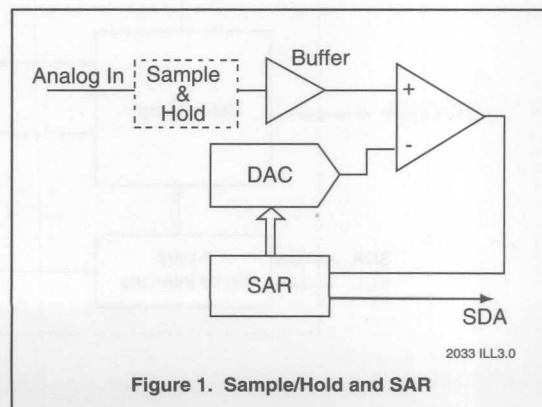
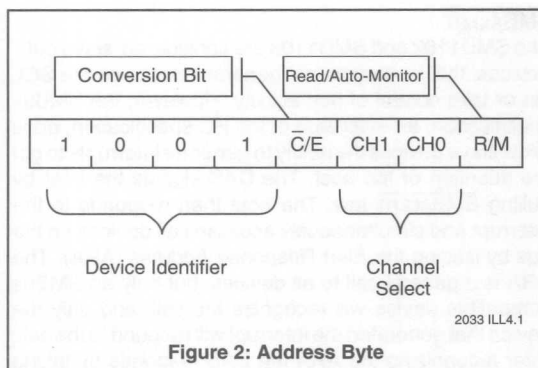


Figure 1. Sample/Hold and SAR



Addressing and Command Sequence

All operations of the DAS are preceded first by the start condition and then by the addressing command sequence, 1001. The next bit in the addressing sequence is the conversion bit; when set to zero the device is instructed to perform an A/D conversion, and when set to logic one the EEPROM limit register will be addressed. The next two bits are the channel select bits. If the channel select bits are set to 11, and the conversion bit is set to 0, then auto-increment is enabled. In the auto-increment mode, conversions are performed on successive channels, starting with channel 0. After channel 2 is converted (channel 1 on the SMD1102) the address will wrap around to channel 0. The last bit is for mode selection. When mode select is set to logic one, data can be read from a

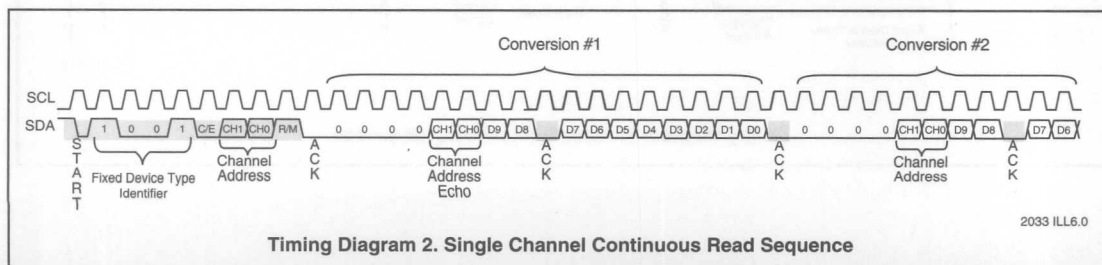
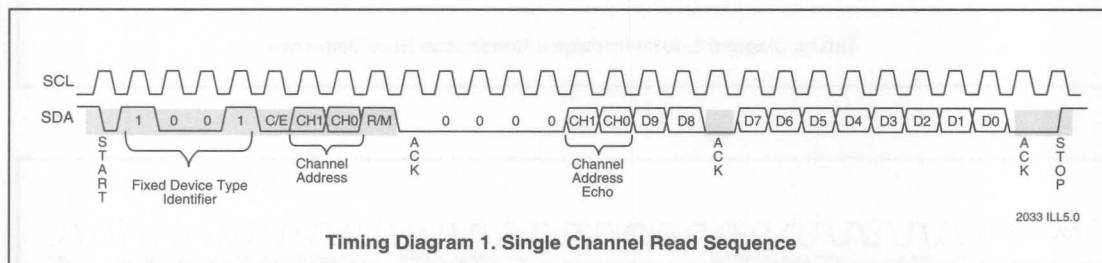
conversion or from one of the EEPROM limit registers, depending on the state of the conversion bit. When the mode select bit is logic zero, either the auto-monitor mode is entered or the EEPROM limit register is programmed, again depending on the state of the conversion bit.

Single Channel Conversions

The command sequence is the device identifier followed by conversion bit set to zero and the channel select bits set to the desired value and R/M set to logic one. After the R/M bit is clocked in, the host releases the SDA line and monitors the SDA line for an acknowledge bit (ACK) from the SMD1102/03. The device will drive the SDA line low indicating it received the command and that it has initiated the acquisition and conversion on the selected channel. The clock source for the acquisition and conversion is an internal clock. After the ACK, the SMD1102/03 will output four dummy zeros on SDA followed by an echo of the channel's address, 2 bits. The remaining bits in this first byte are the two MSBs of the conversion. Refer to timing diagram 1 for a detailed illustration of this sequence, and that for retrieving the remaining conversion byte. The host can issue a stop condition after retrieving the conversion data and place the SMD1102/03 in a low power standby mode.

Successive Single Channel Conversions

If the host does not issue a stop command after receiving the last bit of the previous conversion, but instead issues an ACK and continues clocking, then the SMD1102/03 will begin another acquisition and conversion process on the same channel.





Auto-Increment

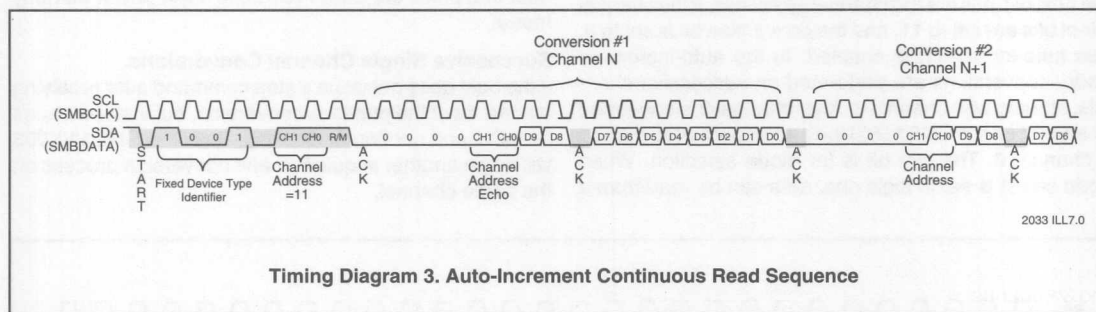
In the auto-increment mode, the DAS starts a conversion and then automatically advances to the next channel. The auto-increment mode always starts at channel 0 and switches the channel input in the sequence 0, 1, 2, 0, 1, 2, etc. (SMD1103) after each successive conversion. The SMD1102 and SMD1103 independently repeat this process so long as; the host continues clocking the device and supplies ACK bits at the appropriate clock interval, and issues no stop conditions. Refer to Timing Diagram 3 for a detailed illustration of the sequence.

Auto-Monitor

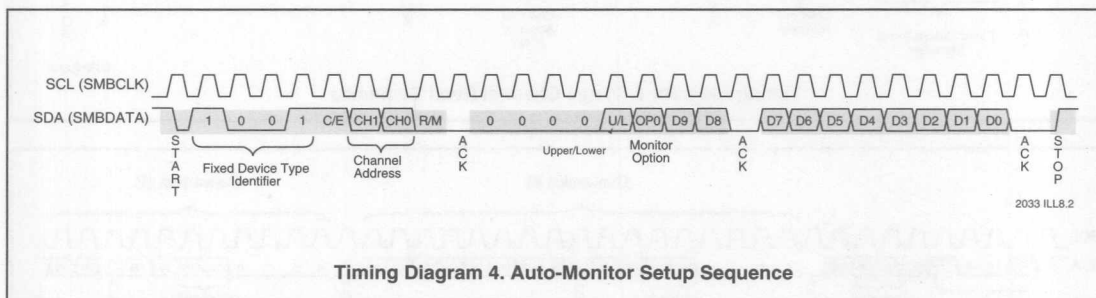
Auto-monitor operation takes full advantage of the unique capabilities of the SMD1102/03. Each device can autonomously monitor the analog channels, compare the conversion data to stored nonvolatile register data and if necessary alert the host to out-of-limit conditions.

SMBALERT

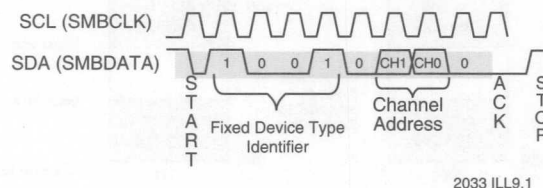
The SMD1102 and SMD1103 are considered 'slave only' devices; that is, they do not generate clocks on the SCL pin or take control of bus activity. However, the SMBus specification, an extension of the I²C specification, does allow slave devices the ability to generate interrupts to get the attention of the host. The DAS signals the host by pulling SMBALERT low. The host then responds to the interrupt and simultaneously accesses all devices on the bus by issuing the Alert Response Address (ARA). The ARA is a general call to all devices, but only an SMBus compatible device will recognize the call, and only the device that generated the interrupt will respond to the call. After recognizing the ARA the DAS responds by taking SDA low (generating an ACK back to the host). The host will now continue clocking SCL and the DAS will output its Device Address. If more than one SMBus compliant device is in an alert condition, standard I²C bus arbitration allows the device with the lowest address to be serviced first. The DAS will release the SMBALERT signal when it has been directly addressed.



Timing Diagram 3. Auto-Increment Continuous Read Sequence



Timing Diagram 4. Auto-Monitor Setup Sequence

**Timing Diagram 5. Auto-Monitor Start Sequence**

Programming For Auto-Monitor

Setting-up the SMD1102/03 for the auto-monitor function is straightforward. In the first byte to SDA, the host issues a start condition bit, followed by the device identifier, the conversion bit set to one, the channel select bits set to the desired state, and the R/M bit set to zero. The 1102/03 responds with an ACK, and the host sends the second byte. The first four bits must be zero, the fifth bit is limit select (0 = lower limit, 1 = upper limit), and this is followed by the monitor option bit, described below. The final two bits are the high-order comparison bits that will be stored in a nonvolatile register. The 1102/03 responds with another ACK and the host clocks in the final eight bits of the comparison data with the 1102/03 responding with a final ACK. Refer to Timing Diagrams 4 and 5 for detailed sequence information. The host will issue a stop condition and the SMD1102/03 will store the data in the nonvolatile registers (a 10ms maximum operation). After defining both limits the host can issue a start monitor command for that particular channel. Alternatively, to monitor all 3 channels in an auto-increment mode, the limits for the 2nd and 3rd channel must be programmed. Note that the host must program the upper and lower limits for each channel used. Therefore six operations are needed to set all channels on the SMD1103, and four operations on the SMD1102.

Alert Conditions

For each channel the host can select one of four conditions that will generate an alert. These conditions are determined by the option bits stored with the upper and lower limits in the NV registers. Chart 1 details these conditions. If an out-of-limit condition is detected, the SMD1102/03 will temporarily remove itself from the auto-increment mode, (if that was selected) and monitor the

channel that caused the alert. There must be five successive conversions resulting in an out-of-limit condition before the SMD1102/03 will pull SMBALERT low. If at any time during the verify routine, the out-of-limit condition is negated, the SMD1102/03 will re-enter its normal monitor routine and not assert SMBALERT. If the SMBALERT signal has been pulled low, the SMD1102/03 will halt its monitoring function and await instructions from the host.

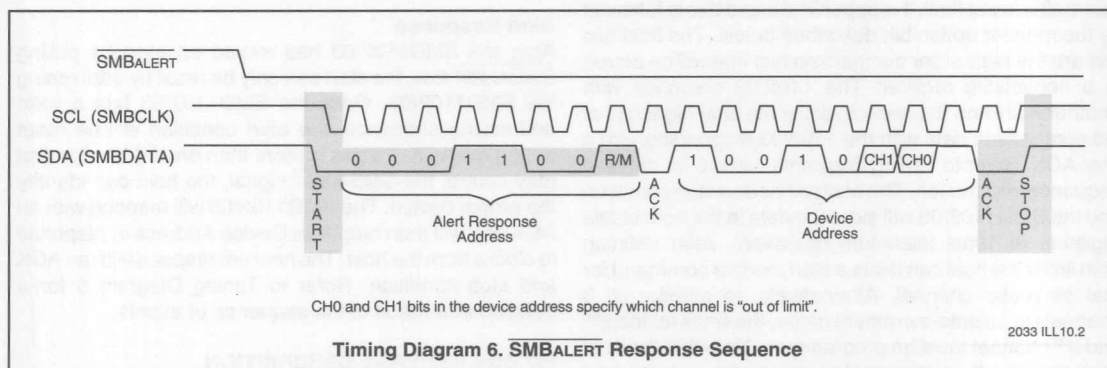
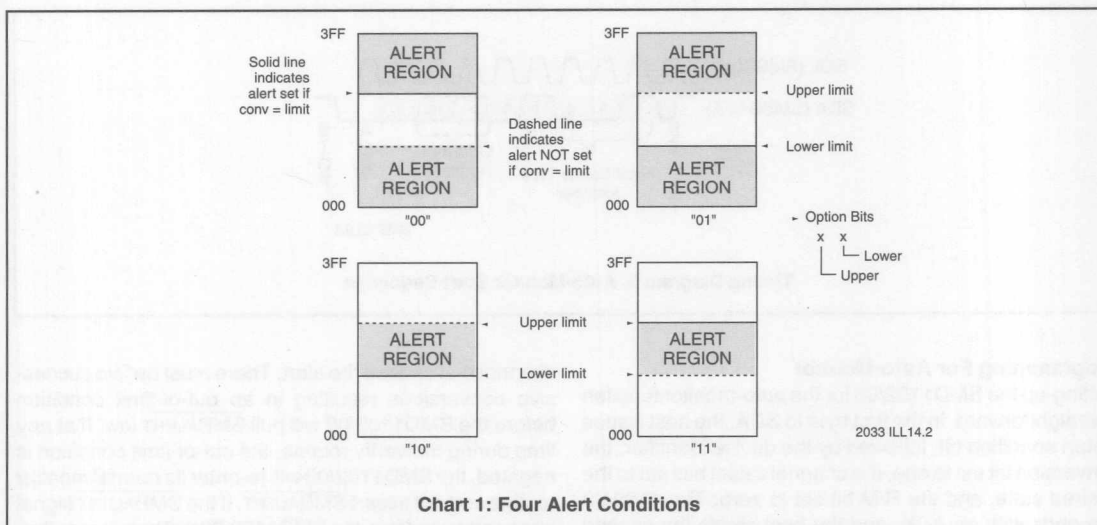
Alert Response

After the SMD1102/03 has issued an alert by pulling SMBALERT low, the alert can only be reset by addressing the SMD1102/03. Once the SMD1102/03 has a valid addressing sequence, the alert condition will be reset during the ACK. If there is more than one I²C device that may control the SMBALERT signal, the host can identify the proper device. The SMD1102/03 will respond with an ACK and will then output its Device Address in response to clocks from the host. The host will respond with an ACK and stop condition. Refer to Timing Diagram 6 for a detailed illustration of the sequence of events.

I²C BUS GENERAL DESCRIPTION

General Description

The I²C bus is a bi-directional, two-line, serial communications interface between integrated circuits. The two communication lines are the serial data line, SDA, and the serial clock line, SCL. The SDA line must be connected to a positive supply by a pull-up resistor located somewhere on the bus. Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy). The SMD1102/03 communicate with the host μ P using the I²C data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device that receives data as a "receiver". The device controlling data transmission is called the "master" and the controlled device is called the "slave".





Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition, refer to Figure 1.

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be "not busy". A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 3).

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it re-

ceived the eight bits of data (See Figure 4). The SMD1102/03 will respond with an ACK bit after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the SMD1102/03 will respond with an ACK after the receipt of each subsequent 8-bit word or byte. In the READ mode, the SMD1102/03 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACK signal. If an ACK is detected, and no STOP condition is generated by the master, the SMD1102/03 will continue to transmit data. If an ACK is not detected, the 1102/03 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 1). For the SMD1102 and SMD1103 this is fixed as 1001 (binary). The following bits provide conversion information, channel address and operating mode.

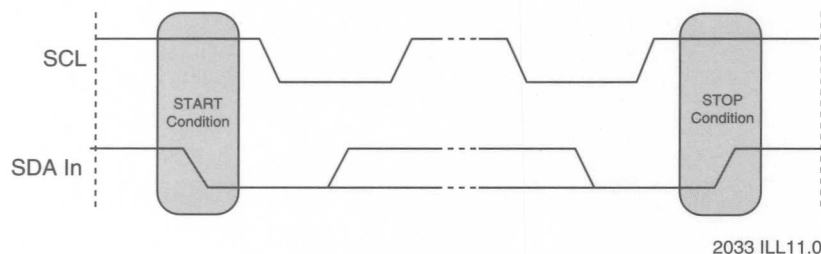


Figure 3: Start and Stop Conditions

2033 ILL11.0

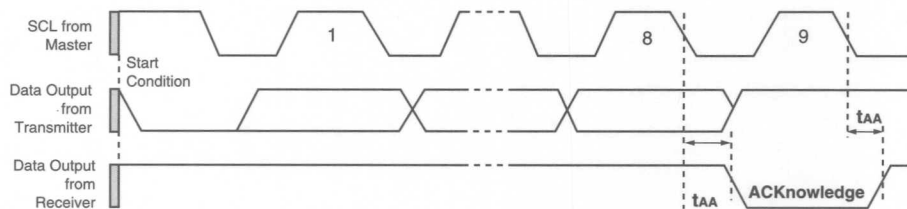


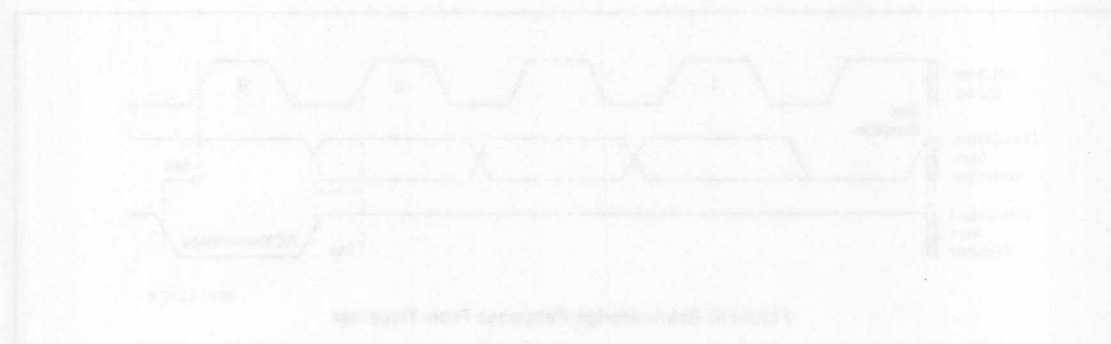
Figure 4: Acknowledge Response From Receiver

2033 ILL12.0



Figure 1 shows the timing diagram for the SMD1102/SMD1103. The diagram illustrates the relationship between the input signal (IN) and the output signal (OUT) during a typical operation. The input signal is a square wave, and the output signal is a square wave that follows the input signal with a delay. The delay is caused by the internal capacitance of the device. The diagram also shows the setup and hold times for the input signal. The setup time is the time interval between the last change of the input signal and the sampling clock edge. The hold time is the time interval between the sampling clock edge and the first change of the input signal. The diagram shows that the setup and hold times are both satisfied for the SMD1102/SMD1103.

Figure 2 shows the timing diagram for the SMD1102/SMD1103. The diagram illustrates the relationship between the input signal (IN) and the output signal (OUT) during a typical operation. The input signal is a square wave, and the output signal is a square wave that follows the input signal with a delay. The delay is caused by the internal capacitance of the device. The diagram also shows the setup and hold times for the input signal. The setup time is the time interval between the last change of the input signal and the sampling clock edge. The hold time is the time interval between the sampling clock edge and the first change of the input signal. The diagram shows that the setup and hold times are both satisfied for the SMD1102/SMD1103.



Nonvolatile DACPOT™ Electronic Potentiometer With Up/Down Counter Interface

FEATURES

- Digitally Controlled Electronic Potentiometer
- 8-Bit Digital-to-Analog Converter (DAC)
 - Independent Reference Inputs
 - Differential Non-Linearity - $\pm 0.5\text{LSB}$
 - Integral Non-Linearity - $\pm 1\text{LSB}$
- V_{OUT} Value in $E^2\text{PROM}$ for Power-On Recall
 - Equivalent to 256-Step Potentiometer
- Unity Gain Op Amp Drives $\pm 100\mu\text{A}$
- Simple Trimming Adjustment
 - Up/Down Counter Style Operation
- Low Noise Operation
- “Clickless” Transitions between DAC Steps
- No Mechanical Wearout Problem
 - 1,000,000 Stores (typical)
 - 100 Year Data Retention
- Operation from +2.7V to +5.5V Supply
- Ultra-Low Power, 0.5mW max at +5V

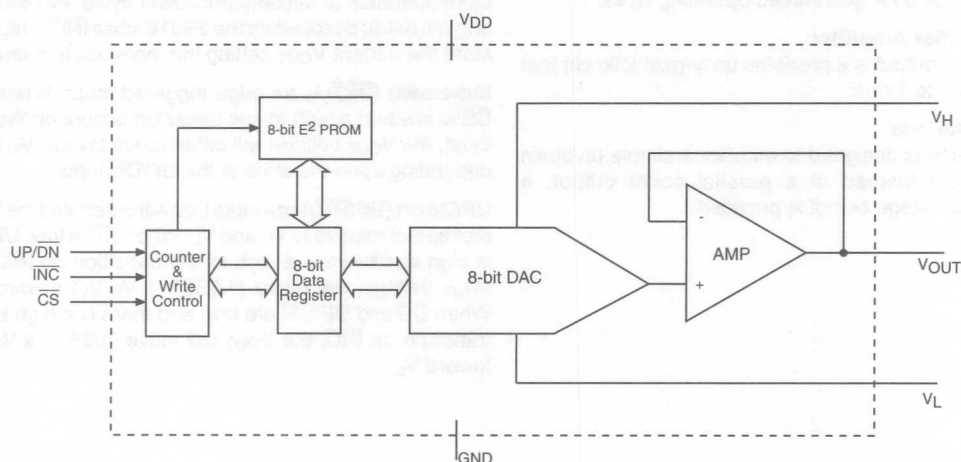
OVERVIEW

The S9318 DACPOT™ trimmer is an 8-bit nonvolatile DAC designed to replace mechanical potentiometers. The S9318 includes a unity-gain amplifier to buffer the DAC output and enables V_{OUT} to swing from rail to rail. The DACPOT trimmer operates over a supply voltage range of 2.7V to 5.5V.

The S9318's simple up/down counter input provides an ideal interface for automatic test equipment to dither and monitor the V_{OUT} voltage. This interface allows for quick and consistent calibration of even the most sophisticated systems.

The S9318 is a pin-compatible performance upgrade for other industry nonvolatile potentiometers. The S9318 offers double the resolution of these devices and provides 'clickless' transitions of V_{OUT} .

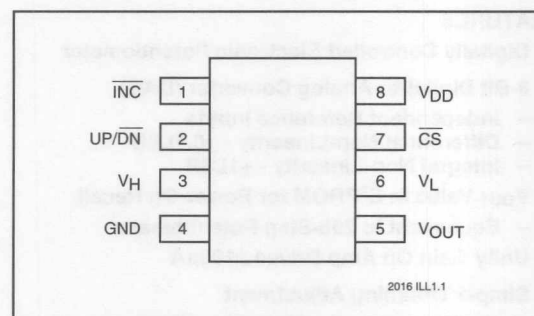
FUNCTIONAL BLOCK DIAGRAM



2016 ILL2.1

**PIN NAMES**

Symbol	Description
$\overline{\text{INC}}$	Increment Input, High to Low Edge Trigger
$\text{UP}/\overline{\text{DN}}$	Up/Down Input controlling relative V_{OUT} movement
V_{H}	V_{+} reference input
GND	Analog and Digital Ground
V_{OUT}	Trimmed Voltage Output
V_{L}	V_{-} reference input
$\overline{\text{CS}}$	Active low chip select input
V_{DD}	Supply Voltage (2.7V to 5.5V)

PINOUT**Analog Section**

The S9318 is an 8-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts an 8-bit value into equivalent analog output voltages in proportion to the applied reference voltage.

Reference Inputs

The voltage differential between the V_{L} and V_{H} inputs sets the full-scale output voltage range. V_{L} must be equal to or greater than ground (i.e. a positive voltage). V_{H} must be greater than V_{L} and less than or equal to V_{DD} . See table on page 3 for guaranteed operating limits.

Output Buffer Amplifier

The voltage output is a precision unity-gain follower that can slew up to $1\text{V}/\mu\text{s}$.

Digital Interface

The interface is designed to emulate a simple up/down counter, but instead of a parallel count output, a ratiometric voltage output is provided.

Chip Select ($\overline{\text{CS}}$) is an active low input. Whenever $\overline{\text{CS}}$ is high the S9318 is in standby mode and consumes the least power. This mode is equivalent to a potentiometer that is adjusted to the required setting. When $\overline{\text{CS}}$ is low the S9318 will recognize transitions on the $\overline{\text{INC}}$ input and will move the V_{OUT} either toward the V_{H} reference or toward the V_{L} reference depending upon the state of the $\text{UP}/\overline{\text{DN}}$ input.

The host may exit an adjustment routine in two ways: deselecting the S9318 while $\overline{\text{INC}}$ is low will not perform a store operation (a subsequent power cycle will recall the original data); deselecting the S9318 while $\overline{\text{INC}}$ is high will store the current V_{OUT} setting into nonvolatile memory.

Increment ($\overline{\text{INC}}$) is an edge triggered input. Whenever $\overline{\text{CS}}$ is low and a high to low transition occurs on the $\overline{\text{INC}}$ input, the V_{OUT} voltage will either move toward V_{H} or V_{L} depending upon the state of the $\text{UP}/\overline{\text{DN}}$ input.

UP/Down ($\text{UP}/\overline{\text{DN}}$) is an input that will determine the V_{OUT} movement relative to V_{H} and V_{L} . When $\overline{\text{CS}}$ is low, $\text{UP}/\overline{\text{DN}}$ is high and there is a high to low transition on $\overline{\text{INC}}$, the V_{OUT} voltage will move $(1/256^{\text{th}} \times V_{\text{H}} - V_{\text{L}})$ toward V_{H} . When $\overline{\text{CS}}$ and $\text{UP}/\overline{\text{DN}}$ are low, and there is a high to low transition on $\overline{\text{INC}}$, the V_{OUT} will move $(1/256^{\text{th}} \times V_{\text{H}} - V_{\text{L}})$ toward V_{L} .

**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on pins with reference to GND:	
Analog Inputs	-0.5V to V _{DD} +5V
Digital Inputs	-0.5V to V _{DD} +5V
Analog Outputs	-0.5V to V _{DD} +5V
Digital Outputs	-0.5V to V _{DD} +5V
Lead Solder Temperature (10 secs)	300°C

***COMMENT**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operation sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Condition	Min	Max
Temperature	-40°C	+85°C
V _{DD}	+2.7V	+5.5V

2016 PGM T1.1

DAC DC ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, V_{refH} = V_{DD}, V_{refL} = 0V, T_A = -40°C to +85°C, unless specified otherwise

	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Accuracy	INL	Integral Non-Linearity	I _{LOAD} = 50μA, T _R = C	-	0.6	±1	LSB
			T _R = I	-	0.6	±1	LSB
	DNL	Differential Non-Linearity	I _{LOAD} = 100μA, T _R = C	-	1.2	-	LSB
			T _R = I	-	1.2	-	LSB
References	V _H	V _{refH} Input Voltage		2.5	-	V _{DD}	V
	V _L	V _{refL} Input Voltage		Gnd	-	V _{DD} -2.5	V
	R _{IN}	V _{refH} to V _{refL} Resistance		-	38K	-	Ω
	TCR _{IN}	Temperature Coefficient of R _{IN}	V _{refH} to V _{refL}	-	700	-	ppm/°C
Analog Output	GEFS	Full-Scale Gain Error	DATA = FF	-	-	±1	LSB
	V _{OUTZS}	Zero-Scale Output Voltage	DATA = 00	0		20	mV
	TCV _{OUT}	V _{OUT} Temperature Coefficient	V _{DD} = +5, I _{LOAD} = 50μA, V _{refH} = +5V, V _{refL} = 0V	-	-	200	μV/°C
	I _L	Amplifier Output Load Current				100	μA
	R _{OUT}	Amplifier Output Resistance	I _L = 100μA	-	10		Ω
			+5V	-	20		Ω
			+3V				
	PSRR	Power Supply Rejection	I _{LOAD} = 10μA	-	-	1	LSB/V
	e _N	Amplifier Output Noise	f = 1KHz, V _{DD} = +5V	-	90	-	nV/√Hz
	THD	Total Harmonic Distortion	V _{IN} = 1V rms, f = 1KHz	-	0.08	-	%
	BW	Bandwidth - 3dB	V _{IN} = 100mV rms	-	1,000	-	kHz

2016 PGM T3.3

2016-03 4/17/98



RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Method
V _{ZAP}	ESD Susceptibility	2000		V	MS-883, TM 3015
I _{LTH}	Latch-Up	100		mA	JEDEC Standard 17
T _{DR}	Data Retention	100		Years	MS-883, TM 1008
N _{END}	Endurance	1,000,000		Stores	MS-883, TM 1033

2016 PGM T2.0

DC ELECTRICAL CHARACTERISTICS $V_{DD} = +2.7V$ to $+5.5V$, $V_H = V_{DD}$, $V_L = 0V$, Unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I _{DD}	Supply Current during store, note 1	CS = V _{IL}		1.0	mA
I _{SB}	Supply Standby Current	CS = V _{IH}		100	μA
I _{IH}	Input Leakage Current	V _{IN} = V _{DD}		10	μA
I _{IL}	Input Leakage Current, note 2	V _{IN} = 0V		-25	μA
V _{IH}	High Level Input Voltage		2	V _{DD}	V
V _{IL}	Low Level Input Voltage		0	0.8	V

2016 PGM T4.2

Notes:

1. I_{DD} is the supply current drawn while the EEPROM is being updated. I_{DD} does not include the current that flows through the Reference resistor chain.
2. \overline{CS} , UP/ \overline{DN} and \overline{INC} have internal pull-up resistors of approximately 200kΩ. When the input is pulled to ground the resulting output current will be V_{DD}/200kΩ.



OPERATIONAL TRUTH TABLE

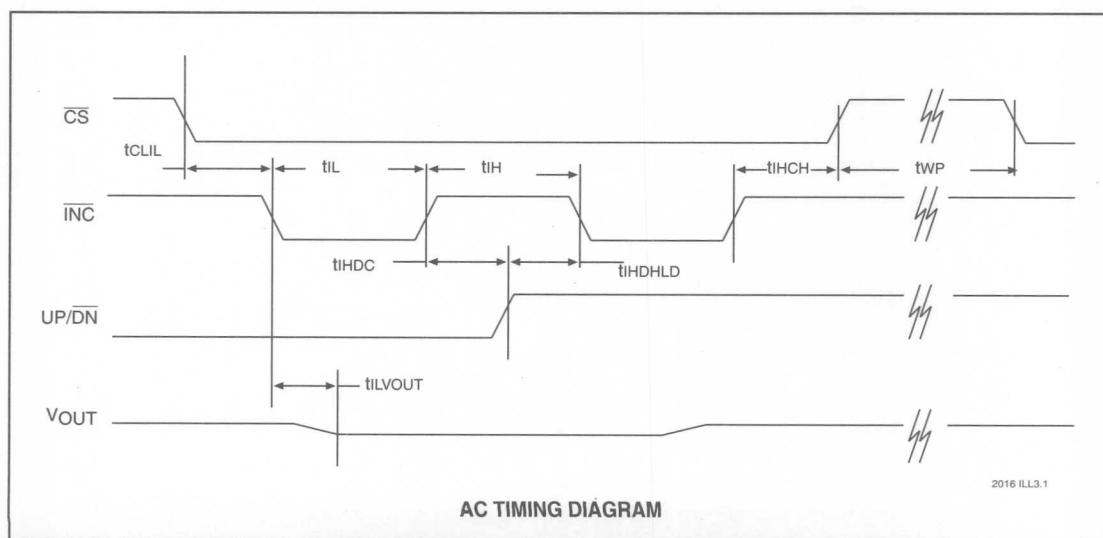
$\overline{\text{INC}}$	$\overline{\text{CS}}$	UP/DN	Operation
HI _{TO} LO	L	H	V _{OUT} toward V _H
HI _{TO} LO	L	L	V _{OUT} toward V _L
H	LO _{TO} HI	X	Store Setting
L	LO _{TO} HI	X	Maintain Setting, NO Store
V _{DD}	V _{DD}	V _{DD}	Standby

2016 PGM T5.1

AC TIMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t _{CLIL}	$\overline{\text{CS}}$ to $\overline{\text{INC}}$ Setup	100		ns
t _{IHDC}	$\overline{\text{INC}}$ High to UP/DN Change	100		ns
t _{DCIL}	UP/DN to $\overline{\text{INC}}$ Setup	100		ns
t _{IL}	$\overline{\text{INC}}$ Low Period	200		ns
t _{IH}	$\overline{\text{INC}}$ High Period	200		ns
t _{IHCH}	$\overline{\text{INC}}$ Inactive to $\overline{\text{CS}}$ Inactive	100		ns
t _{WP}	Write Cycle Time		5	ms
t _{ILVOUT}	$\overline{\text{INC}}$ to V _{OUT} Delay		5	μ s

2016 PGM T6.1



2016 ILL3.1

**Nonvolatile DACPOT™ Electronic Potentiometer
 With Up/Down Counter Interface**

Preliminary

FEATURES

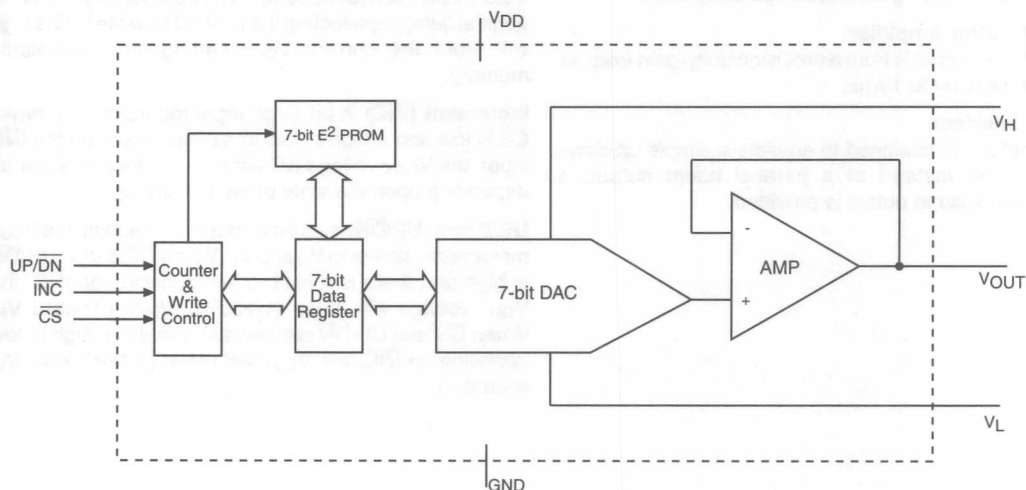
- Digitally Controlled Electronic Potentiometer
- 7-Bit Digital-to-Analog Converter (DAC)
 - Independent Reference Inputs
 - Differential Non-Linearity - $\pm 0.5\text{LSB}$
 - Integral Non-Linearity - $\pm 1\text{LSB}$
- V_{OUT} Value in EEPROM for Power-On Recall
 - Equivalent to 128-Step Potentiometer
- Unity Gain Op Amp Drives $\pm 100\mu\text{A}$
- Simple Trimming Adjustment
 - Up/Down Counter Style Operation
- Low Noise Operation
- “Clickless” Transitions between DAC Steps
- No Mechanical Wearout Problem
 - 1,000,000 Stores (typical)
 - 100 Year Data Retention
- Operation from +2.7V to +5.5V Supply
- Ultra-Low Power, 0.5mW max at +5V

OVERVIEW

The SMP9317 DACPOT™ trimmer is a 7-bit nonvolatile DAC designed to replace mechanical potentiometers. The SMP9317 includes a unity-gain amplifier to buffer the DAC output and enables V_{OUT} to swing from rail to rail. The DACPOT trimmer operates over a supply voltage range of 2.7V to 5.5V.

The SMP9317's simple up/down counter input provides an ideal interface for automatic test equipment to dither and monitor the V_{OUT} voltage. This interface allows for quick and consistent calibration of even the most sophisticated systems.

The SMP9317 is a pin-compatible performance upgrade for other industry nonvolatile potentiometers. The SMP9317 offers higher resolution than these devices and provides 'clickless' transitions of V_{OUT} .

FUNCTIONAL BLOCK DIAGRAM


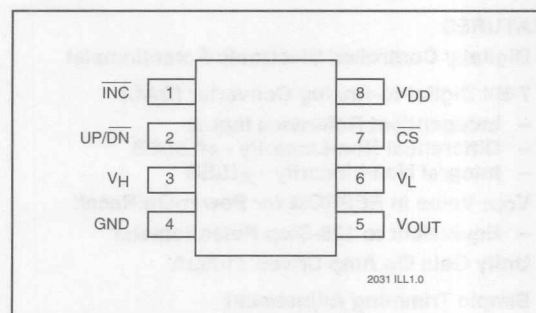
2031 ILL2.0



PIN NAMES

Symbol	Description
\overline{INC}	Increment Input, High to Low Edge Trigger
UP/\overline{DN}	Up/Down Input controlling relative V_{OUT} movement
V_H	V_+ reference input
GND	Analog and Digital Ground
V_{OUT}	Trimmed Voltage Output
V_L	V_- reference input
\overline{CS}	Active low chip select input
V_{DD}	Supply Voltage (2.7V to 5.5V)

PINOUT



Analog Section

The SMP9317 is a 7-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts a 7-bit value into equivalent analog output voltages in proportion to the applied reference voltage.

Reference Inputs

The voltage differential between the V_L and V_H inputs sets the full-scale output voltage range. V_L must be equal to or greater than ground (i.e. a positive voltage). V_H must be greater than V_L and less than or equal to V_{DD} . See table on page 3 for guaranteed operating limits.

Output Buffer Amplifier

The voltage output is from a precision unity-gain follower that can slew up to $1V/\mu s$.

Digital Interface

The interface is designed to emulate a simple up/down counter, but instead of a parallel count output, a ratiometric voltage output is provided.

Chip Select (\overline{CS}) is an active low input. Whenever \overline{CS} is high the SMP9317 is in standby mode and consumes the least power. This mode is equivalent to a potentiometer that is adjusted to the required setting. When \overline{CS} is low the SMP9317 will recognize transitions on the \overline{INC} input and will move the V_{OUT} either toward the V_H reference or toward the V_L reference depending upon the state of the UP/\overline{DN} input.

The host may exit an adjustment routine in two ways: deselecting the SMP9317 while \overline{INC} is low will not perform a store operation (a subsequent power cycle will recall the original data); deselecting the SMP9317 while \overline{INC} is high will store the current V_{OUT} setting into nonvolatile memory.

Increment (\overline{INC}) is an edge triggered input. Whenever \overline{CS} is low and a high to low transition occurs on the \overline{INC} input, the V_{OUT} voltage will either move toward V_H or V_L depending upon the state of the UP/\overline{DN} input.

UP/Down (UP/\overline{DN}) is an input that will determine the V_{OUT} movement relative to V_H and V_L . When \overline{CS} is low, UP/\overline{DN} is high and there is a high to low transition on \overline{INC} , the V_{OUT} voltage will move $(1/128^{th} \times V_H - V_L)$ toward V_H . When \overline{CS} and UP/\overline{DN} are low, and there is a high to low transition on \overline{INC} , the V_{OUT} will move $(1/128^{th} \times V_H - V_L)$ toward V_L .

**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on pins with reference to GND:	
Analog Inputs	-0.5V to V _{DD} +5V
Digital Inputs	-0.5V to V _{DD} +5V
Analog Outputs	-0.5V to V _{DD} +5V
Digital Outputs	-0.5V to V _{DD} +5V
Lead Solder Temperature (10 secs)	300°C

***COMMENT**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operation sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Condition	Min	Max
Temperature	-40°C	+85°C
V _{DD}	+2.7V	+5.5V

2031 PGM T1.0

DAC DC ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, V_{refH} = V_{DD}, V_{refL} = 0V, T_A = -40°C to +85°C, unless specified otherwise

	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Accuracy	INL	Integral Non-Linearity	I _{LOAD} = 50μA, T _R = C	-	0.6	±1	LSB
				-	0.6	±1	LSB
			I _{LOAD} = 100μA, T _R = C	-	1.2	-	LSB
				-	1.2	-	LSB
	DNL	Differential Non-Linearity	I _{LOAD} = 50μA, T _R = C	-	0.25	±0.5	LSB
				-	0.25	±0.5	LSB
			I _{LOAD} = 100μA, T _R = C	-	0.5	-	LSB
				-	0.5	-	LSB
References	V _H	V _{refH} Input Voltage		2.5	-	V _{DD}	V
	V _L	V _{refL} Input Voltage		Gnd	-	V _{DD} -2.5	V
	R _{IN}	V _{refH} to V _{refL} Resistance		-	38K	-	Ω
	TC _{RIN}	Temperature Coefficient of R _{IN}	V _{refH} to V _{refL}	-	700	-	ppm/°C
Analog Output	G _{EFS}	Full-Scale Gain Error	DATA = FF	-	-	±1	LSB
	V _{OUTZS}	Zero-Scale Output Voltage	DATA = 00	0		20	mV
	TC _{VOUT}	V _{OUT} Temperature Coefficient	V _{DD} = +5, I _{LOAD} = 50μA, V _{refH} = +5V, V _{refL} = 0V	-	-	200	μV/°C
	I _L	Amplifier Output Load Current				100	μA
	R _{OUT}	Amplifier Output Resistance	I _L = 100μA	-	10		Ω
			+5V	-	20		Ω
			+3V	-			
	PSRR	Power Supply Rejection	I _{LOAD} = 10μA	-	-	1	LSB/V
	e _N	Amplifier Output Noise	f = 1KHz, V _{DD} = +5V	-	90	-	nV/√Hz
	THD	Total Harmonic Distortion	V _{IN} = 1V rms, f = 1KHz	-	0.08	-	%
	BW	Bandwidth - 3dB	V _{IN} = 100mV rms	-	1,000	-	kHz

2031 PGM T3.1

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**RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Min	Max	Unit	Test Method
V_{ZAP}	ESD Susceptibility	2000		V	MS-883, TM 3015
I_{LTH}	Latch-Up	100		mA	JEDEC Standard 17
T_{DR}	Data Retention	100		Years	MS-883, TM 1008
N_{END}	Endurance	1,000,000		Stores	MS-883, TM 1033

2031 PGM T2.0

DC ELECTRICAL CHARACTERISTICS $V_{DD} = +2.7V$ to $+5.5V$, $V_H = V_{DD}$, $V_L = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, Unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{DD}	Supply Current during store, note 1	$CS = V_{IL}$		1.0	mA
I_{SB}	Supply Standby Current	$CS = V_{IH}$		100	μA
I_{IH}	Input Leakage Current	$V_{IN} = V_{DD}$		10	μA
I_{IL}	Input Leakage Current, note 2	$V_{IN} = 0V$		-25	μA
V_{IH}	High Level Input Voltage		2	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V

2031 PGM T4.0

Notes:

1. I_{DD} is the supply current drawn while the EEPROM is being updated. I_{DD} does not include the current that flows through the Reference resistor chain.
2. CS , UP/DN and INC have internal pull-up resistors of approximately $200k\Omega$. When the input is pulled to ground the resulting output current will be $V_{DD}/200k\Omega$.

**OPERATIONAL TRUTH TABLE**

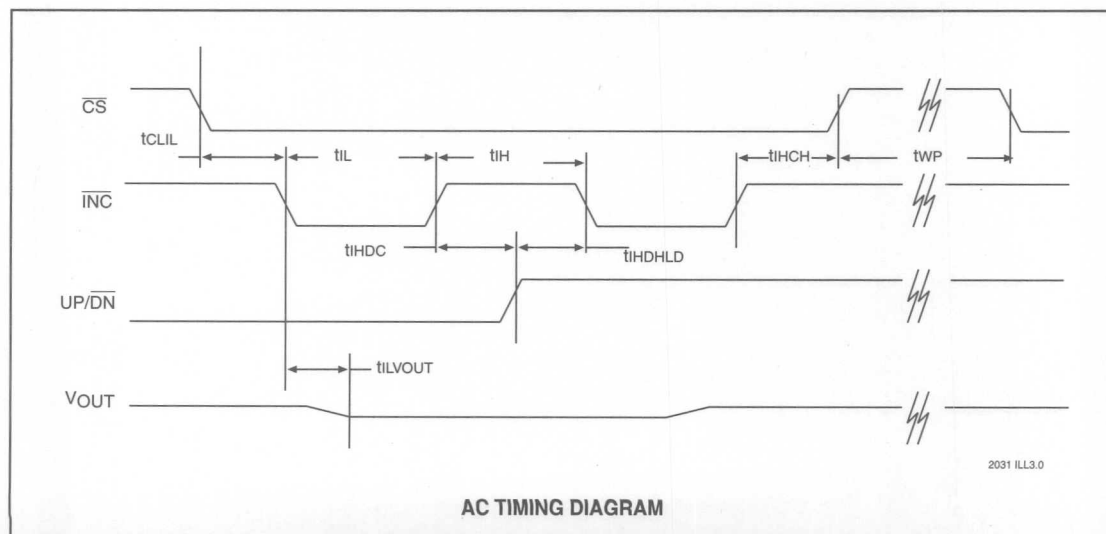
$\overline{\text{INC}}$	$\overline{\text{CS}}$	UP/DN	Operation
HiToLo	L	H	V _{OUT} toward V _H
HiToLo	L	L	V _{OUT} toward V _L
H	LOToHI	X	Store Setting
L	LOToHI	X	Maintain Setting, NO Store
V _{DD}	V _{DD}	V _{DD}	Standby

2031 PGM T5.0

AC TIMING CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
t _{CLIL}	$\overline{\text{CS}}$ to $\overline{\text{INC}}$ Setup	100		ns
t _{IHDC}	$\overline{\text{INC}}$ High to UP/DN Change	100		ns
t _{DCIL}	UP/DN to $\overline{\text{INC}}$ Setup	100		ns
t _{IL}	$\overline{\text{INC}}$ Low Period	200		ns
t _{IH}	$\overline{\text{INC}}$ High Period	200		ns
t _{IHCH}	$\overline{\text{INC}}$ Inactive to $\overline{\text{CS}}$ Inactive	100		ns
t _{WP}	Write Cycle Time		5	ms
t _{ILVOUT}	$\overline{\text{INC}}$ to V _{OUT} Delay		5	μs

2031 PGM T6.0



2031 ILL3.0



SMP9317

Preliminary

Station	Depth	Time	Remarks
100	10	10:00	Start of run
100	10	10:05	100 fathoms
100	10	10:10	100 fathoms
100	10	10:15	100 fathoms
100	10	10:20	100 fathoms
100	10	10:25	100 fathoms
100	10	10:30	100 fathoms
100	10	10:35	100 fathoms
100	10	10:40	100 fathoms
100	10	10:45	100 fathoms
100	10	10:50	100 fathoms
100	10	10:55	100 fathoms
100	10	11:00	End of run

Station	Depth	Time	Remarks
100	10	11:05	100 fathoms
100	10	11:10	100 fathoms
100	10	11:15	100 fathoms
100	10	11:20	100 fathoms
100	10	11:25	100 fathoms
100	10	11:30	100 fathoms
100	10	11:35	100 fathoms
100	10	11:40	100 fathoms
100	10	11:45	100 fathoms
100	10	11:50	100 fathoms
100	10	11:55	100 fathoms
100	10	12:00	End of run



**Nonvolatile DACPOT™ Electronic Potentiometer
 With Debounced Push Button Interface**
FEATURES
Digitally Controlled Electronic Potentiometer

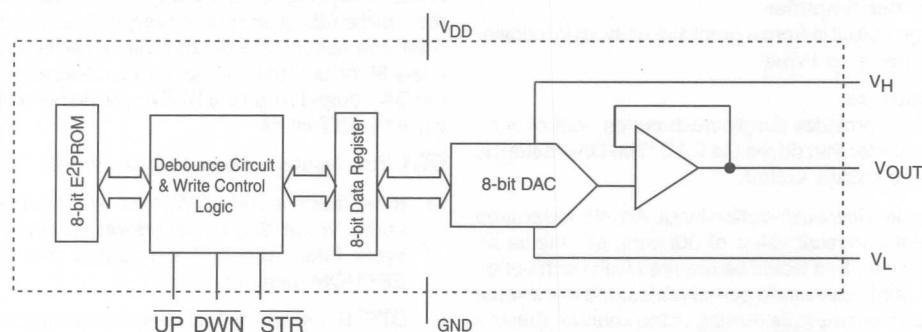
- **8-Bit Digital-to-Analog Converter (DAC)**
 - Independent Reference Inputs
 - Differential Non-Linearity - $\pm 0.5\text{LSB}$
 - Integral Non-Linearity - $\pm 1\text{LSB}$
- **V_{OUT} Value in EEPROM for Power-On Recall**
 - Equivalent to 256-Step Potentiometer
- **Unity Gain Op Amp Drives $\pm 100\mu\text{A}$**
- **Simple Trimming Adjustment**
 - Debounced Push Button Interface
- **Low Noise Operation**
- **"Clickless" Transitions between DAC Steps**
- **No Mechanical Wearout Problem**
 - 1,000,000 Stores (typical)
 - 100 Year Data Retention
- **Operation from +2.7V to +5.5V Supply**
- **Ultra-Low Power, 0.5mW max at +5V**

OVERVIEW

The S9518 DACPOT trimmer is an 8-bit nonvolatile DAC designed to replace mechanical potentiometers. The S9518 includes a unity-gain amplifier to buffer the DAC output and enables V_{OUT} to swing from rail to rail. The DACPOT trimmer operates over a supply voltage range of 2.7V to 5.5V.

The S9518's simple push button input provides an ideal interface for operator adjusted equipment. This interface allows for quick and easy adjustment of even the most sophisticated systems.

The S9518 is a pin-compatible performance upgrade for other industry nonvolatile potentiometers. The S9518 offers double the resolution of these devices and provides 'clickless' transitions of V_{OUT}.

FUNCTIONAL BLOCK DIAGRAM


**PIN NAMES**

Symbol	Description
\overline{UP}	PB Input, Moves V_{OUT} Toward V_H Input
\overline{DWN}	PB Input, Moves V_{OUT} Toward V_L Input
V_H	Vref High
GND	Ground
V_{OUT}	Trimmed Voltage Output
V_L	Vref Low
\overline{STR}	Store Input, Providing a Control Input to Initiate a Store Operation
V_{DD}	Supply Voltage (2.7V to 5.5V)

2017 PGM T1.0

Analog Section

The S9518 is an 8-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts 8-bit digital values into equivalent analog output voltages in proportion to the applied reference voltage.

Reference Inputs

The voltage differential between the V_L and V_H inputs sets the full-scale output voltage range. V_L must be equal to or greater than ground (a positive voltage). V_H must be greater than V_L and less than or equal to V_{DD} . See specifications on page 5 for guaranteed operating limits.

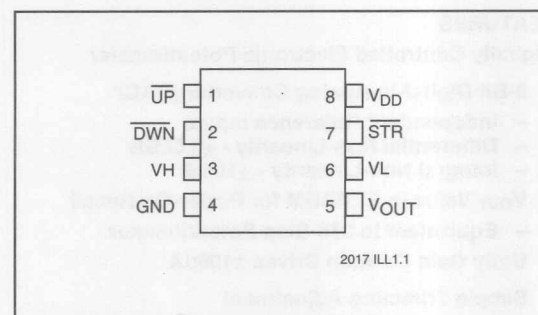
Output Buffer Amplifier

The voltage output is from a precision unity-gain follower that can slew up to 1V/ μ s.

Digital Interface

The interface provides simple push button control of an up/down counter that drives the DAC. The DAC output is a ratiometric voltage output.

\overline{UP} is an active low push-button input. An internal pull-up resistor, with nominal value of 50k Ω , eliminates an external resistor that would be required with push button control. A 30ms debounce period is included in the input timing to prevent multiple pulsing of the counter. Either a switch closure to ground or a LOW logic level will, after the debounce time, change the potentiometer tap position. \overline{UP} moves the output voltage towards the V_H reference input. If the \overline{UP} push-button is kept depressed, the counter will continue to increment at the rate of one count every 250ms for one second. After one second the

PINOUT

counter increments faster, one count every 50ms, until the push-button is released. Changes to the DAC output using the \overline{UP} input do not alter the data stored in EEPROM. The \overline{STR} input updates the nonvolatile EEPROM memory.

\overline{DWN} is an active low push-button input that decrements the counter and moves the potentiometer output voltage towards the V_L reference input. The \overline{DWN} control input also includes an internal 50k Ω pull-up resistor and a 30ms debounce period to prevent multiple pulsing. A LOW logic level will also change the potentiometer tap position after the debounce period. If the \overline{DWN} push-button is kept depressed, the counter continues to decrement at the rate of one count every 250ms for one second. After one second the counter decrements at one count every 50ms until the push-button is released. Changes to the DAC output using the \overline{DWN} input do not alter the data stored in EEPROM.

\overline{STR} This input can be used in two ways:

- 1) If the input is tied LOW, then AUTOSTORE is enabled. When V_{DD} powers-down an automatic store cycle takes place that updates the nonvolatile EEPROM memory.
- 2) \overline{STR} is an active low push-button input that also updates the nonvolatile memory. The input is debounced but does not have an internal pull-up resistor. For every valid push, the S9518 will store the current potentiometer position to EEPROM.



DEVICE OPERATION

There are five main blocks to the S9518: an 8-bit EEPROM memory; input debounce circuits, control logic, and 8-bit counter; 8-bit data register; decode section and resistor ladder (DAC); and the buffer amplifier. The input control section operates just like an up/down counter. The output of this counter is fed to the data register and then decoded to activate one of 255 electronic switches connected to the resistor ladder. Each switch connects a point on the ladder to the buffer amplifier input. When requested, the contents of the counter can be stored in EEPROM memory and retained for future use. The ladder is comprised of 256 resistors of equal value connected in series. At the bottom of the ladder and at the junctions of the resistors there are electronic switches that transfer the voltage at each point to the buffer amplifier and hence to the output. The S9518 is designed to interface directly to two push button switches that effectively move the potentiometer wiper up or down. The \overline{UP} and \overline{DWN} inputs increment or decrement the 8-bit counter respectively. The data input to the DAC is decoded to select one of the 256 wiper positions along the resistive ladder. The wiper increment input, \overline{UP} and the wiper decrement input, \overline{DWN} are connected to internal pull-ups so that they normally remain HIGH. When pulled LOW by an external push button switch or a logic LOW level input, the wiper will be switched to the next adjacent tap position. Internal debounce circuitry prevents inadvertent switching of the wiper position if \overline{UP} or \overline{DWN} remain LOW for less than 30ms (typical). Each of the buttons can be pushed either once for a single increment/decrement or held low continuously for a multiple increments/decrements. The number of increments/decrements of the wiper position

depends on how long the button is pushed. When making a continuous push, after the first second, the increment/decrement speed increases. For the first second the device will be in the slow scan mode. Then if the button is held for longer than one second the device will go into the fast scan mode. As soon as the button is released the S9518 will return to a standby condition. The DAC, whether set to 00 or FF, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked beyond FF or below 00.

AUTOSTORE

The value of the counter is stored in EEPROM memory whenever the chip senses a power-down of V_{DD} while \overline{STR} is enabled (held LOW). When power is restored, the contents of the memory are recalled and the counter reset to the last value stored. If AUTOSTORE is to be implemented, \overline{STR} is typically hard wired to GND. If \overline{STR} is held HIGH during power-up and then taken LOW, the wiper will not respond to the \overline{UP} or \overline{DWN} inputs until \overline{STR} is brought HIGH and the store is complete. Figure 1.

Manual (Push Button) Store

When \overline{STR} is not enabled (held HIGH) a push button switch may be used to pull \overline{STR} LOW and released to perform a manual store of the wiper position in EEPROM memory. Figure 2.

Effect of V_{DD} Removal

The resistor ladder, connected between V_H and V_L , does not change value when V_{DD} is removed. However, the buffer amplifier no longer functions and consequently a high impedance appears at the V_{OUT} pin.

Figure 1: Typical circuit with \overline{STR} store pin used in AUTOSTORE mode

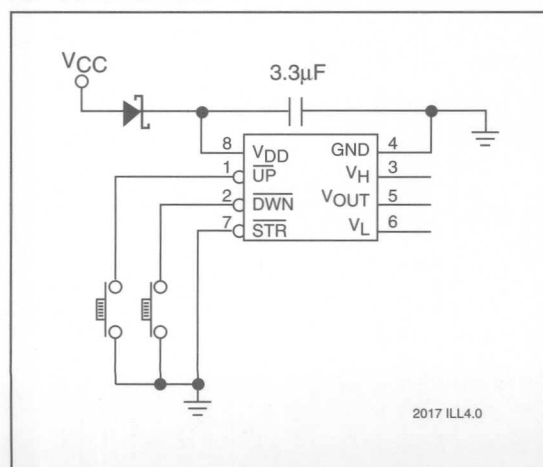
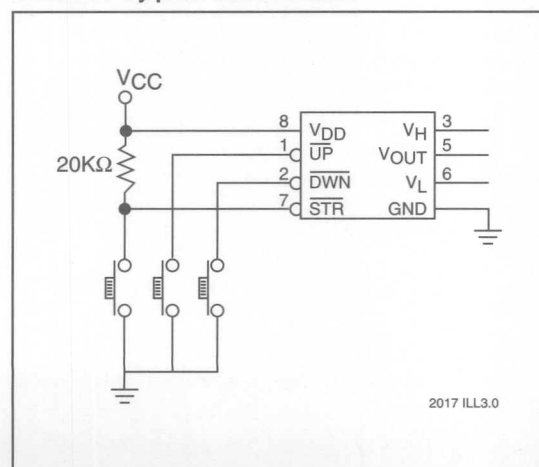


Figure 2: Typical circuit with \overline{STR} store pin controlled by push button switch



**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on pins with reference to GND:	
Analog Inputs	-0.5V to $V_{DD}+0.5V$
Digital Inputs	-0.5V to $V_{DD}+0.5V$
Analog Outputs	-0.5V to $V_{DD}+0.5V$
Digital Outputs	-0.5V to $V_{DD}+0.5V$
Lead Solder Temperature (10 secs)	300°C

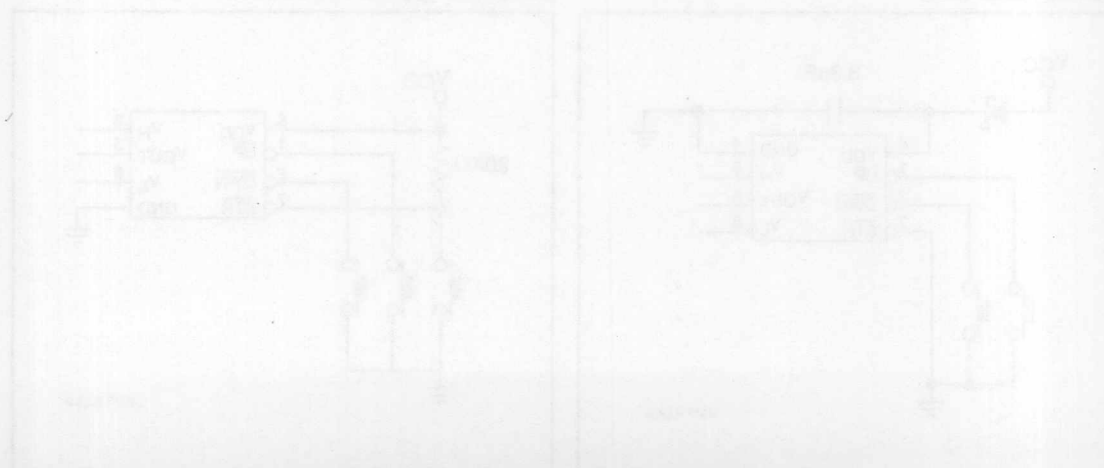
***COMMENT**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operation sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Condition	Min	Max
Temperature	-40°C	+85°C
V_{DD}	+2.7V	+5.5V

2017 PGM T2.2



**DAC DC ELECTRICAL CHARACTERISTICS**

$V_{DD} = +2.7V$ to $+5.5V$, $V_{refH} = V_{DD}$, $V_{refL} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless specified otherwise

	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Accuracy	INL	Integral Non-Linearity	$I_{LOAD} = 50\mu A$, $T_R = C$	-	0.6	± 1	LSB
			$T_R = I$	-	0.6	± 1	LSB
			$I_{LOAD} = 100\mu A$, $T_R = C$	-	1.2	-	LSB
			$T_R = I$	-	1.2	-	LSB
	DNL	Differential Non-Linearity	$I_{LOAD} = 50\mu A$, $T_R = C$	-	0.25	± 0.5	LSB
			$T_R = I$	-	0.25	± 0.5	LSB
			$I_{LOAD} = 100\mu A$, $T_R = C$	-	0.5	-	LSB
			$T_R = I$	-	0.5	-	LSB
References	V_H	V_{refH} Input Voltage		2.5	-	V_{DD}	V
	V_L	V_{refL} Input Voltage		Gnd	-	$V_{DD}-2.5$	V
	R_{IN}	V_{refH} to V_{refL} Resistance		-	38k	-	Ω
	TCR_{IN}	Temperature Coefficient of R_{IN}	V_{refH} to V_{refL}	-	700	-	ppm/ $^{\circ}C$
Analog	$GEFS$	Full-Scale Gain Error	DATA = FF			± 1	LSB
Output	V_{OUTZS}	Zero-Scale Output Voltage	DATA = 00	0		20	mV
	TCV_{OUT}	V_{OUT} Temperature Coefficient	$V_{DD} = +5$, $I_{LOAD} = 50\mu A$, $V_{refH} = +5V$, $V_{refL} = 0V$	-	-	200	$\mu V/^{\circ}C$
	I_L	Amplifier Output Load Current				100	μA
	R_{OUT}	Amplifier Output Resistance	$I_{LOAD} = 100\mu A$, $+5V$, $+3V$	-	10 20		Ω Ω
	$PSRR$	Power Supply Rejection	$I_{LOAD} = 10\mu A$	-	-	1	LSB/V
	e_N	Amplifier Output Noise	$f = 1kHz$, $V_{DD} = +5V$	-	90	-	nV/ \sqrt{Hz}
	THD	Total Harmonic Distortion	$V_{IN} = 1V$ rms, $f = 1kHz$	-	0.08	-	%
	BW	Bandwidth - 3dB	$V_{IN} = 100mV$ rms	-	1,000	-	kHz

2017 PGM T3.3

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Method
V_{ZAP}	ESD Susceptibility	2000		V	MS-883, TM 3015
I_{LTH}	Latch-Up	100		mA	JEDEC Standard 17
T_{DR}	Data Retention	100		Years	MS-883, TM 1008
N_{END}	Endurance	1,000,000		Stores	MS-883, TM 1033

2017 PGM T4.0

**DC ELECTRICAL CHARACTERISTICS** $V_{DD} = +2.7V$ to $+5.5V$, $V_H = V_{DD}$, $V_L = 0V$, Unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{DD}	Supply Current during store, note 1	$\overline{STR} = \text{[square wave]}$		1.0	mA
I_{SB}	Supply Standby Current			100	μA
I_{IH}	Input Leakage Current	$V_{IN} = V_{DD}$		10	μA
I_{IL}	Input Leakage Current, note 2	$V_{IN} = 0V$		-100	μA
V_{IH}	High Level Input Voltage		2	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	0.8	V

2017 PGM T5.0

Notes:

1. I_{DD} is the supply current drawn while the EEPROM is being updated. I_{DD} does not include the current that flows through the Reference resistor chain.
2. \overline{UP} and \overline{DWN} have internal pull-up resistors of approximately 50k Ω . When the input is pulled to ground the resulting output current will be $V_{DD}/50k\Omega$.

AC OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
f_{GAP}	Time Between Two Separate Push Button Events	0			μs
t_{DB}	Debounce Time		30	60	ms
$t_{S\ SLOW}$	After Debounce to Wiper Change on a Slow Mode	100	250	375	ms
$t_{S\ FAST}$	Wiper Change on a Fast Mode	25	50	75	ms
t_{PU}	Power-Up to Wiper Stable			500	μs
$t_R\ V_{DD}$	V_{DD} Power-Up Rate	0.2		50	mV/ μs
t_{ASTO}	AUTOSTORE Cycle Time	2			ms
t_{ASTH}	AUTOSTORE Threshold Voltage		4		V
t_{ASEND}	AUTOSTORE Cycle End Voltage		3.5		V

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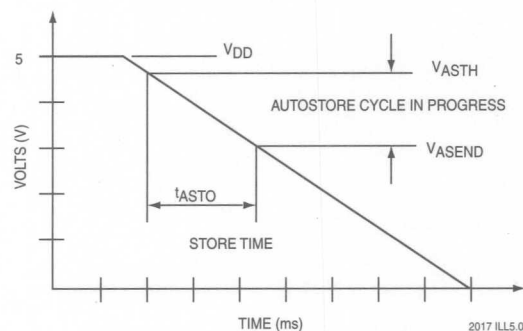


FIGURE 3. AUTOSTORE CYCLE TIMING DIAGRAM

Notes:

VASTH - AUTOSTORE threshold voltage

VASEND - AUTOSTORE cycle end voltage

tASTO - AUTOSTORE cycle time

(6) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

(7) This parameter is periodically sampled and not 100% tested.

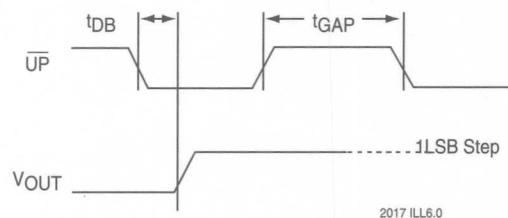


FIGURE 4. SLOW MODE TIMING

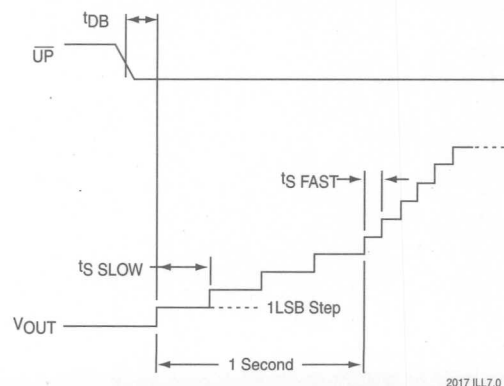


FIGURE 5. FAST MODE TIMING

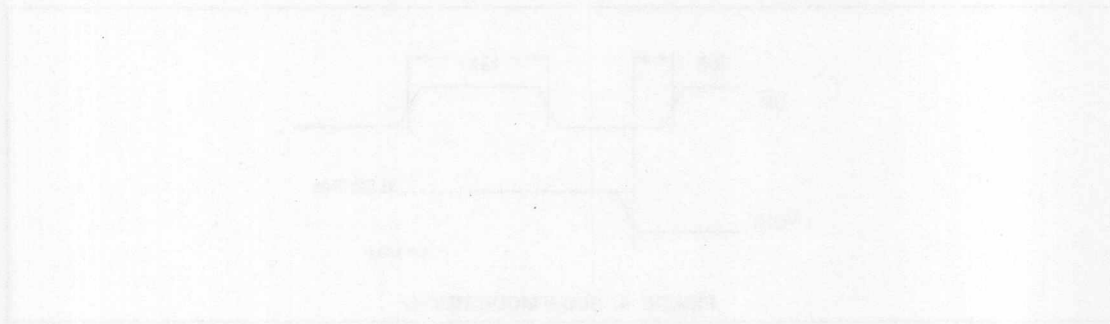


S9518

Preliminary



Figure 1: A line graph showing a linear increase over time. The x-axis is labeled 'Time' and the y-axis is labeled 'Value'. The line starts at the origin and rises steadily. There are some faint labels on the axes, but they are not legible.





SECTION 9 **Voltage Protected Nonvolatile Memories**

S24VP02 Low V _{CC} Write Protected 2K I ² C Memory	9-3
S24VP04 Low V _{CC} Write Protected 4K I ² C Memory	9-15
S24VP16 Low V _{CC} Write Protected 16K I ² C Memory	9-27
S93VP662 Low V _{CC} Write Protected 4K Microwire Memory in a x8 Data Configuration	9-39
S93VP663 Low V _{CC} Write Protected 4K Microwire Memory in a x16 Data Configuration	9-39

2K Serial E²PROM with a Precision Low-V_{CC} Lockout Circuit 3 and 5 Volt Systems

FEATURES

- **Voltage Protection™**
- **Precision Low-V_{CC} Write Lockout**
- **All Write Operations Inhibited When V_{CC} Falls below V_{LOCK}**
- **One 3Volt and Two 5Volt System Versions**
 - V_{LOCK} = 2.6V ± .1V / - .05V
 - V_{LOCK} = 4.25V ± .25V / - 0.0V
 - V_{LOCK} = 4.50 ± .25V / - 0.0V
- **100% Compatible with Industry Standard I²C™ Devices**
 - Bi-directional data transfer protocol
 - Standard 100kHz and 400kHz Transfer Rates
- **16-Byte Page-Write Mode**
 - Minimizes total write time per byte
- **1,000,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Commercial Industrial Temperature Range**

OVERVIEW

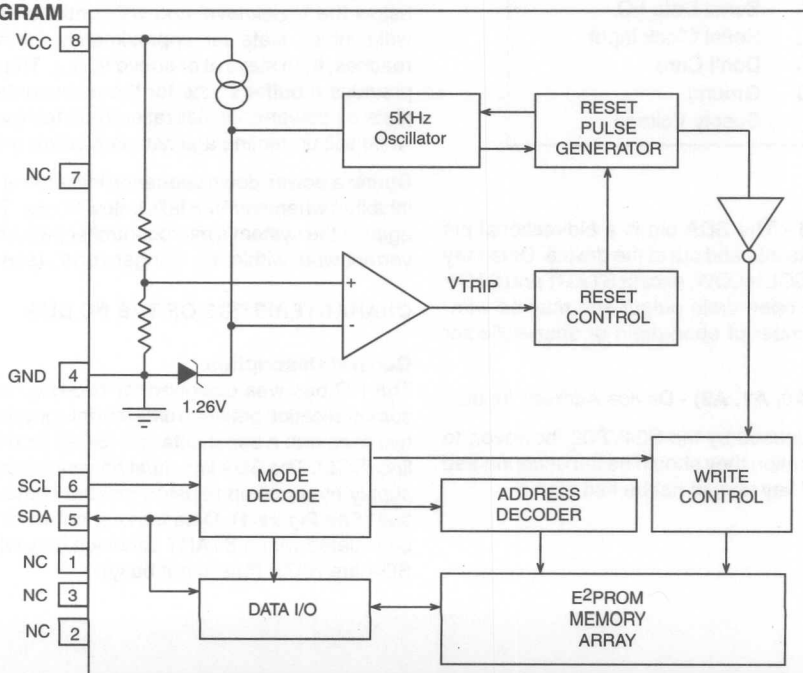
The S24VP02 is a 2K-bit serial E²PROM memory integrated with a precision V_{CC} sense circuit. The sense circuit will disable write operations whenever V_{CC} falls below the V_{LOCK} voltage. It is fabricated using SUMMIT's advanced CMOS E²PROM technology and is suitable for both 3 and 5 volt systems.

The S24VP02 is internally organized as 256 x 8. It features the I²C serial interface and software protocol allowing operation on a simple two-wire bus.

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

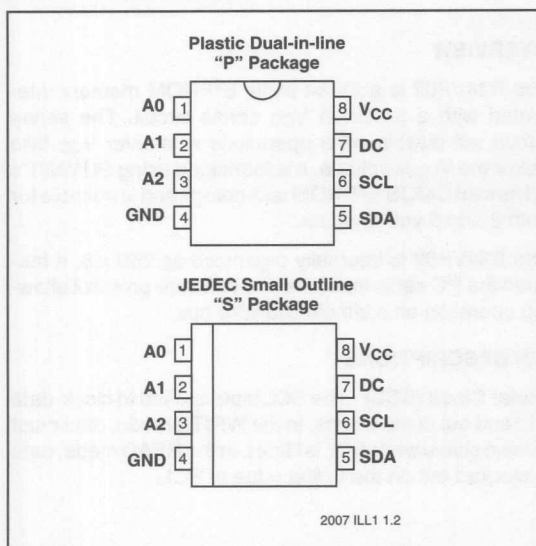
BLOCK DIAGRAM



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PIN CONFIGURATIONS



PIN NAMES

A0, A1, A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
DC	Don't Care
GND	Ground
VCC	Supply Voltage

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

Address Inputs (A0, A1, A2) - Device Address Inputs

These inputs are unused by the S24VP02; however, to ensure proper operation they should be left unconnected or tied to ground. They should not be tied high.

ENDURANCE AND DATA RETENTION

The S24VP02 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

DEVICE OPERATION

APPLICATIONS

The S24VP02 was designed specifically for applications where the integrity of the stored data is paramount. In recent years, as the operating voltage range of serial E²PROMs has widened, most semiconductor manufacturers have arbitrarily eliminated their V_{CC} sense circuits. The S24VP02 will protect your data by guaranteeing write lockout below the selected V_{CC} Lockout voltage.

V_{CC} Lockout

The S24VP02 has an on-board precision V_{CC} sense circuit. Whenever V_{CC} is below V_{LOCK}, the S24VP02 will disable the internal write circuitry. The V_{CC} lockout circuit will ensure a higher level of data integrity than can be expected from industry standard devices that have either a very loose specification or no V_{CC} lockout specification.

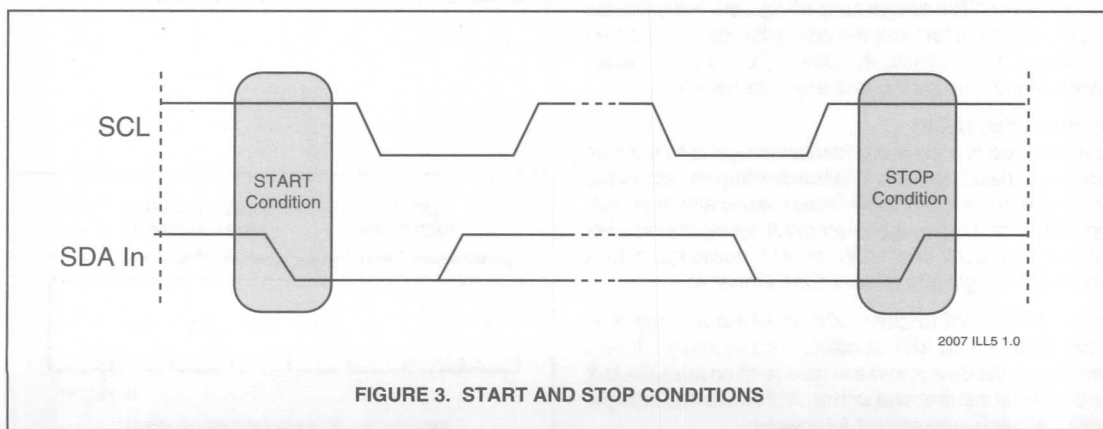
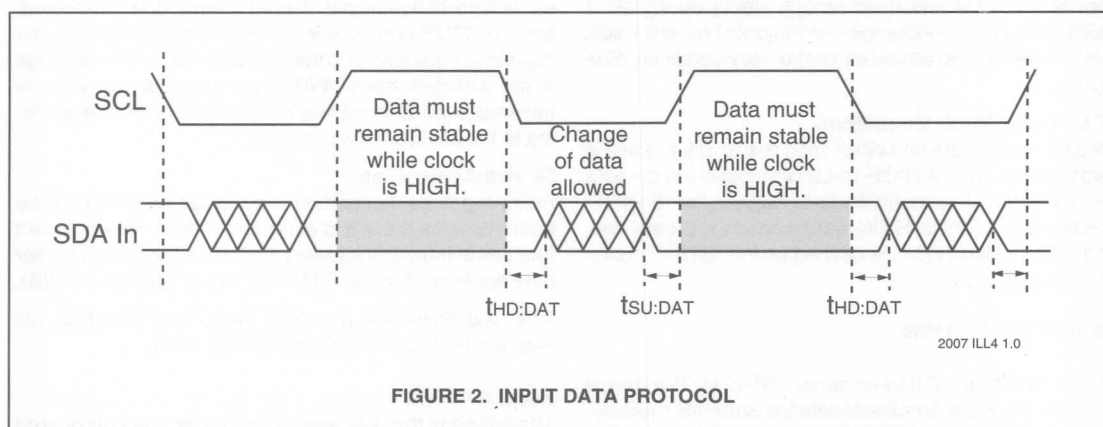
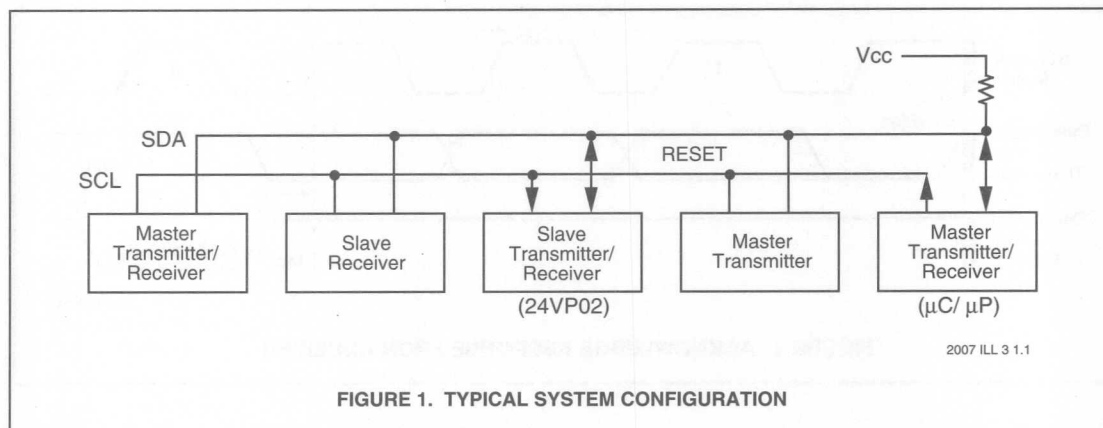
During a power-on sequence all writes will be inhibited below the V_{LOCK} level and will continue to be held in a write inhibit state for approximately 200ms after V_{CC} reaches, then stays at or above V_{LOCK}. The 200ms delay provides a buffer space for the microcontroller to complete its power-on initialization routines (reading is OK) while still protecting against inadvertent writes.

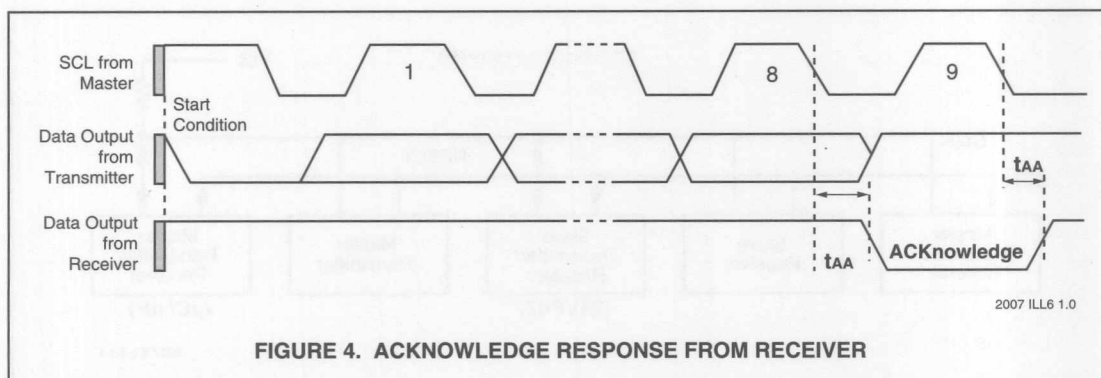
During a power-down sequence initiation of writes will be inhibited whenever V_{CC} falls below V_{LOCK}. This will guard against the system's microcontroller performing an inadvertent write within the 'danger zone'. (see AN001)

CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).





Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition (See Figure 2).

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 3).

DEVICE OPERATION

The S24VP02 is a 2,048-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S24VP02 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 4).

The S24VP02 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S24VP02 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S24VP02 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S24VP02 will continue to transmit data. If an ACKnowledge is not detected, the S24VP02 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

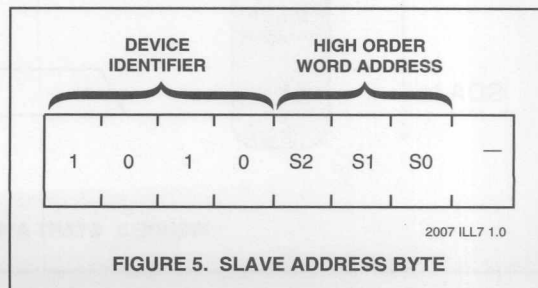
Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 5). For the S24VP02 this is fixed as 1010[B].

The next three bits are don't care. The S24VP02 will respond to all commands for device 1010.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.





WRITE OPERATIONS

The S24VP02 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 8 bytes in the same page to be written during t_{WR} .

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 256 words in the array.

Upon receipt of the word address, the S24VP02 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S24VP02 begins the internal write cycle.

While the internal write cycle is in progress, the S24VP02 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S24VP02 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more bytes of data. After the receipt of each byte, the S24VP02 will respond with an ACKnowledge.

The S24VP02 automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

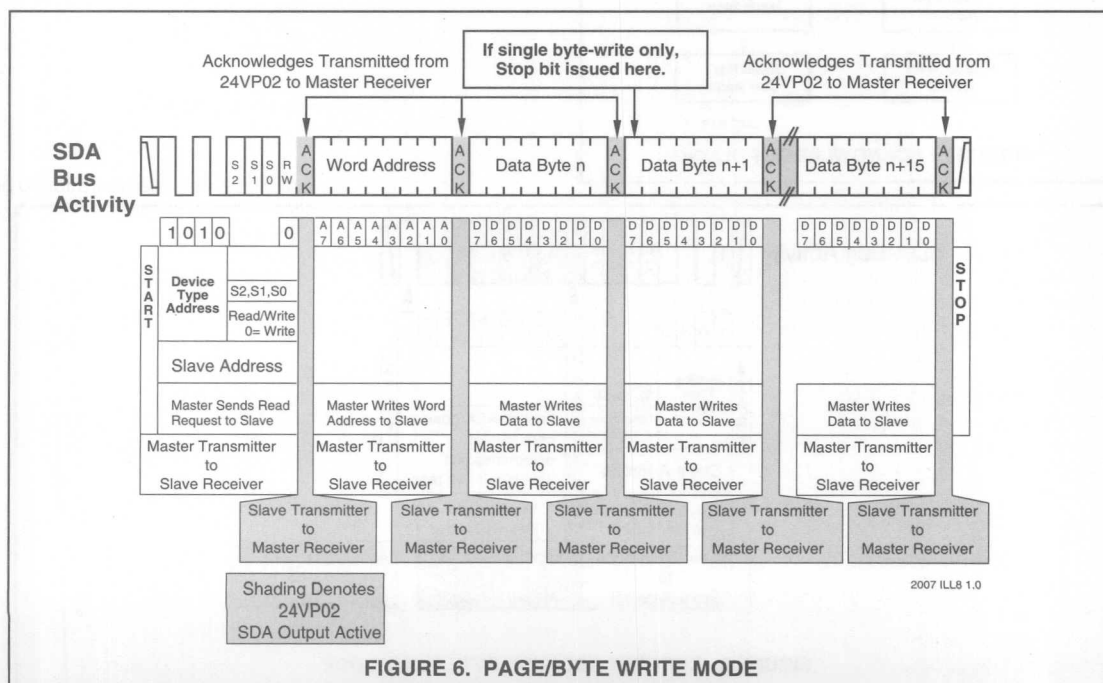


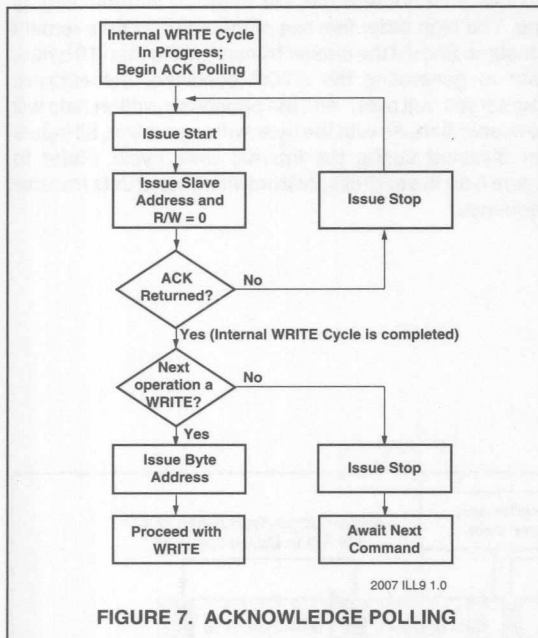
FIGURE 6. PAGE/BYTE WRITE MODE



Acknowledge Polling

When the S24VP02 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).



READ OPERATIONS

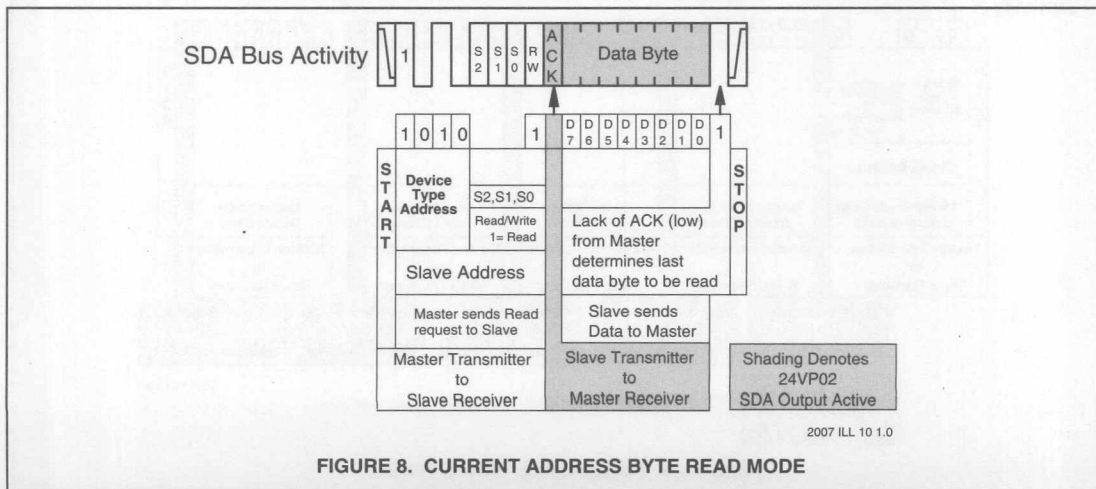
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S24VP02 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n , the next read operation would access data from address location $n+1$ and increment the current address pointer. When the S24VP02 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location $n+1$.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S24VP02 discontinues data transmission. See Figure 8 for the address acknowledge and data transfer sequence.

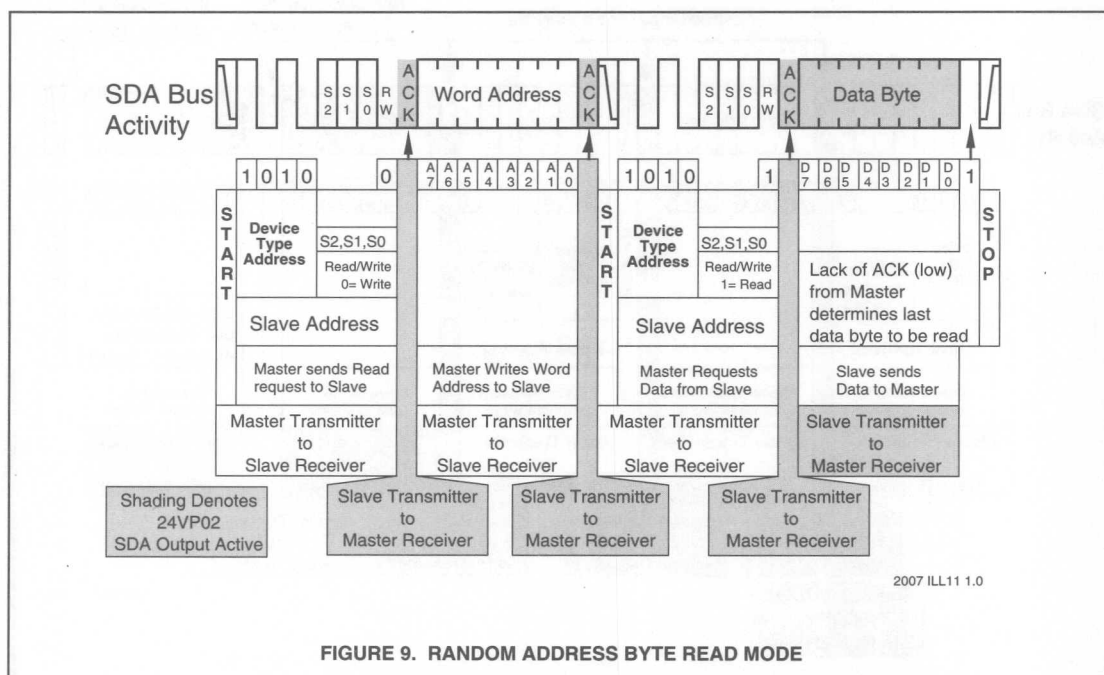




Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S24VP02 to the desired address.

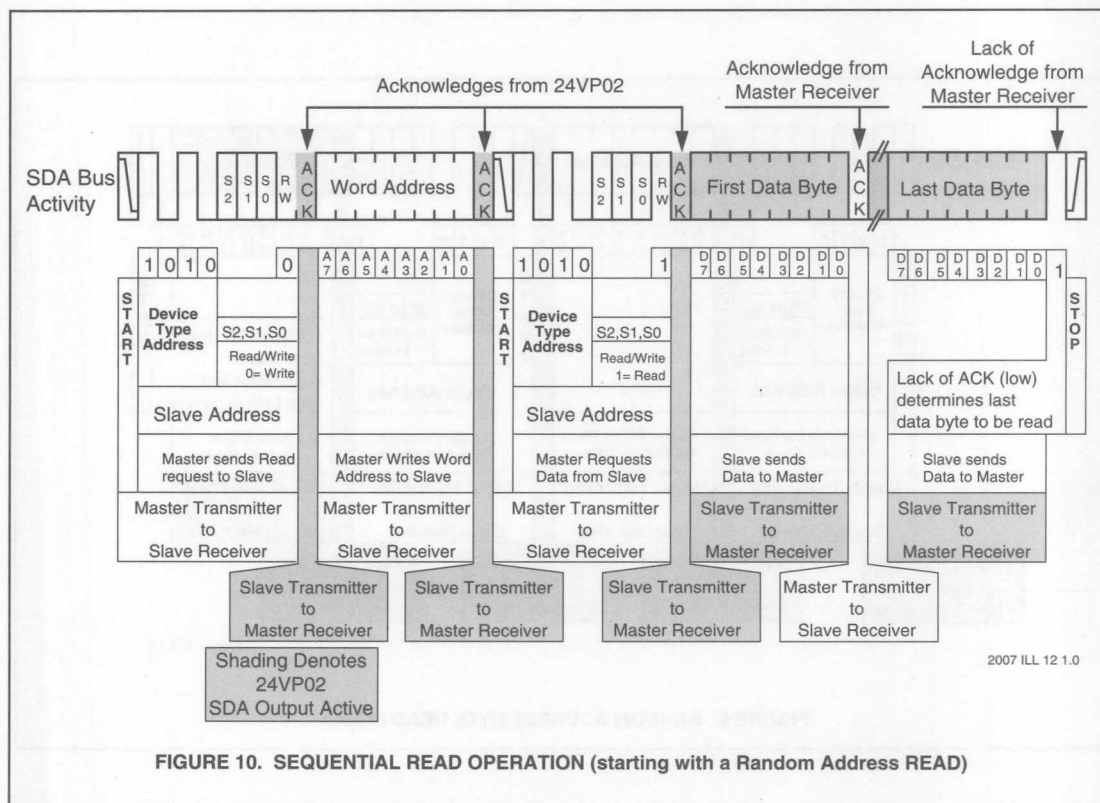
After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S24VP02 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S24VP02 discontinues data transmission and reverts to its standby power mode. See Figure 9 for the address, acknowledge and data transfer sequence.





Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S24VP02. The S24VP02 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 10 for the address, acknowledge and data transfer sequence.



**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

S24VP02, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$

S24VP02-3, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7V$ to $5.5V$

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA	$0.7 \times V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$		0.4	V

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AC ELECTRICAL CHARACTERISTICS

S24VP02, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$

S24VP02-3, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7V$ to $5.5V$

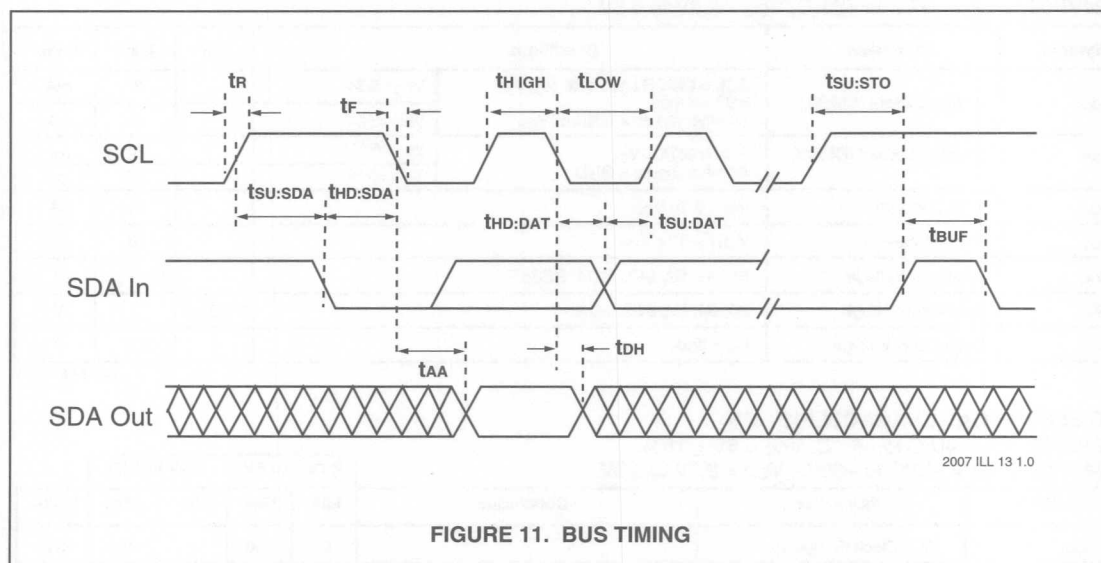
Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

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**CAPACITANCE** $T_A = 25^{\circ}\text{C}$, $f = 100\text{KHz}$

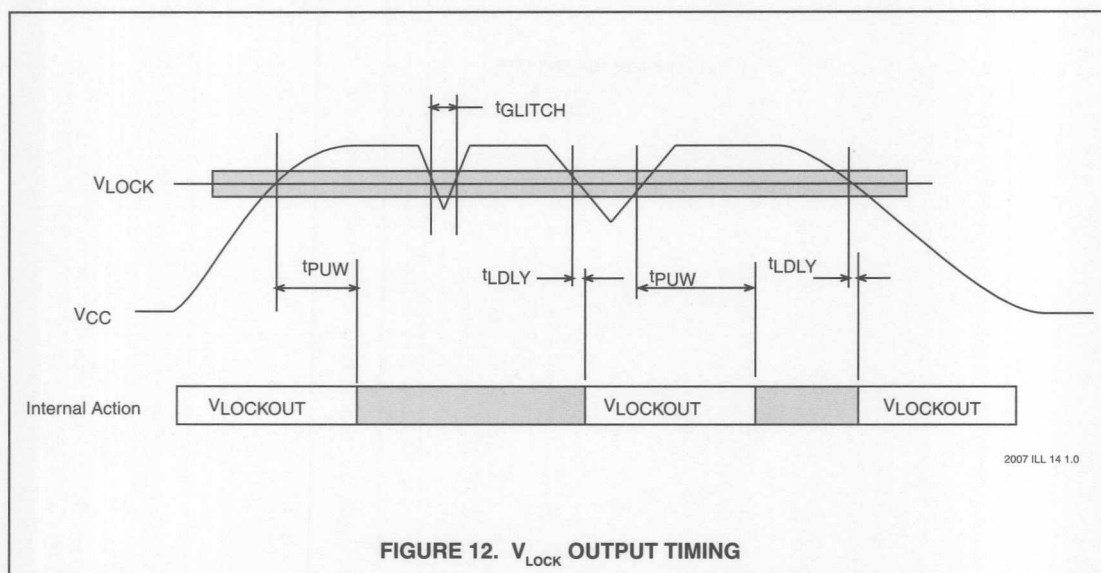
Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

2007 PGM T3 1.0

 **V_{LOCK} CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS** $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	S24VP02-2.7		S24VP02-A		S24VP02-B		Unit
		Min	Max	Min	Max	Min	Max	
V_{LOCK}	Write Lockout Voltage Level	2.55	2.70	4.25	4.50	4.50	4.75	V
t_{PUW}	Power-Up Write Delay	130	20	130	270	130	270	ms
t_{LDLY}	Delay to $V_{LOCKOUT}$		5		5		5	μs
t_{GLITCH}	Glitch Filter		30		30		30	ns

2007 PGM T4 1.3

**FIGURE 12. V_{LOCK} OUTPUT TIMING**



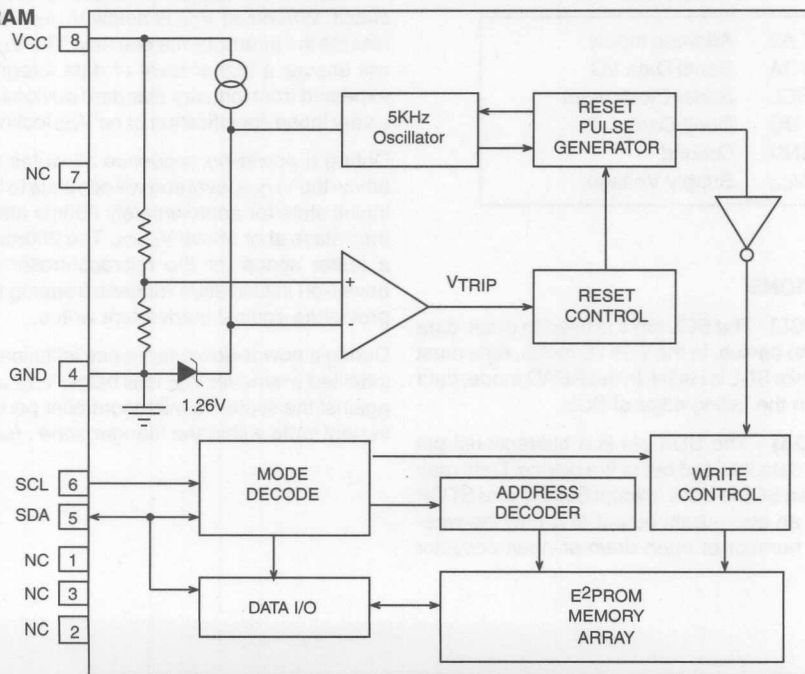
4K Serial E²PROM with a Precision Low-V_{CC} Lockout Circuit 3 and 5 Volt Systems
FEATURES

- Voltage Protection™
- Precision Low-V_{CC} Write Lockout
- All Write Operations Inhibited When V_{CC} Falls below V_{LOCK}
- One 3Volt and Two 5Volt System Versions
 - V_{LOCK} = 2.6V ± .1V / - .05V
 - V_{LOCK} = 4.25V ± .25V / - 0.0V
 - V_{LOCK} = 4.50 ± .25V / - 0.0V
- 100% Compatible with Industry Standard I²C™ Devices
 - Bi-directional data transfer protocol
 - Standard 100kHz and 400kHz Transfer Rates
- 16-Byte Page-Write Mode
 - Minimizes total write time per byte
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Commercial Industrial Temperature Range

OVERVIEW

The S24VP04 is a 4K-bit serial E²PROM memory integrated with a precision V_{CC} sense circuit. The sense circuit will disable write operations whenever V_{CC} falls below the V_{LOCK} voltage. It is fabricated using SUMMIT's advanced CMOS E²PROM technology and is suitable for both 3 and 5 volt systems.

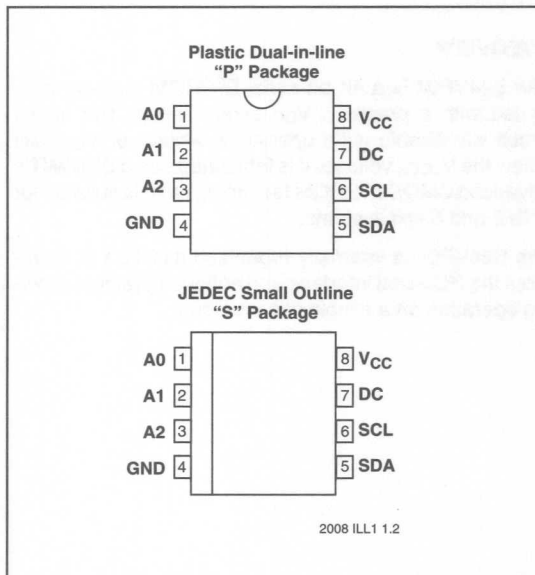
The S24VP04 is internally organized as 512 x 8. It features the I²C serial interface and software protocol allowing operation on a simple two-wire bus.

BLOCK DIAGRAM


2008 ILL2 1.2



PIN CONFIGURATIONS



PIN NAMES

A0, A1, A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
DC	Don't Care
GND	Ground
Vcc	Supply Voltage

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

Address Inputs A0, A1, A2- Device Address Inputs

These inputs are unused by the S24VP04; however, to ensure proper operation they should be left unconnected or tied to ground. They should not be tied high.

ENDURANCE AND DATA RETENTION

The S24VP04 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

DEVICE OPERATION

APPLICATIONS

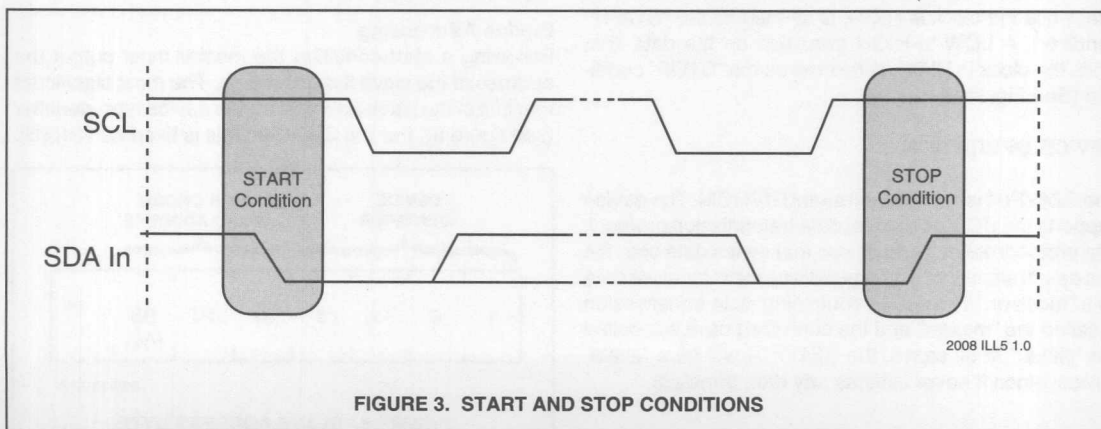
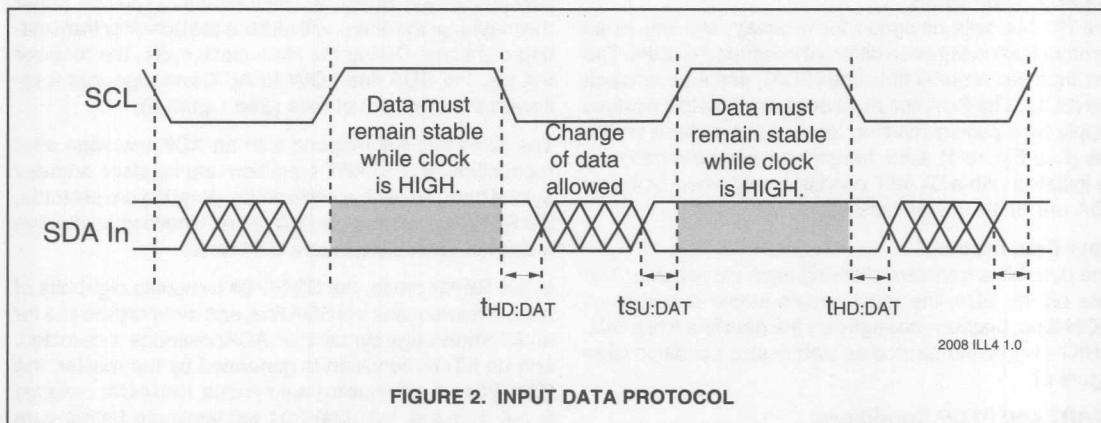
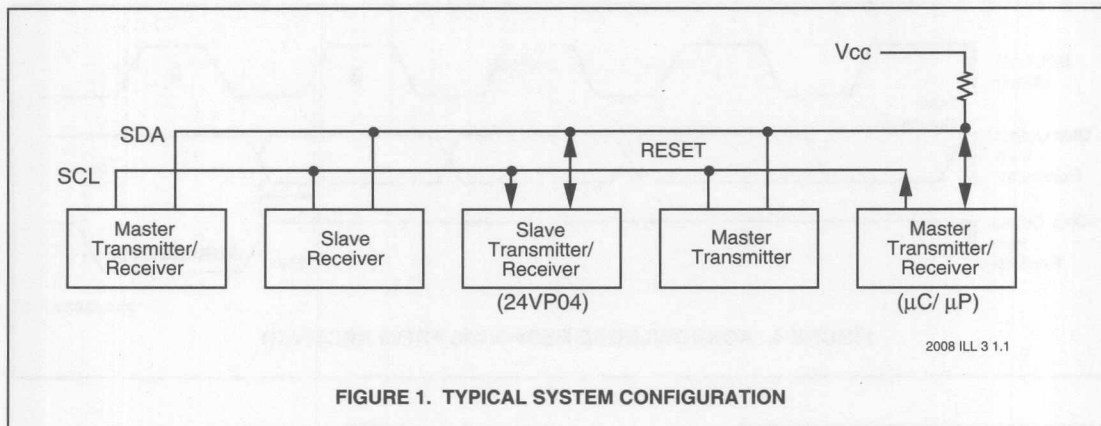
The S24VP04 was designed specifically for applications where the integrity of the stored data is paramount. In recent years, as the operating voltage range of serial E²PROMs has widened, most semiconductor manufacturers have arbitrarily eliminated their V_{CC} sense circuits. The S24VP04 will protect your data by guaranteeing write lockout below the selected V_{CC} Lockout voltage.

V_{CC} Lockout

The S24VP04 has an on-board precision V_{CC} sense circuit. Whenever V_{CC} is below V_{LOCK}, the S24VP04 will disable the internal write circuitry. The V_{CC} lockout circuit will ensure a higher level of data integrity than can be expected from industry standard devices that have either a very loose specification or no V_{CC} lockout specification.

During a power-on sequence all writes will be inhibited below the V_{LOCK} level and will continue to be held in a write inhibit state for approximately 200ms after V_{CC} reaches, then stays at or above V_{LOCK}. The 200ms delay provides a buffer space for the microcontroller to complete its power-on initialization routines (reading is OK) while still protecting against inadvertent writes.

During a power-down sequence initiation of writes will be inhibited whenever V_{CC} falls below V_{LOCK}. This will guard against the system's microcontroller performing an inadvertent write within the 'danger zone'. (see AN001)



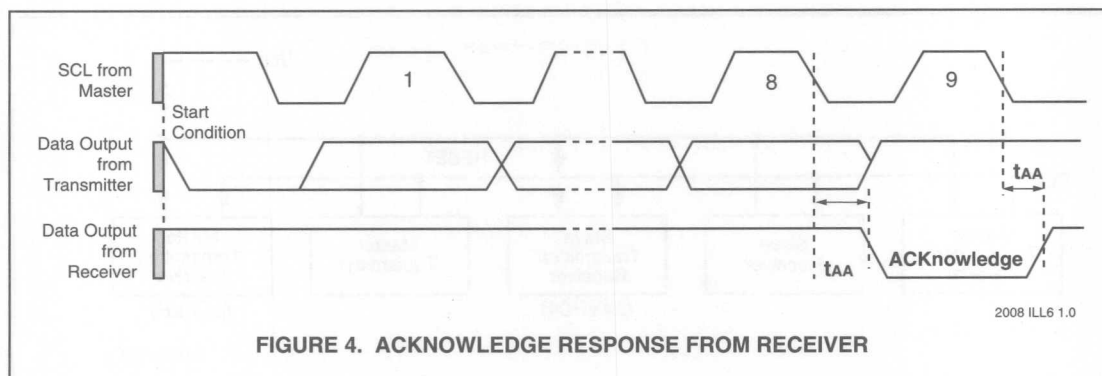


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition (See Figure 2).

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 3).

DEVICE OPERATION

The S24VP04 is a 16,384-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S24VP04 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 4).

The S24VP04 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S24VP04 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S24VP04 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S24VP04 will continue to transmit data. If an ACKnowledge is not detected, the S24VP04 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 5). For the S24VP04 this is fixed as 1010[B].

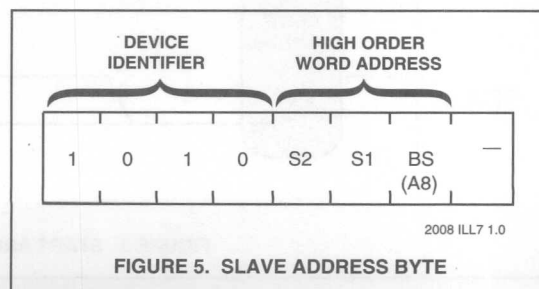


FIGURE 5. SLAVE ADDRESS BYTE



The next two bits are don't care. The S24VP04 will respond to all commands for device 1010.

Bank Select Bit

The next bit of the serial stream is the bank select bit. It is used by the host to toggle between the two 2K-bit banks of memory. It is, in effect, the most significant bit of the word address, or A8.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The S24VP04 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 512 words in the array.

Upon receipt of the word address, the S24VP04 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S24VP04 begins the internal write cycle.

While the internal write cycle is in progress, the S24VP04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S24VP04 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S24VP04 will respond with an ACKnowledge.

The S24VP04 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

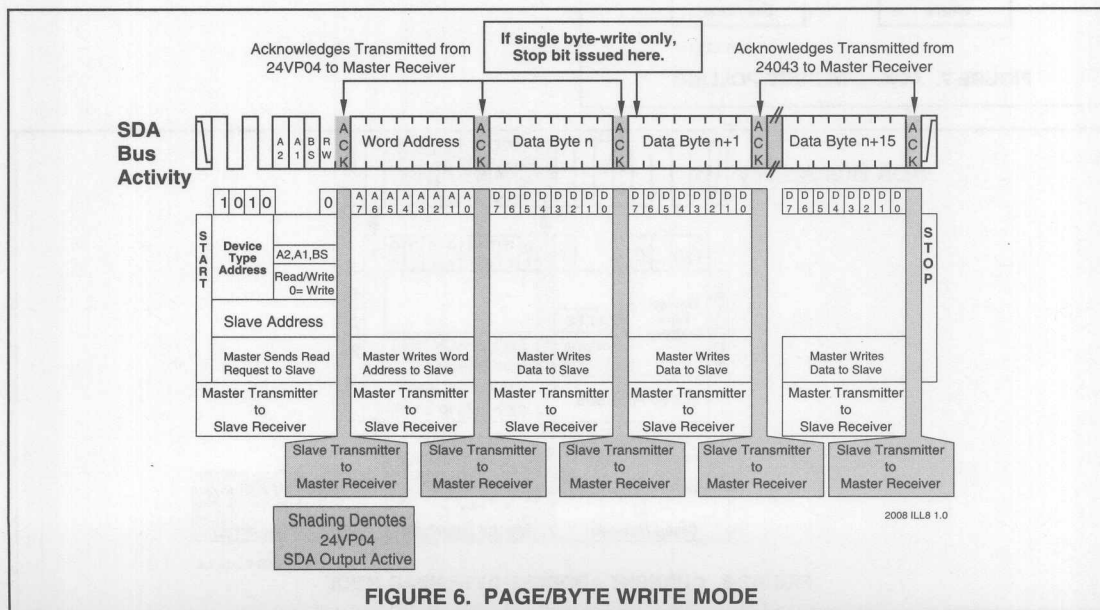


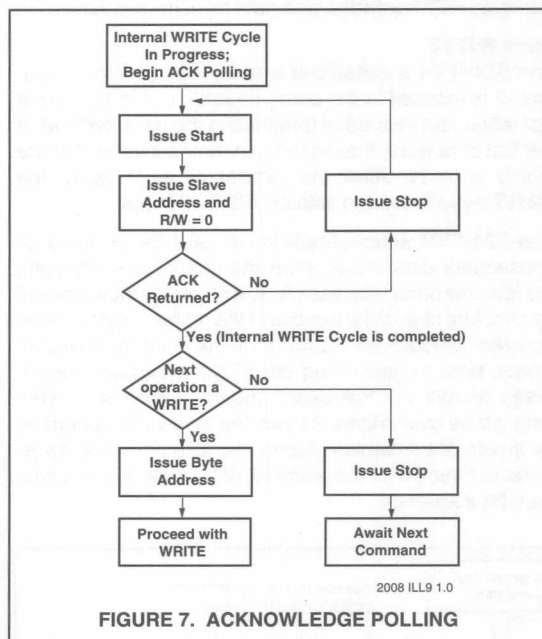
FIGURE 6. PAGE/BYTE WRITE MODE



Acknowledge Polling

When the S24VP04 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).



READ OPERATIONS

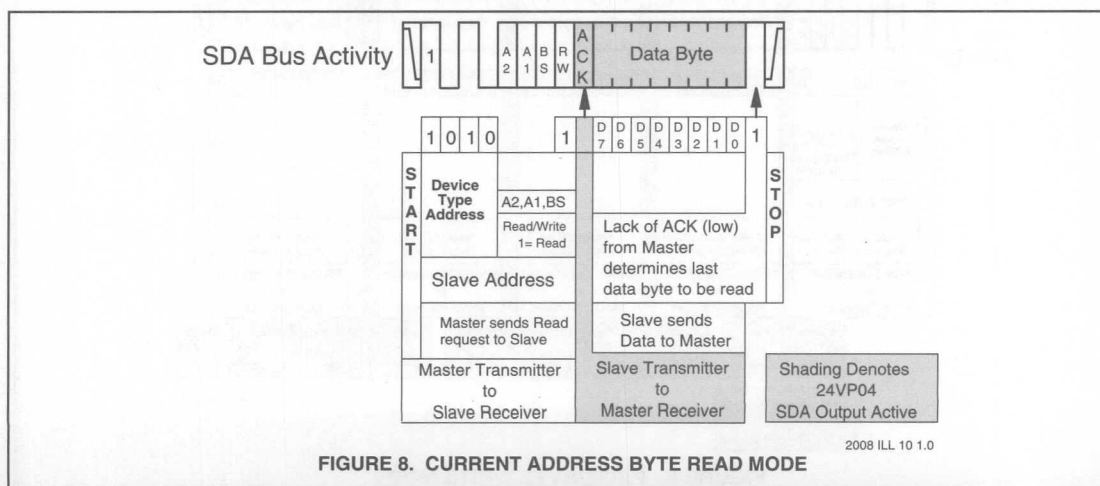
Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S24VP04 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n , the next read operation would access data from address location $n+1$ and increment the current address pointer. When the S24VP04 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location $n+1$.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S24VP04 discontinues data transmission. See Figure 8 for the address acknowledge and data transfer sequence.





Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S24VP04 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S24VP04 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S24VP04 discontinues data transmission and reverts to its standby power mode. See Figure 9 for the address, acknowledge and data transfer sequence.

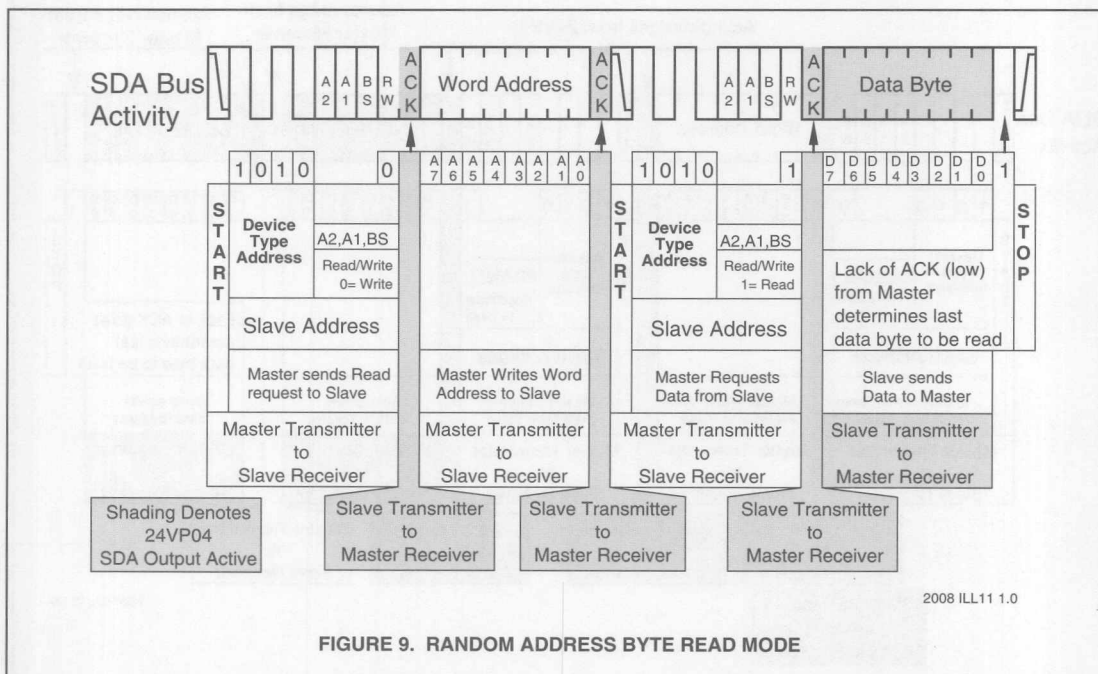


FIGURE 9. RANDOM ADDRESS BYTE READ MODE



Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S24VP04. The S24VP04 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 10 for the address, acknowledge and data transfer sequence.

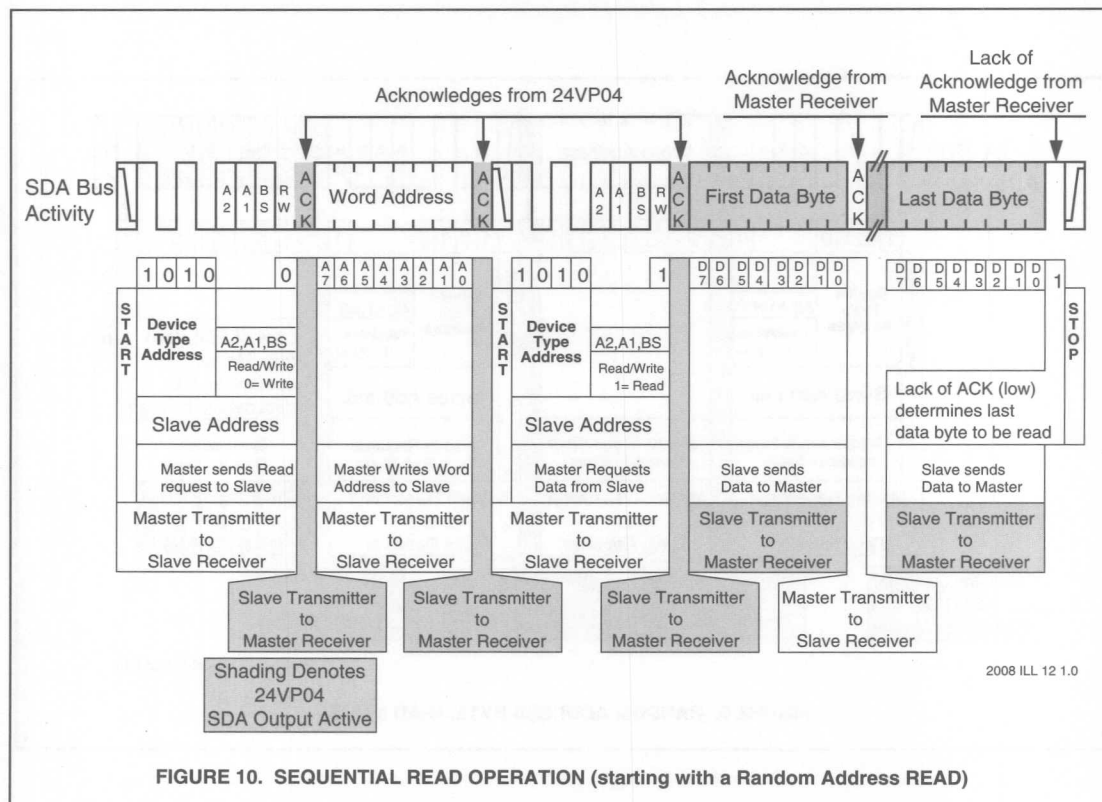


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

S24VP04, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$

S24VP04-3, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7V$ to $5.5V$

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA	$0.7 \times V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OL} = 3\text{mA}$		0.4	V

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AC ELECTRICAL CHARACTERISTICS

S24VP04, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$

S24VP04-3, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7V$ to $5.5V$

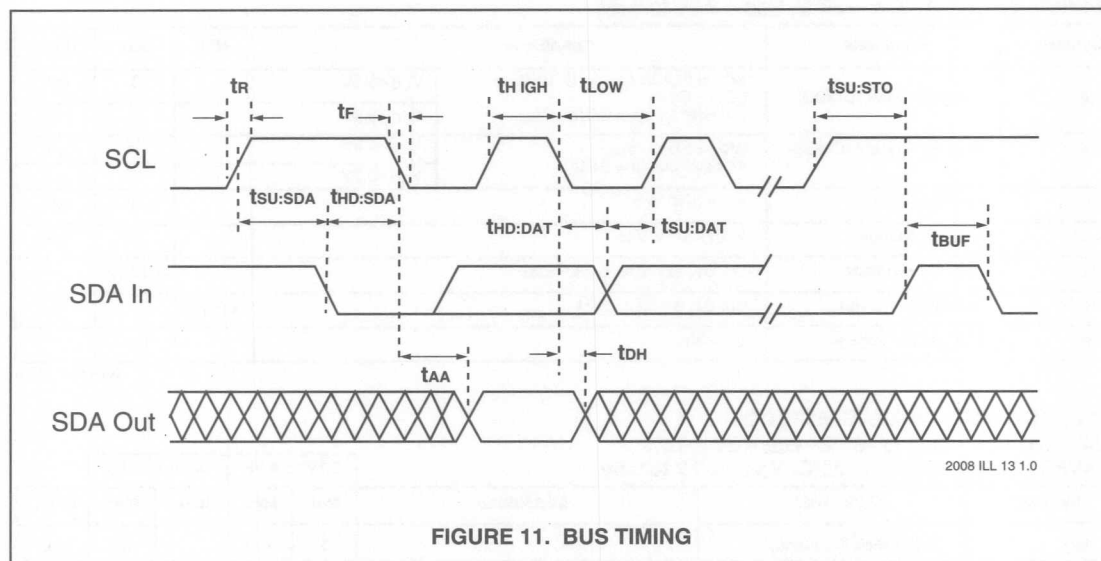
Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

2008 PGM T2 1.0

**CAPACITANCE** $T_A = 25^\circ\text{C}$, $f = 100\text{KHz}$

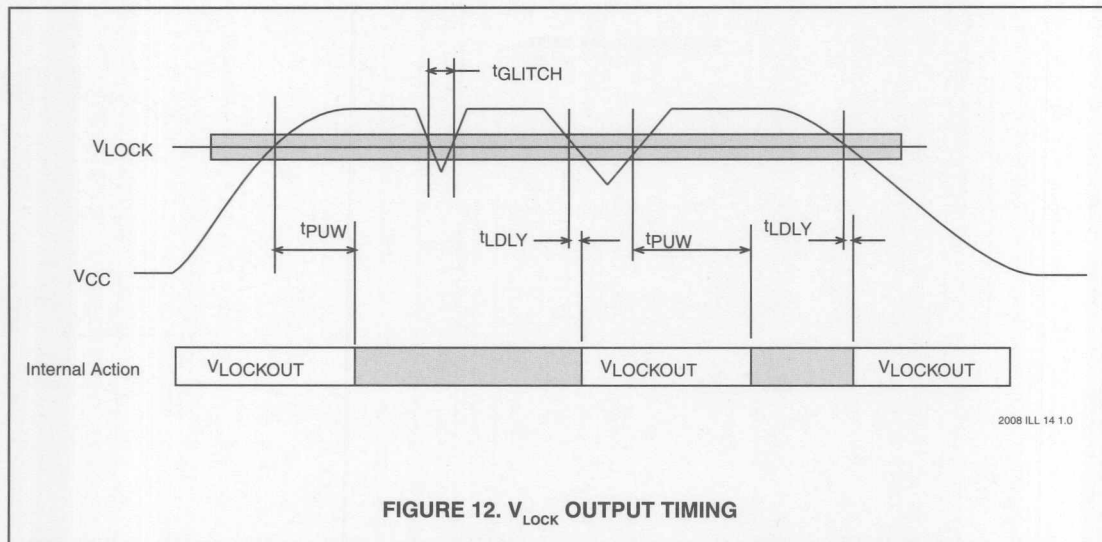
Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

2008 PGM T3 1.0

**FIGURE 11. BUS TIMING** **V_{LOCK} CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS** $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	S24VP04-2.7		S24VP04-A		S24VP04-B		Unit
		Min	Max	Min	Max	Min	Max	
V_{LOCK}	Write Lockout Voltage Level	2.55	2.70	4.25	4.50	4.50	4.75	V
t_{PUW}	Power-Up Write Delay	130	20	130	270	130	270	ms
t_{LDLY}	Delay to $V_{LOCKOUT}$		5		5		5	μs
t_{GLITCH}	Glitch Filter		30		30		30	ns

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16K Serial E²PROM with a Precision Low-V_{CC} Lockout Circuit 3 and 5 Volt Systems
FEATURES

- **Voltage Protection™**
- **Precision Low-V_{CC} Write Lockout**
- **All Write Operations Inhibited When V_{CC} Falls below V_{LOCK}**
- **One 3Volt and Two 5Volt System Versions**
 - V_{LOCK} = 2.6V ± .1V / -0.05V
 - V_{LOCK} = 4.25V ± .25V / -0.0V
 - V_{LOCK} = 4.50 ± .25V / -0.0V
- **100% Compatible with Industry Standard I²C™ Devices**
 - Bi-directional data transfer protocol
 - Standard 100kHz and 400kHz Transfer Rates
- **16-Byte Page-Write Mode**
 - Minimizes total write time per byte
- **1,000,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Commercial Industrial Temperature Range**

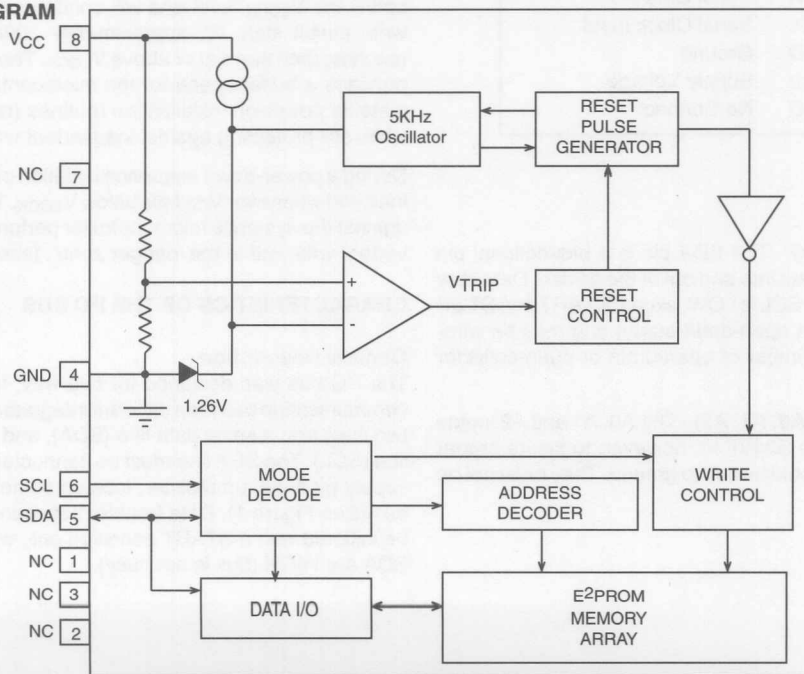
OVERVIEW

The S24VP16 is a 16K-bit serial E²PROM memory integrated with a precision V_{CC} sense circuit. The sense circuit will disable write operations whenever V_{CC} falls below the V_{LOCK} voltage. It is fabricated using SUMMIT's advanced CMOS E²PROM technology and is suitable for both 3 and 5 volt systems.

The S24VP16 is internally organized as 2,048 x 8. It features the I²C serial interface and software protocol allowing operation on a simple two-wire bus.

PIN DESCRIPTIONS

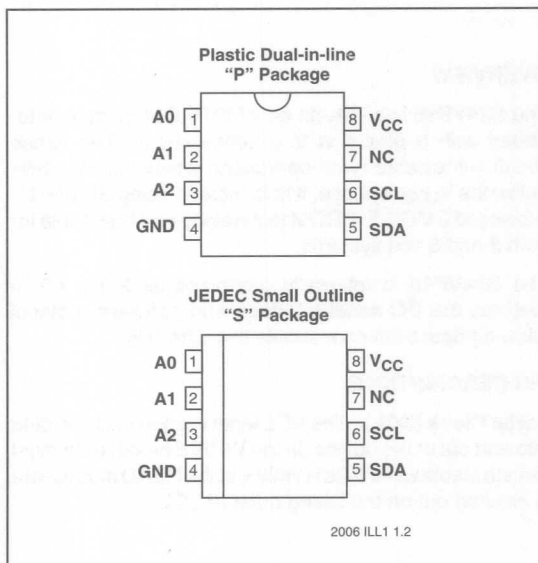
Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

BLOCK DIAGRAM


2006 ILL2 1.2



PIN CONFIGURATIONS



PIN NAMES

A0, A1, A2	Unused Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
GND	Ground
V _{CC}	Supply Voltage
NC	No Connect

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

Address Inputs (A0, A1, A2) - The A0, A1 and A2 inputs are unused by the S24VP16; however, to insure proper operation they should be tied to ground. They must not be tied to V_{CC}.

ENDURANCE AND DATA RETENTION

The S24VP16 is designed for applications requiring up to 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

DEVICE OPERATION

APPLICATIONS

The S24VP16 was designed specifically for applications where the integrity of the stored data is paramount. In recent years, as the operating voltage range of serial E²PROMs has widened, most semiconductor manufacturers have arbitrarily eliminated their V_{CC} sense circuits. The S24VP16 will protect your data by guaranteeing write lockout below the selected V_{CC} Lockout voltage.

V_{CC} Lockout

The S24VP16 has an on-board precision V_{CC} sense circuit. Whenever V_{CC} is below V_{LOCK}, the S24VP16 will disable the internal write circuitry. The V_{CC} lockout circuit will ensure a higher level of data integrity than can be expected from industry standard devices that have either a very loose specification or no V_{CC} lockout specification.

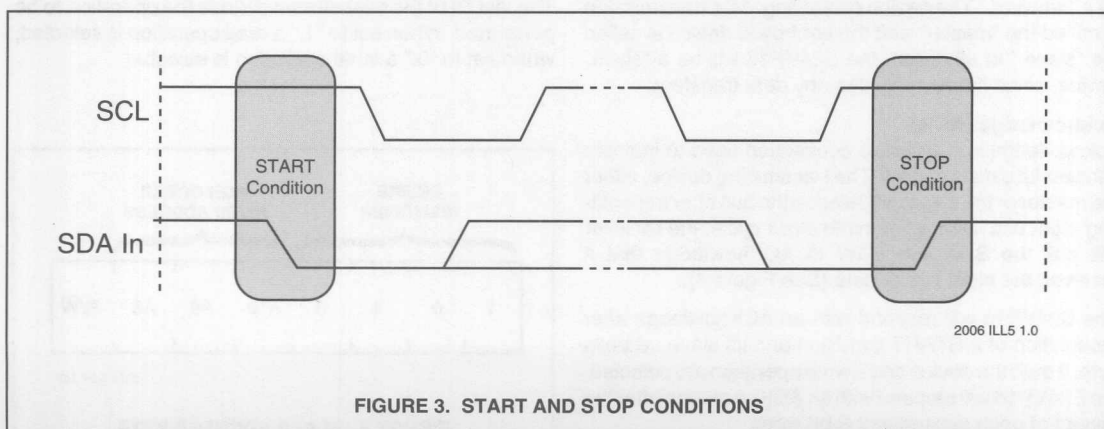
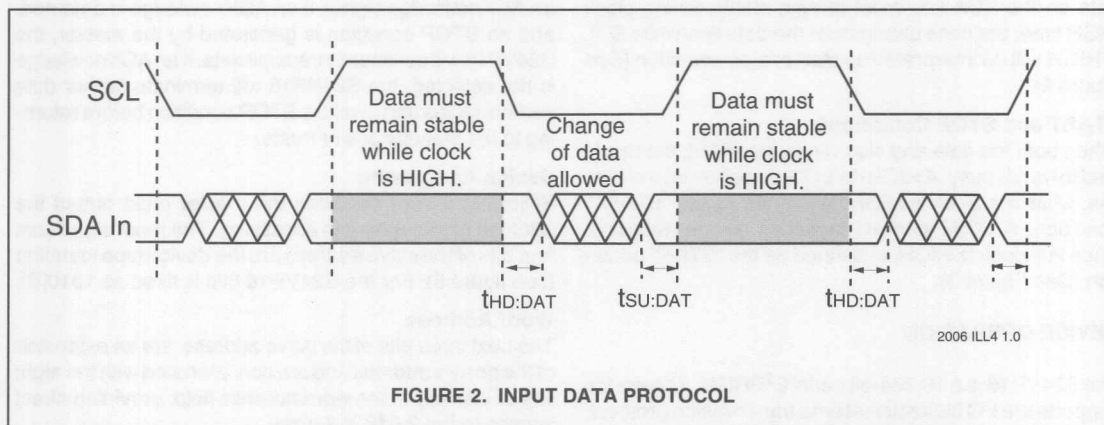
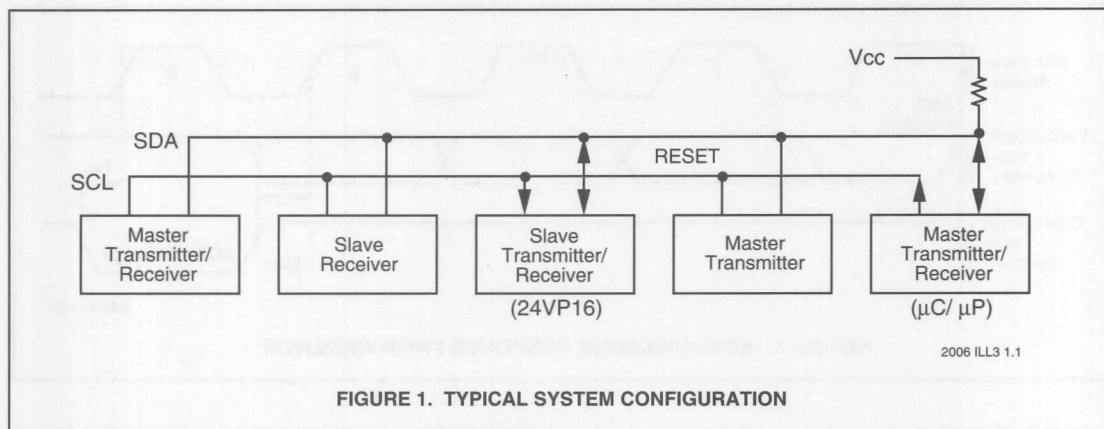
During a power-on sequence all writes will be inhibited below the V_{LOCK} level and will continue to be held in a write inhibit state for approximately 200ms after V_{CC} reaches, then stays at or above V_{LOCK}. The 200ms delay provides a buffer space for the microcontroller to complete its power-on initialization routines (reading is OK) while still protecting against inadvertent writes.

During a power-down sequence initiation of writes will be inhibited whenever V_{CC} falls below V_{LOCK}. This will guard against the system's microcontroller performing an inadvertent write within the 'danger zone'. (see AN001)

CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).



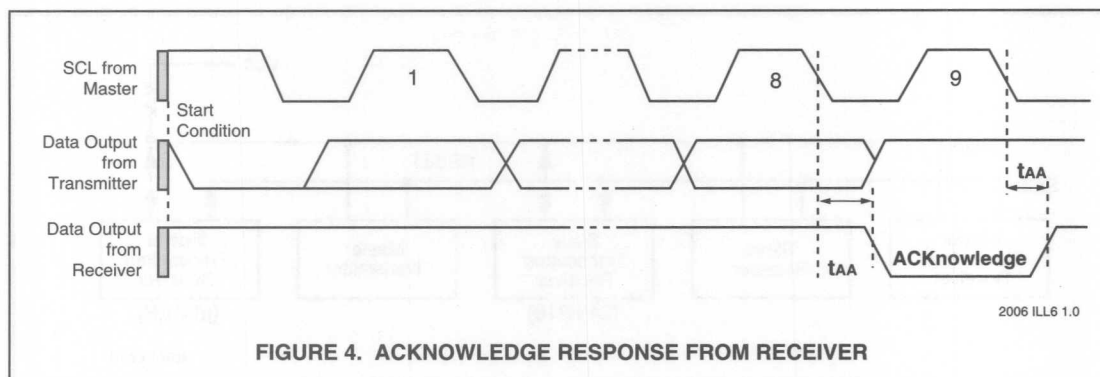


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition (See Figure 2).

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 3).

DEVICE OPERATION

The S24VP16 is a 16,384-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." In all cases, the S24VP16 will be a "slave" device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 4).

The S24VP16 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S24VP16 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S24VP16 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S24VP16 will continue to transmit data. If an ACKnowledge is not detected, the S24VP16 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 5). For the S24VP16 this is fixed as 1010[B].

Word Address

The next three bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the 2,048 X 8 array.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

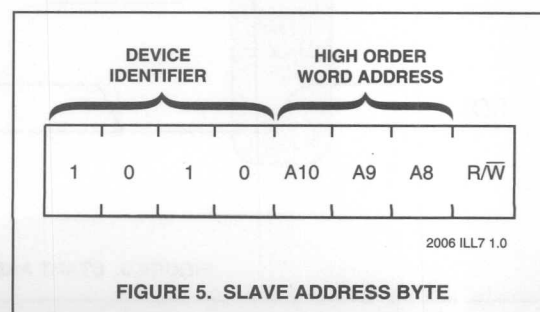


FIGURE 5. SLAVE ADDRESS BYTE



WRITE OPERATIONS

The S24VP16 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR} .

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 2,048 words in the array.

Upon receipt of the word address, the S24VP16 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S24VP16 begins the internal write cycle.

While the internal write cycle is in progress, the S24VP16 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S24VP16 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S24VP16 will respond with an ACKnowledge.

The S24VP16 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

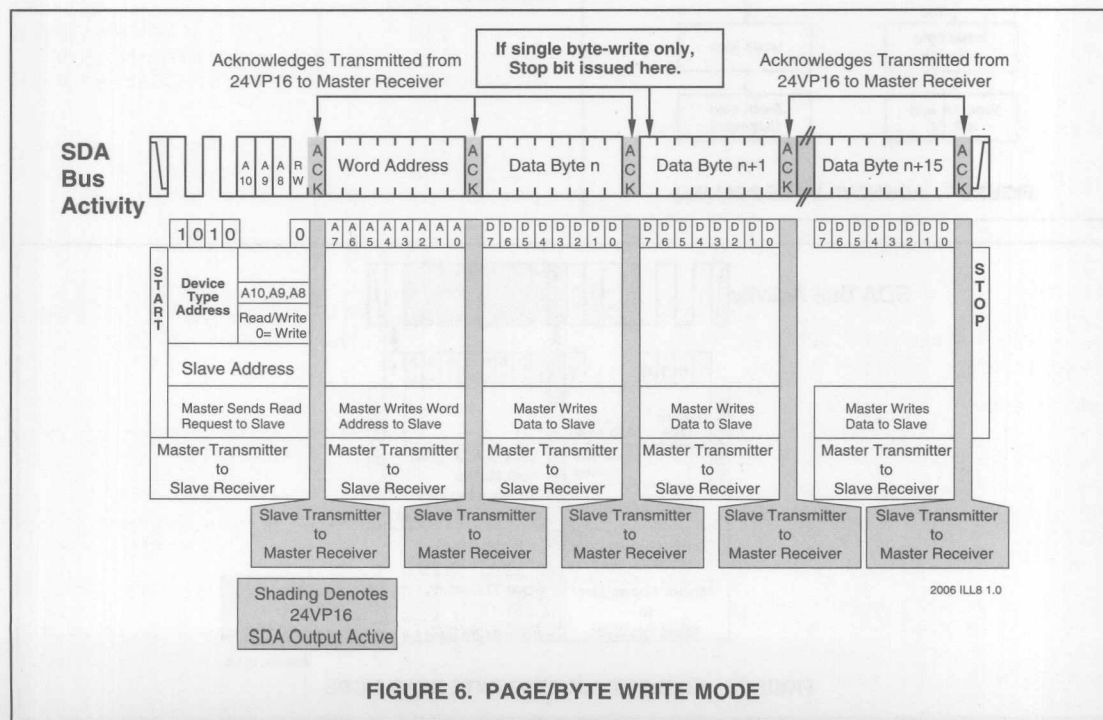


FIGURE 6. PAGE/BYTE WRITE MODE



To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).

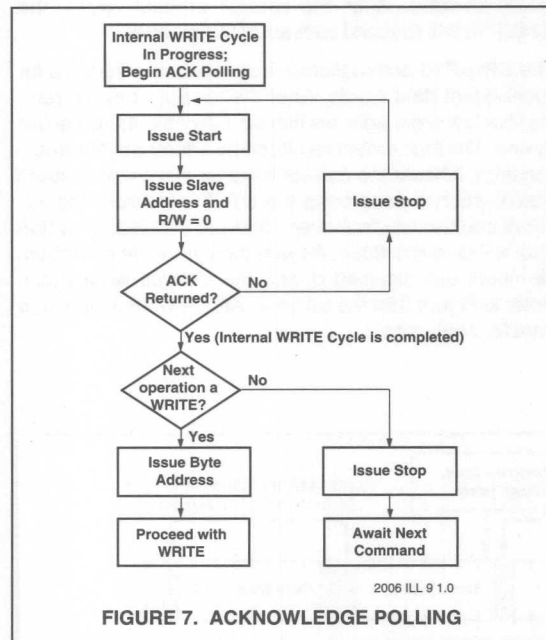


FIGURE 7. ACKNOWLEDGE POLLING

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S24VP16 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location *n*, the next read operation would access data from address location *n*+1 and increment the current address pointer. When the S24VP16 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location *n*+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S24VP16 discontinues data transmission. See Figure 8 for the address acknowledge and data transfer sequence.

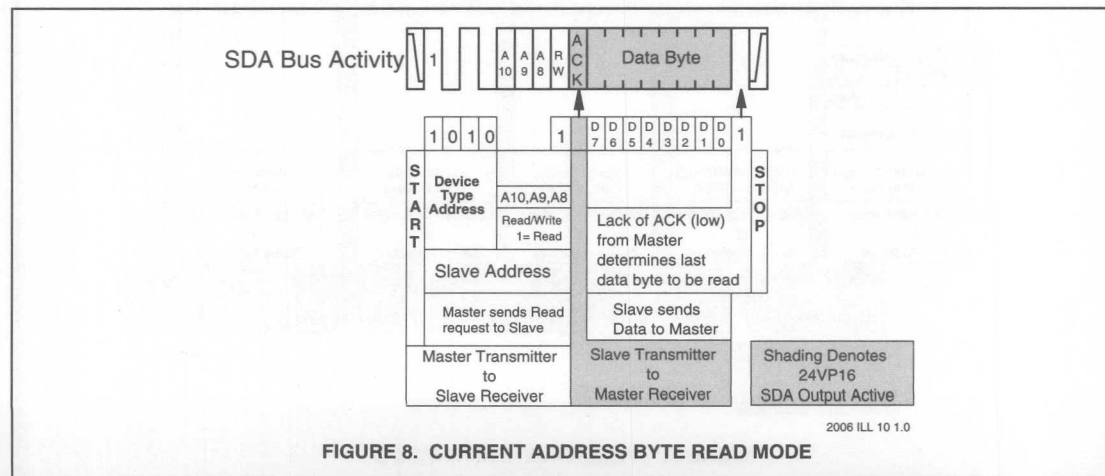


FIGURE 8. CURRENT ADDRESS BYTE READ MODE



Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S24VP16 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S24VP16 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S24VP16 discontinues data transmission and reverts to its standby power mode. See Figure 9 for the address, acknowledge and data transfer sequence.

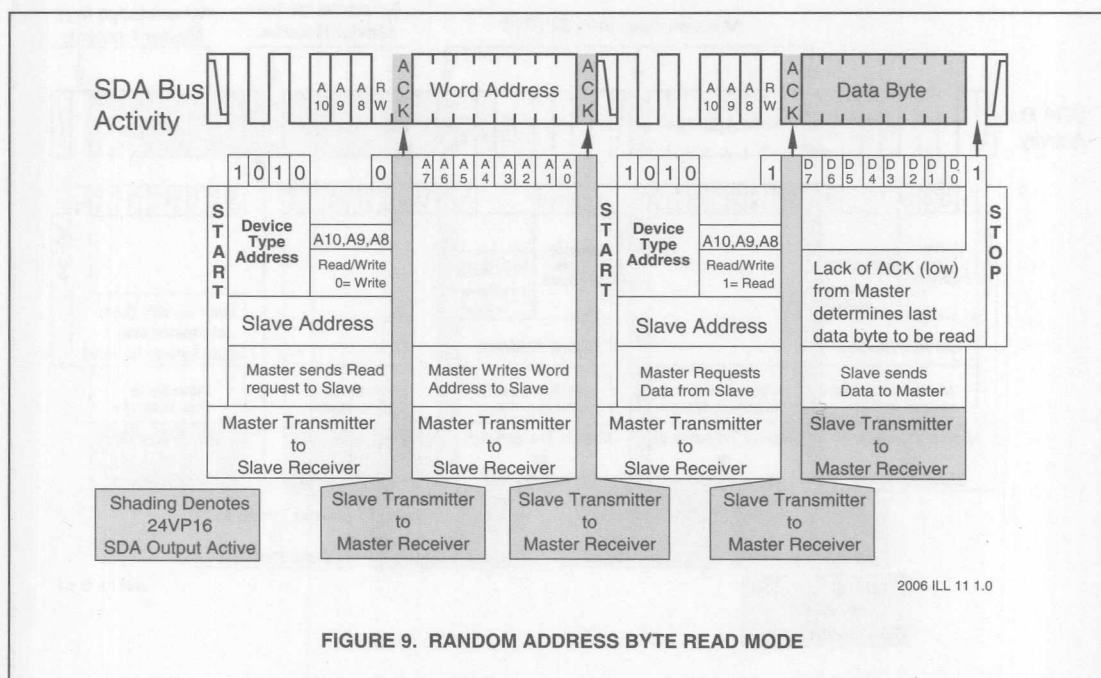


FIGURE 9. RANDOM ADDRESS BYTE READ MODE



Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S24VP16. The S24VP16 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 10 for the address, acknowledge and data transfer sequence.

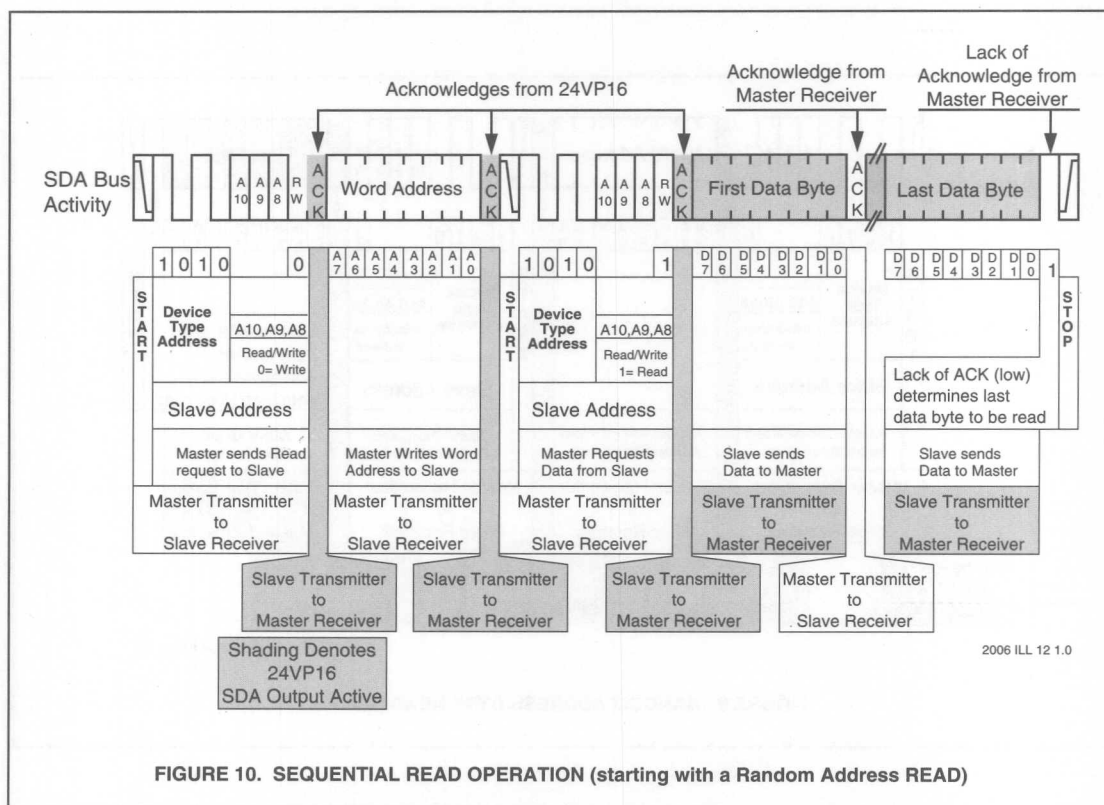


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Soldering Temperature (less than 10 seconds)	300°C
Supply Voltage	0 to 6.5V
Voltage on Any Pin	-0.3V to $V_{CC}+0.3V$
ESD Voltage (JEDEC method)	2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

S24VP16, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$

S24VP16-3, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7V$ to $5.5V$

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	$V_{CC}=5.5V$	3	mA
			$V_{CC}=3.3V$	2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	$V_{CC}=5.5V$	50	μA
			$V_{CC}=3.3V$	25	μA
I_{LI}	Input Leakage	$V_{IN} = 0$ To V_{CC}		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 0$ To V_{CC}		10	μA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET		$0.3 \times V_{CC}$	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA	$0.7 \times V_{CC}$		V
V_{OL}	Output Low Voltage	$I_{OL} = 3mA$		0.4	V

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AC ELECTRICAL CHARACTERISTICS

S24VP16, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5V \pm 10\%$

S24VP16-3, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7V$ to $5.5V$

Symbol	Parameter	Conditions	2.7V to 4.5V		4.5V to 5.5V		Units
			Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		μs
t_{HIGH}	Clock High Period		4.0		0.6		μs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		μs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		μs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		μs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		μs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	μs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		μs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

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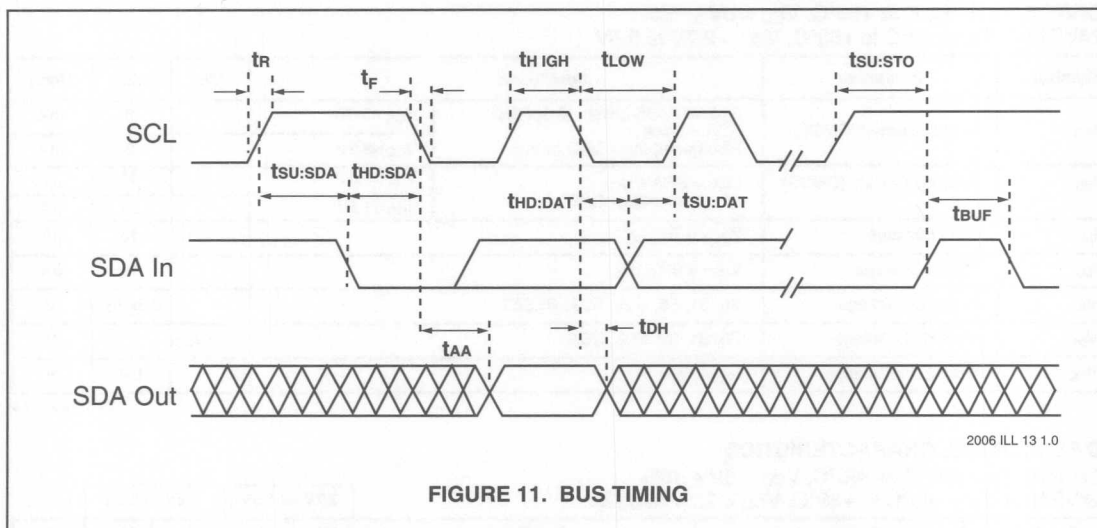


CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C _{IN}	Input Capacitance	5	pF
C _{OUT}	Output Capacitance	8	pF

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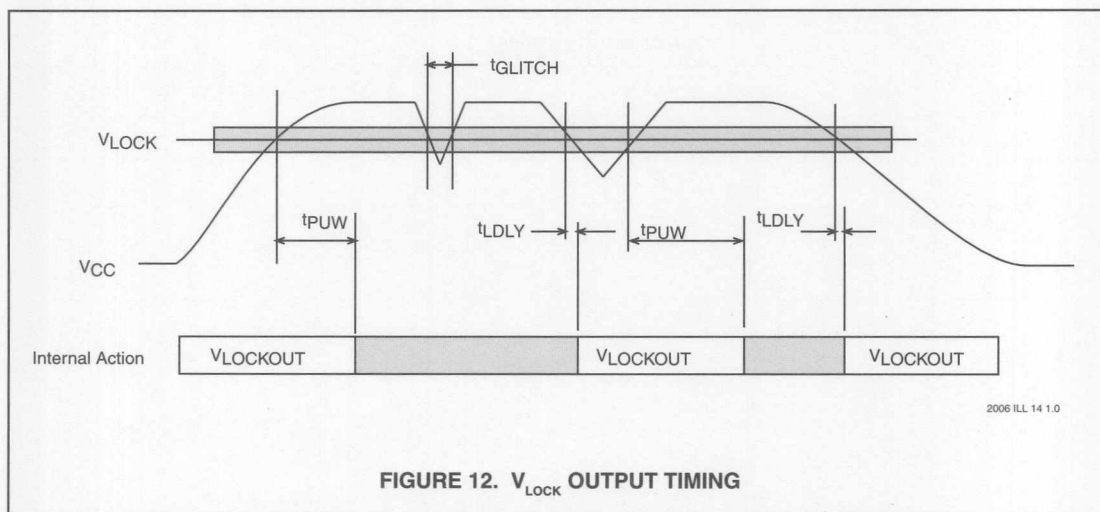


V_{LOCK} CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C

Symbol	Parameter	S24VP16-2.7		S24VP16-A		S24VP16-B		Unit
		Min	Max	Min	Max	Min	Max	
V _{LOCK}	Write Lockout Voltage Level	2.55	2.70	4.25	4.50	4.50	4.75	V
t _{PUW}	Power-Up Write Delay	130	20	130	270	130	270	ms
t _{LDLY}	Delay to V _{LOCKOUT}		5		5		5	μs
t _{GLITCH}	Glitch Filter		30		30		30	ns

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4K Serial E²PROM with a Precision Low-V_{CC} Lockout Circuit

FEATURES

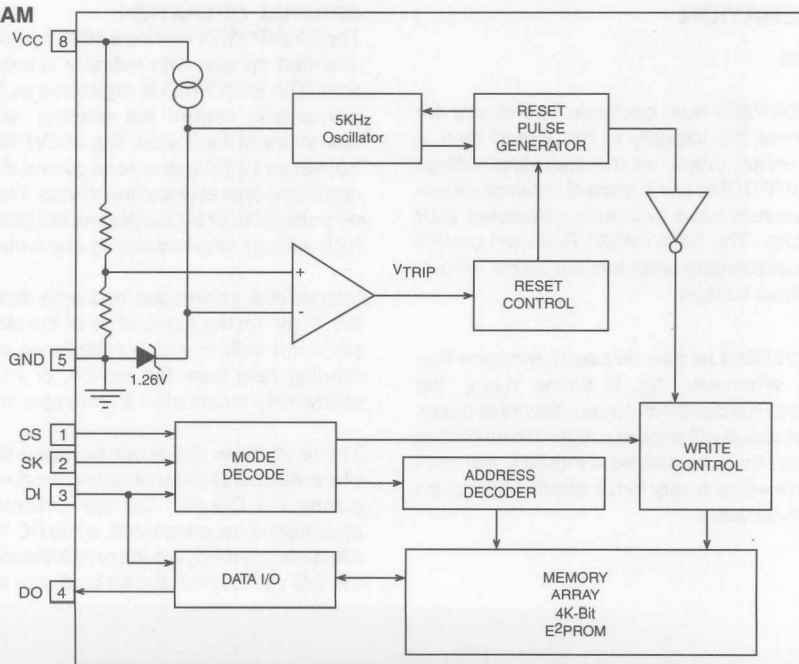
- Voltage Protection™
- Precision Low-V_{CC} Write Lockout
- All Write Operations Inhibited When V_{CC} Falls below V_{LOCK}
- One 3Volt and Two 5Volt System Versions
 - V_{LOCK} = 2.6V ± .1V / - .05V
 - V_{LOCK} = 4.25V ± .25V / - 0.0V
 - V_{LOCK} = 4.50 ± .25V / - 0.0V
- 100% Compatible with Industry Standard Microwire Devices
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Commercial Industrial Temperature Range

OVERVIEW

The S93VP662 and S93VP663 are 4K-bit serial E²PROM memories integrated with a precision V_{CC} sense circuit. The sense circuit will disable write operations whenever V_{CC} falls below the V_{LOCK} voltage. They are fabricated using SUMMIT's advanced CMOS E²PROM technology and is suitable for both 3 and 5 volt systems.

Both devices have 4k-bits of E²PROM memory that is accessible via the industry standard microwire bus. The S93VP662 is configured with an internal ORG pin tied low providing an 8-bit byte organization and the S93VP663 is configured with an internal ORG pin tied high providing a 16-bit word organization. Both the S93VP662 and S93VP663 have page write capability. The devices are designed for a minimum 1,000,000 program/erase cycles and have data retention in excess of 100 years.

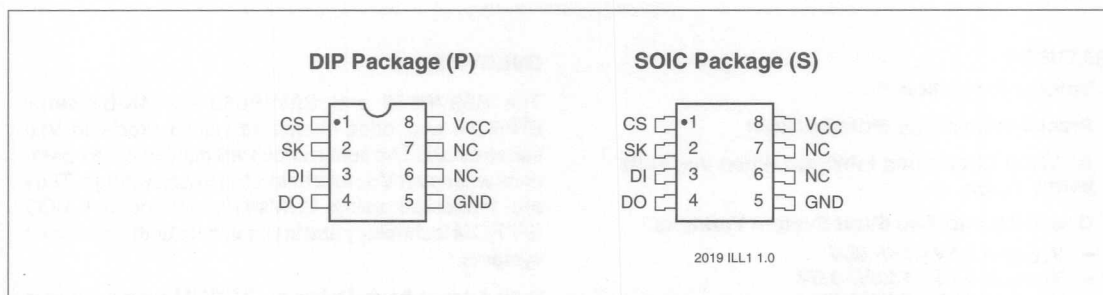
BLOCK DIAGRAM



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PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V _{CC}	+2.7 to 6.0V Power Supply
GND	Ground

During a power-on sequence all writes will be inhibited below the V_{LOCK} level and will continue to be held in a write inhibit state for approximately 200ms after V_{CC} reaches, then stays at or above V_{LOCK} . The 200ms delay provides a buffer space for the microcontroller to complete its power-on initialization routines (reading is OK) while still protecting against inadvertent writes.

During a power-down sequence initiation of writes will be inhibited whenever V_{CC} falls below V_{LOCK} . This will guard against the system's microcontroller performing an inadvertent write within the 'danger zone'. (see AN003)

DEVICE OPERATION

APPLICATIONS

The S93VP662/VP663 was designed specifically for applications where the integrity of the stored data is paramount. In recent years, as the operating voltage range of serial E²PROMs has widened, most semiconductor manufacturers have arbitrarily eliminated their V_{CC} sense circuits. The S93VP662/VP663 will protect your data by guaranteeing write lockout below the selected V_{CC} Lockout voltage.

V_{CC} Lockout

The S93VP662/VP663 has an on-board precision V_{CC} sense circuit. Whenever V_{CC} is below V_{LOCK} , the S93VP662/VP663 will disable the internal write circuitry. The V_{CC} lockout circuit will ensure a higher level of data integrity than can be expected from industry standard devices that have either a very loose specification or no V_{CC} lockout specification.

GENERAL OPERATION

The S93VP662/VP663 is a 4096-bit nonvolatile memory intended for use with industry standard microprocessors. The S93VP663 is organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. The S93VP662 is organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The device operates on a single 3V or 5V supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance



state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions is: one start bit; two op code bits and either eight (x16) or nine (x8) address/instruction bits.

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the S93VP662/VP663 will come out of the high impedance state and, will first output an initial dummy zero bit, then begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start automatic erase and write cycle to the memory location specified in the instruction. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the auto erase cycle of the selected memory location. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

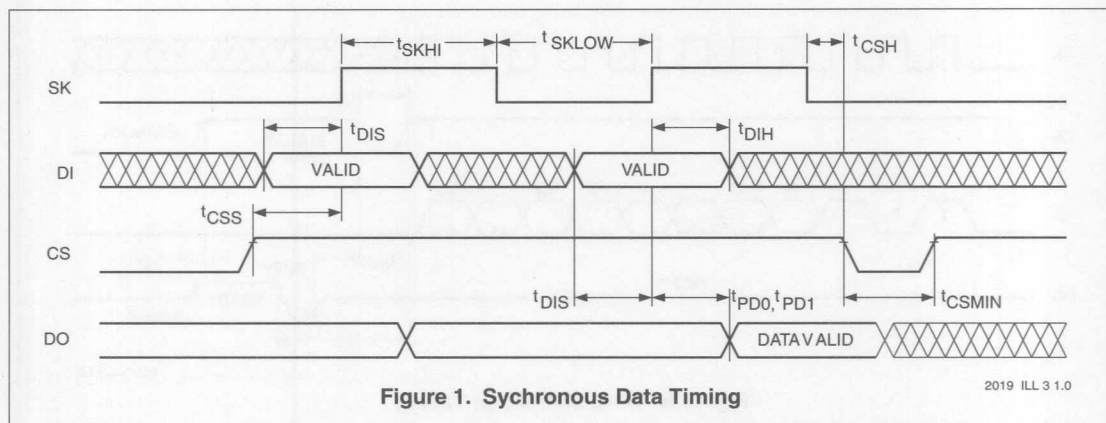


Figure 1. Synchronous Data Timing

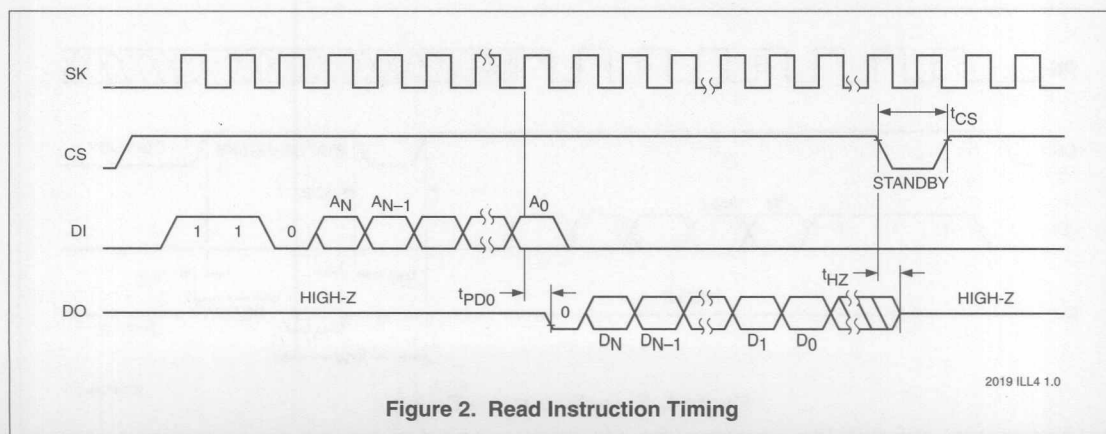


Figure 2. Read Instruction Timing



Erase/Write Enable and Disable

The S93VP662/VP663 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all S93VP662/VP663 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

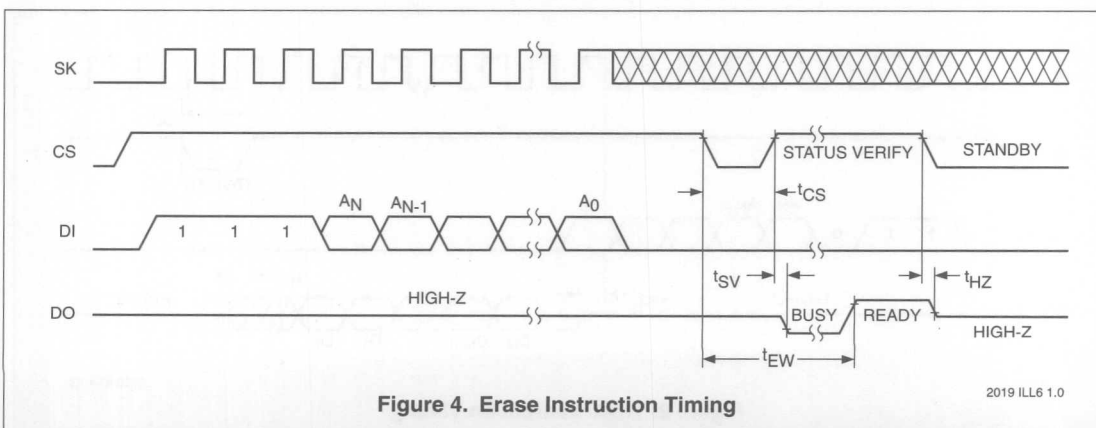
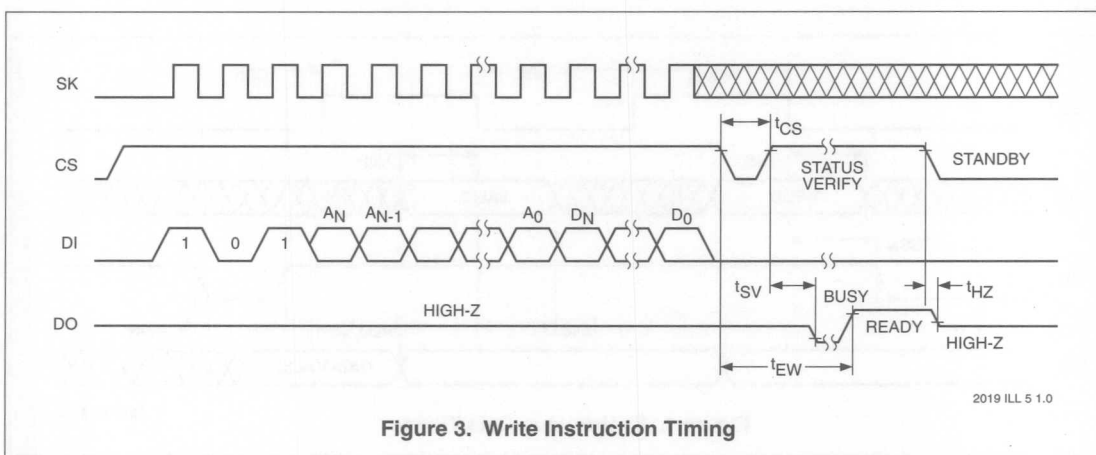
Erase All

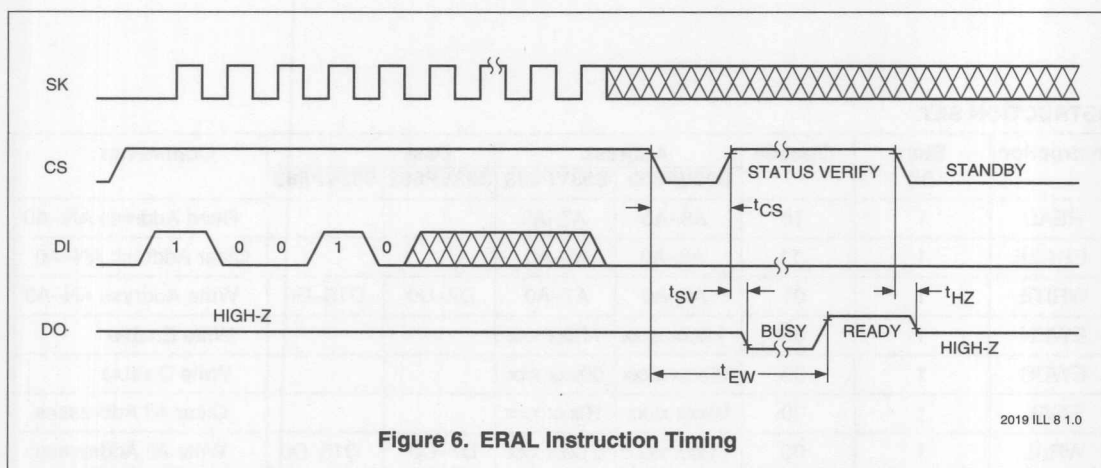
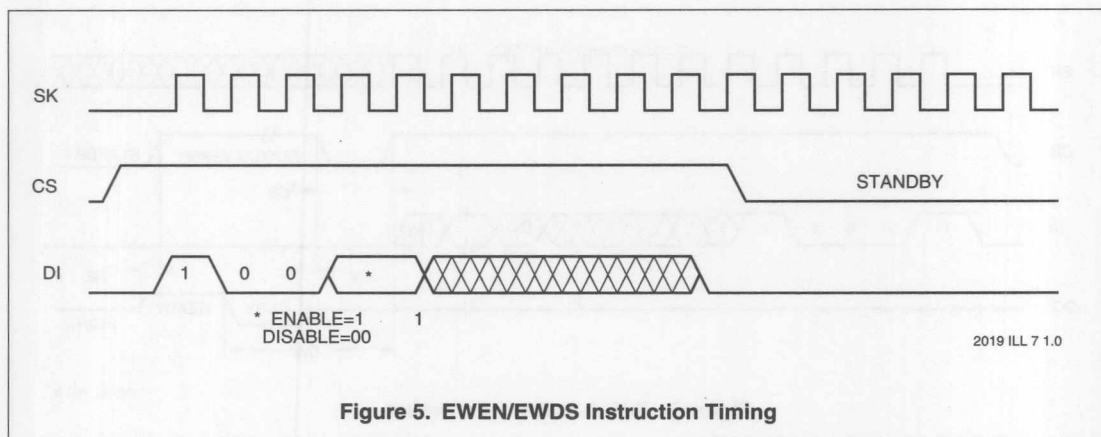
Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The

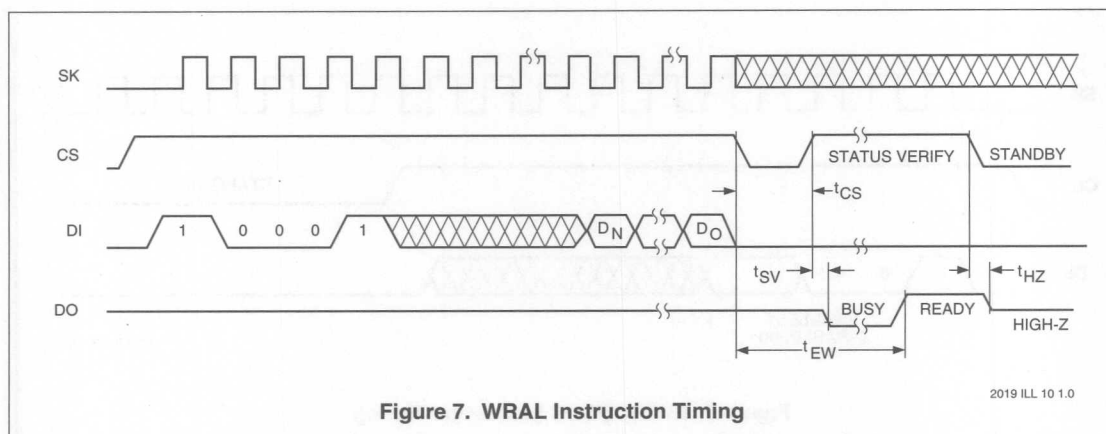
clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of 250ns (t_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the S93VP662/VP663 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.







INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			S93VP662	S93VP663	S93VP662	S93VP663	
READ	1	10	A8-A0	A7-A0			Read Address AN-A0
ERASE	1	11	A8-A0	A7-A0			Clear Address AN-A0
WRITE	1	01	A8-A0	A7-A0	D7-D0	D15-D0	Write Address AN-A0
EWEN	1	00	11xxx xxxx	11xxx xxx			Write Enable
EWDS	1	00	00xxx xxxx	00xxx xxx			Write Disable
ERAL	1	00	10xxx xxxx	10xxx xxx			Clear All Addresses
WRAL	1	00	11xxx xxxx	01xxx xxx	D7-D0	D15-D0	Write All Addresses

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**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with Respect to Ground ⁽¹⁾	-2.0V to +V _{CC} +2.0V
V _{CC} with Respect to Ground	-2.0V to +7.0V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽²⁾	100 mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
NEND ⁽³⁾	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
TDR ⁽³⁾	Data Retention	100		Years	MIL-STD-883, Test Method 1008
VZAP ⁽³⁾	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
ILTH ⁽³⁾⁽⁴⁾	Latch-Up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

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V_{CC} = +2.7V to +6.0V, unless otherwise specified. T_A = -40°C to +85°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I _{CC}	Power Supply Current (Operating)			3	mA	DI = 0.0V, f _{SK} = 1MHz V _{CC} = 5.0V, CS = 5.0V, Output Open
I _{SB}	Power Supply Current (Standby)			50	μA	CS = 0V
I _{LI}	Input Leakage Current			2	μA	V _{IN} = 0V to V _{CC}
I _{LO}	Output Leakage Current (Including ORG pin)			10	μA	V _{OUT} = 0V to V _{CC} , CS = 0V
V _{IL1} V _{IH1}	Input Low Voltage Input High Voltage	-0.1 2		0.8 V _{CC} +1	V V	4.5V ≤ V _{CC} ≤ 5.5V
V _{IL2} V _{IH2}	Input Low Voltage Input High Voltage	0 V _{CC} X0.7		V _{CC} X0.2 V _{CC} +1	V V	1.8V ≤ V _{CC} < 2.7V
V _{OL1} V _{OH1}	Output Low Voltage Output High Voltage	2.4		0.4	V V	4.5V ≤ V _{CC} ≤ 5.5V I _{OL} = 2.1mA I _{OH} = -400μA
V _{OL2} V _{OH2}	Output Low Voltage Output High Voltage	V _{CC} -0.2		0.2	V V	1.8V ≤ V _{CC} < 2.7V I _{OL} = 1mA I _{OH} = -100μA

Note:

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- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V_{CC} +1V.



S93VP662/S93VP663

PIN CAPACITANCE

Symbol	Test	Max.	Units	Conditions
C _{OUT} ⁽¹⁾	OUTPUT CAPACITANCE (DO)	5	pF	V _{OUT} =OV
C _{IN} ⁽¹⁾	INPUT CAPACITANCE (CS, SK, DI, ORG)	5	pF	V _{IN} =OV

Note:

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(1) This parameter is tested initially and after a design or process change that affects the parameter.

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	Limits				UNITS	Test Conditions
		V _{CC} =2.7V-4.5V		V _{CC} =4.5V-5.5V			
		Min.	Max.	Min.	Max.		
t _{CSS}	CS Setup Time	100		50		ns	C _L = 100pF
t _{CSH}	CS Hold Time	0		0		ns	
t _{DIS}	DI Setup Time	200		100		ns	
t _{DIH}	DI Hold Time	200		100		ns	
t _{PD1}	Output Delay to 1		0.5		0.25	μs	
t _{PD0}	Output Delay to 0		0.5		0.25	μs	
t _{HZ} ⁽¹⁾	Output Delay to High-Z		200		100	ns	
t _{EW}	Program/Erase Pulse Width		10		10	ms	
t _{CSSMIN}	Minimum CS Low Time	0.5		0.25		μs	
t _{SKHI}	Minimum SK High Time	0.5		0.25		μs	
t _{SKLOW}	Minimum SK Low Time	0.5		0.25		μs	
t _{SV}	Output Delay to Status Valid		0.5		0.25	μs	
SK _{MAX}	Maximum Clock Frequency	DC	500	DC	1000	KHZ	

Note:

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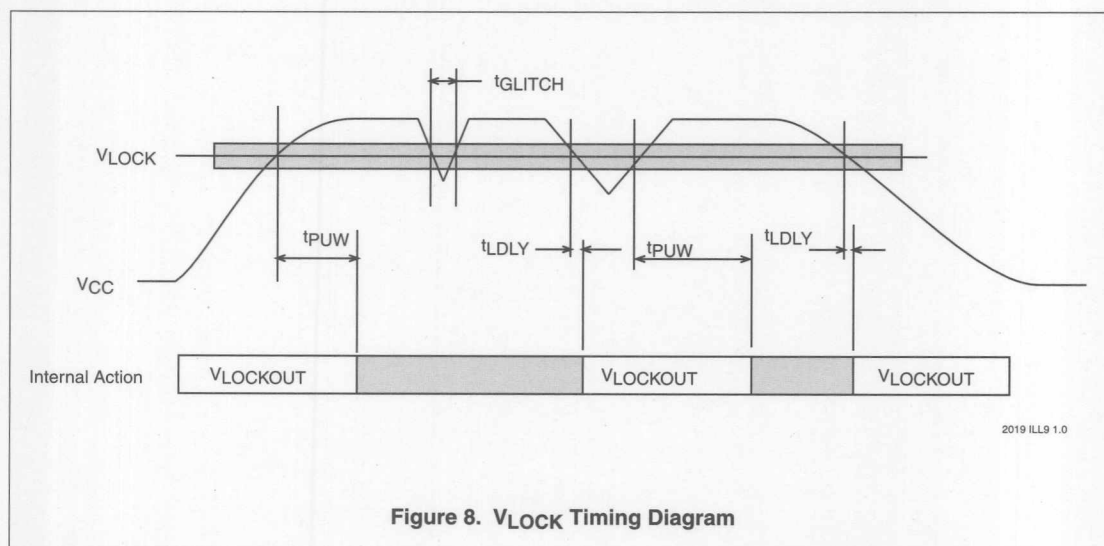
(1) This parameter is tested initially and after a design or process change that affects the parameter.



V_{LOCK} CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	S24VP662/VP663-2.7		S24VP662/VP663-A		S24VP662/VP663-B		Unit
		Min	Max	Min	Max	Min	Max	
V_{LOCK}	Write Lockout Voltage Level	2.55	2.70	4.25	4.50	4.50	4.75	V
t_{PUW}	Power-Up Write Delay	130	20	130	270	130	270	ms
t_{LDLY}	Delay to $V_{LOCKOUT}$		5		5		5	μs
t_{GLITCH}	Glitch Filter		30		30		30	ns

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SECTION 10 **Application Notes**

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Preventing Data Corruption in E²PROM Memory Applications

Abstract

E²PROMs are used in many embedded systems to store data essential to the proper operation of the system. Experience shows that many of these systems are subject to seemingly random low incidence data loss during the operation of the system which cannot be attributed to design or software bugs. The actual failure is corruption of the data by the inadvertent writing of improper data into the E²PROM during power transitions of the system. This situation has been worsened in recent years with the utilization of extended voltage range devices in 5 volt systems. That is, the E²PROMs are designed to write data at voltages much below the operating voltage of the microcontroller. Improved E²PROM sensing circuits and integrated RESET controllers finally provide a reliable solution to this applications problem.

Historical Aspect

The first 5-volt E²PROMs on the market in the early 80s were parallel devices. These devices included a crude V_{CC} sensor to disable write operations from being initiated in the device if V_{CC} fell below a certain voltage. Since these V_{CC} sensors were not specified at close tolerances many applications suffered from 'inadvertent write' data corruption. Software data protection was developed to solve this problem on the 64K densities and was so successful when used in conjunction with a RESET control circuit, it became an industry standard feature for parallel E²PROMs. In retrospect, a RESET input to the E²PROM memory might have been a better solution for many systems.

The emergence of serial E²PROMs, which make up the vast majority of new E²PROM applications, brought a false sense of security. Since a write operation required a definite sequence of data transfers of the serial interface it was assumed that this could not happen by accident in the event of a power cycle. The past 10 years have shown that this was indeed not the case since systems are still experiencing this data corruption problem.

From the beginning several schemes emerged including write enable instructions, write control inputs and the write disabling of certain portions of the memory to try to secure the most critical data in the system. Understanding the entire problem behind data corruption one can see how these features have improved but not solved this problem.

Most inadvertent write problems in today's systems are caused by the 'non-interaction' of the RESET generating circuitry and the E²PROM in the system. That is, if the RESET control circuitry is not valid for controlling the RESET input to the microcontroller during power-up, power-down and brownout situations, it is quite possible for the microcontroller to execute code in an unpredictable manner.

This situation is made worse if a serial E²PROM with a wide operating voltage range such as 1.8-5.5 volts is used in a system designed around 5 volts. If the RESET control circuitry is not designed to keep the microcontroller in RESET down to the 1.8 volt range problems can occur. Modern microcontrollers rely upon the RESET input to set up the voltage boundaries of operation since the manufacturers do not specify a minimum voltage where the microcontroller is guaranteed to stop functioning but rather a minimum voltage where the microcontroller is guaranteed to operate, Figure 1 shows a typical problem. The RESET control for the microcontroller generates a valid reset condition whenever V_{CC} is below 4.5 volts and is valid down to a V_{CC} of 3.0 volts. The serial E²PROM operates down to 1.8 volts which means that its internal V_{CC} sensor will disable write operations when V_{CC} is below 1.6 volts. This defines the area between 3.0V and 1.6V as the danger zone. If the microcontroller, in whatever state that it is in when V_{CC} is between 1.6V and 3.0V initiates a write operation, the E²PROM will execute the write operation, potentially overwriting valid data with invalid data.

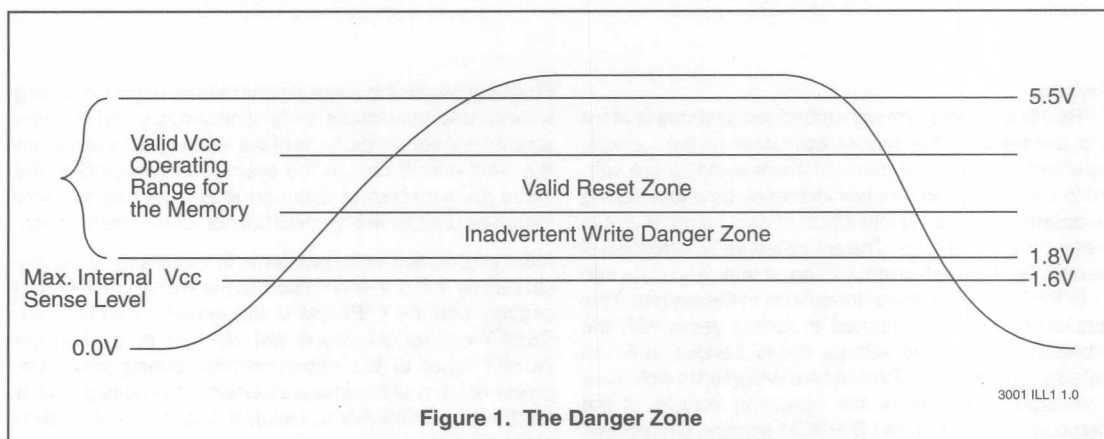


Figure 1. The Danger Zone

The level of the V_{CC} sense on the E²PROM is also important to insure proper operation. If the V_{CC} sense level of the E²PROM is set at a higher level than the RESET controller threshold the E²PROM will ignore valid write instructions and as a result the data will not be updated. This is especially problematic in instances of brown out where the V_{CC} level of the system falls below the V_{CC} sense level of the E²PROM but not far enough to trigger a RESET event.

Design Solutions

The first step is to insure that the V_{CC} sense level of the E²PROM to be used is compatible with the system design. In many cases the actual value of the V_{CC} sense is not stated in the data sheet nor is the stability over temperature specified.

The second step is to insure that the RESET controller provides a reliable RESET signal during all critical power conditions. In addition the logic level of the RESET output must be valid at any V_{CC} level above 1 volt.

Care must be taken to insure that the variances of both the V_{CC} sense on the E²PROM and the RESET are as small as possible since large variations on either will increase the size of the danger as well as interfere with the normal operation of the system.

Ideally the V_{CC} sense level used for the E²PROM write disable and the RESET generation should be the same. Many modern serial E²PROMs include a Write Control input to allow an external hardware write disable. If this signal is driven from the RESET circuitry the same V_{CC} level can be used, albeit with additional components.

A more practical solution to this problem is the integration of the RESET controller on the Serial E²PROM itself. The result is a precise and stable V_{CC} sensor which generates the E²PROM write disable as well as the system RESET signal at the same voltage.

The first examples of this type of device are the S24163, S24162 and S24VP16. All three are 16K-bit two wire serial memories and each has a precision reset controller on-board. The S24163 and S24162 have the reset signal bonded out to the RESET pin. The S24VP16 does not bond out the reset signal, but utilizes it internally to accurately disable the charge pump circuitry.

The RESET pin is both an input and an output allowing the devices to generate a proper RESET sequence either from the internal voltage sensor or an external signal such as a RESET button. The internal RESET timer insures that the RESET pulse width is a minimum of 200 msec regardless of the RESET condition.



Application Note 1

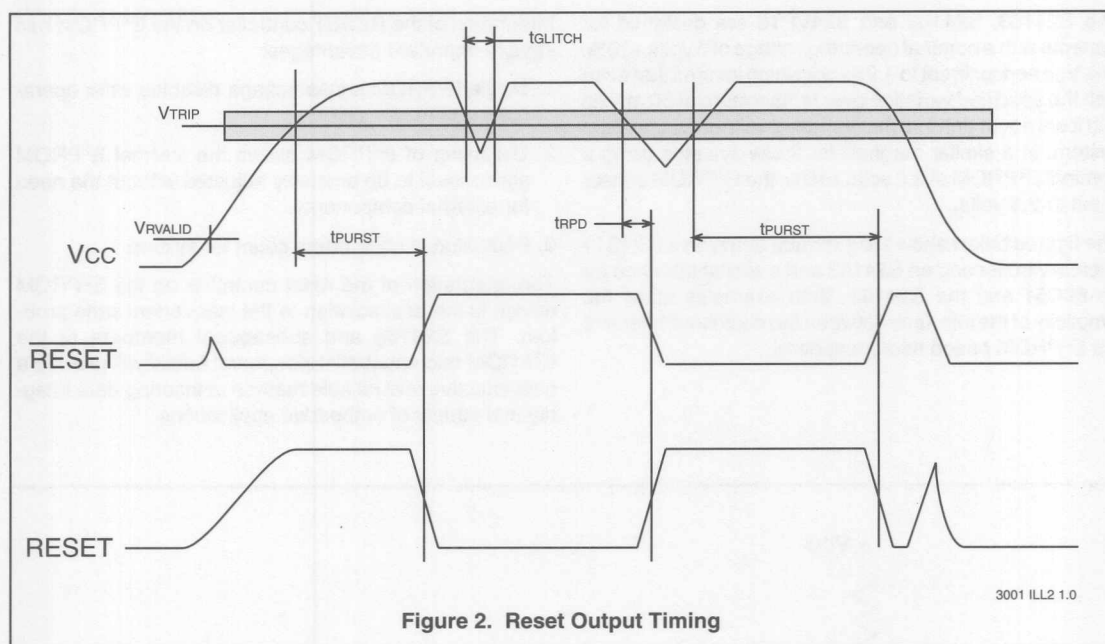


Table 1. Reset Output Characteristics

Symbol	Parameter	S24163-3		S24163		Units
		Min	Max	Min	Max	
VTRIP	Reset Trip Point	2.55	2.70	4.25	4.5	V
tPURST	Power-up Reset Timeout	130	270	130	270	ms
tRPD	VTRIP to RESET Output Delay		5		5	μ s
VRVALID	RESET Output Valid Voltage	1		1		V
tGLITCH	Glitch Reject Pulse Width		30		30	ns

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Application Note 1

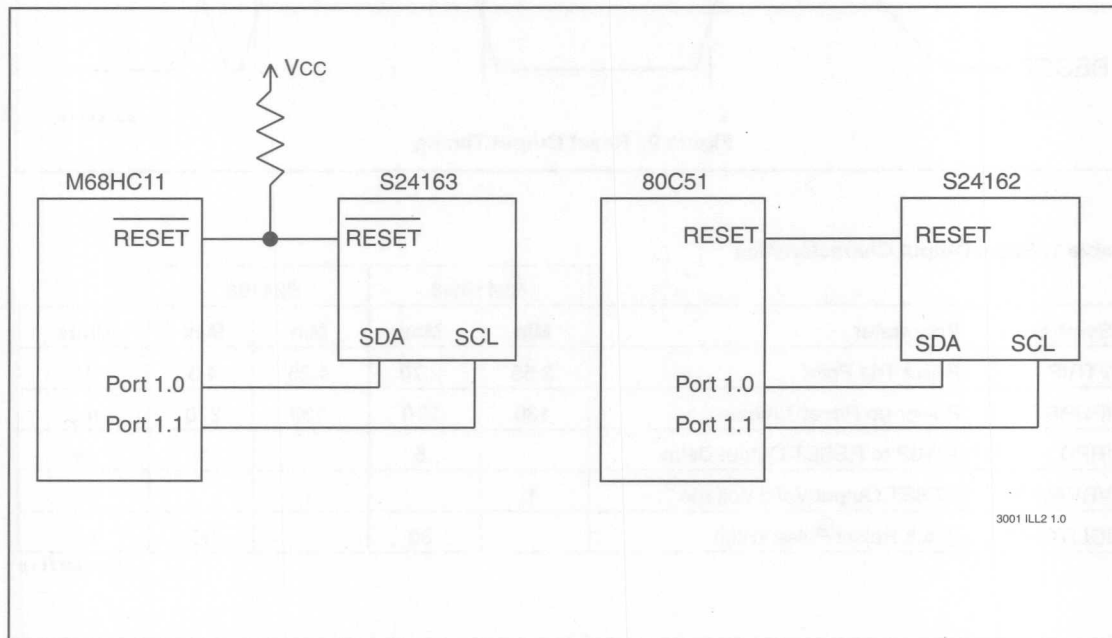
The S24163, S24162 and S24VP16 are designed for systems with a nominal operating voltage of 5 volts $\pm 10\%$. The V_{CC} sensor is set to 4.25 volts which insures that even with the specified variation over temperature of 50 mvolts that it will never drift into the operating voltage range of the system. In a similar manner, for those systems using a nominal E^2PROM of 3.0 volts $\pm 10\%$, the E^2PROM sensor is set to 2.6 volts.

The figures below show the interface between a 68HC11 microcontroller and an S24163 and a similar interface for an 80C51 and the S24162. Both examples show the simplicity of the interface between the microcontroller and the E^2PROM based microperipheral

Integration of the RESET controller on the E^2PROM has several important advantages:

1. Single E^2PROM sense voltage disables write operations and resets system.
2. Utilization of E^2PROM allows the internal E^2PROM sense level to be precisely adjusted without the need for external components.
3. Reduction in component count for system

The integration of the reset controller on the E^2PROM device is the best solution to the inadvertent write problem. The S24163 and subsequent members of the E^2PROM microcontroller peripheral family will provide a cost effective and reliable method of insuring data integrity in a variety of embedded applications.



Data Corruption in I²C Serial E²PROMs

Serial E²PROMs have given many designers a false sense of security with regards to inadvertently writing data to the device during power down and power up. Unlike parallel devices, serial devices needed a very particular sequence of data and clock transitions to complete a write cycle. In the case of the parallel devices, the only condition that needed to be met to initiate a write cycle was $CE = WE = L$ and $OE = H$. In other words, a simple voltage spike can cause an inadvertent write with a parallel E²PROM, but not on a serial device. However, serial E²PROMs are still susceptible to data corruption due to inadvertent writes. The three primary causes of inadvertent writes in I²C type Serial memories are categorized below; a symptom, root cause and solution for each is shown.

Symptom: Random data loss during read operations.

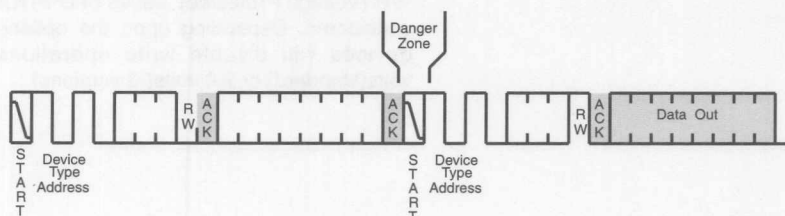
Root Cause: Loss of start condition during random read.

A random read operation to an I²C serial E²PROM consists of two parts. The first of these is the writing of the address to be read into the device (Start, Slave Address R/W {= LOW}, byte address). The second part is reading of the data (Start, Slave Address R/W {= High}, Data Out). In a noisy application the start condition in between these two parts may not be received by the serial E²PROM. If this occurs, a random read operation will be interpreted as a byte write operation and data is corrupted. This is most often seen as the mysterious emergence of the slave address stored in the location that was to be altered.

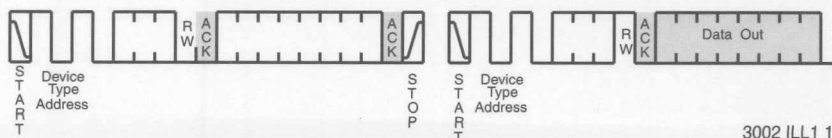
Solution: The random access read operation can easily be broken into two separate instructions. The first is a write instruction and address followed by a stop condition. No write will occur, but the internal address pointer will be updated. The second part is to reissue a start condition, followed by the read command, effectively performing a current address read operation.

If one always uses these two instructions rather than a single instruction, the two operations will be separated by proper acknowledge, stop and start conditions and the problem will be eliminated.

Industry Recommended Method For Random Read



Summit Recommended Method For Performing Random Read



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Symptom: Data is lost when power is turned off and on to the serial E²PROM when power strobing

Root Cause: Test Mode Activation

Power strobing is frequently used by designers of systems to reduce current consumption. It is most often implemented by turning off the VCC to the serial E²PROM through the use of a FET switch. Since the contents of the serial E²PROM are nonvolatile, the device only needs to be turned on to read information into static RAM in the MCU and then turned off during system operation.

Problems may arise in this application if the particular serial E²PROM which is to be used implements test modes by applying a high voltage to certain inputs on the device. With VCC turned off, some devices can interpret a logic level signal on one of the inputs as a "high voltage" and proceed to enter a test mode. Since test modes on serial E²PROMs normally include such things as block erase and block program, entering into these modes can be catastrophic.

Solution: Insure the manufacturer's E²PROMs that you use have no high voltage enabled test modes on inputs that will not be connected to ground when the device is turned off. It should be noted that each serial E²PROM manufacturer will implement different test modes in different manners. These test modes are seldom included on the manufacturer's data sheets.

Symptom: Serial E²PROM Loses data when power is turned off and it appears as if a data retention failure has occurred.

Root Cause: The microcontroller executed a write operation during power-up or power-down. This is by far the most common cause of inadvertent writes of data in the I²C serial E²PROMs. The code to write to the serial E²PROM resides in the program memory of the microcontroller. If the microcontroller gets into this section of code accidentally, the serial E²PROM will be written. In most cases, this occurs during power-down or a brown-out situation where the microcontroller is not held in a proper reset state. This situation combined with today's I²C E²PROMs ability to perform a write operation down to <1.8 volts can again lead to a catastrophic inadvertent write.

Solution: When a serial E²PROM of any kind is used in a microcontroller system, a reset control circuit must be used to hold the microcontroller in a valid reset condition during all power transitions: including power-up, power-down and brown-outs. Traditional R/C circuits are useless in protecting the data in the E²PROM from corruption. The Summit S24XX3 family of devices integrate a precision reset controller with the serial E²PROM in a single cost effective component.

If the system is already in production and adequate reset protection cannot be added, then the Summit "VP"(Voltage Protected) series of E²PROMs should be considered. Depending upon the options chosen the devices will disable write operations below 4.4 volts(standard) or 2.6 volts(-3 versions).

Microwire Memories and Brownouts: Another Danger Zone

When parallel E²PROM's were first introduced to the market, the number one customer issue was inadvertent write operations. These would occur during power-up and power-down operations. The system would be in an unknown state with the write control lines to the E²PROM moving and occasionally matching up to perform a write. The resolution to this phenomenon came about when serial E²PROMs were introduced to the market. Their incident rate of inadvertent writes was practically zero.

After an investigation it became apparent the complex sequence of events required to write to serial devices was the likely solution. This in fact has been proven to be the situation. Almost all parallel E²PROMs now employ some form of software data protection; which is nothing more than requiring the host to issue a sequence of writes to specific addresses with an alternating bit pattern. This sequence of addresses and data patterns are very unlikely to occur during a reset condition regardless of how sloppy the external power-on reset circuit might be.

This situation naturally held true for serial memories, until recently, that is. Almost all manufacturers' devices now operate over the entire voltage range between 1.8V and 5.5V. That is, regardless of the part number suffix denoting voltage range, a single die from a manufacturer provides all the voltage flavors. In order for the low voltage devices to operate correctly, the internal power on reset (POR) circuits have been set to a value below 1.6V or disabled altogether. Thus, a device operating in a 5V system can still be written even when V_{CC} is well below the system's tolerance level. In most instances this is probably ok, but there is still a 'danger zone' that has been described in detail in Summit's Application Note 001.

However, with a microwire device this type of situation can be exacerbated during a brownout. Refer to figure 1 illustrating a V_{CC} slump (brownout condition), a valid ERASE command sequence (shown as light gray waveforms) which have been superimposed by a waveform during a brownout (black waveforms).

A valid ERASE command is comprised of a start bit (logic 1) and a 2-bit command (2 sequential 1's) and then an address to be erased. Suppose the DI line were held high, CS transitioned high and spurious clocks came in on the CLK line – This would perform an erase at location 3F[H] (for the 9346) or location 7F[H] (for the 9356/66)

Now suppose V_{CC} slumps below the system reset threshold and activates the system reset to the microcontroller. The microcontroller will generally respond by resetting its port lines to a default condition as an input.

Assume EWEN is still valid. V_{CC} is still higher than the memory's POR threshold so the 93xx is still 'write viable'. The port lines are attached to the CS, DI and CLK lines of the 93xx device which are high impedance. If you then look at the superimposed waveforms and assume the three inputs then float above V_{IH} and noise is coupled to the lines, specifically the CLK line, then it can be seen an ERASE will occur at the highest address location of the device.

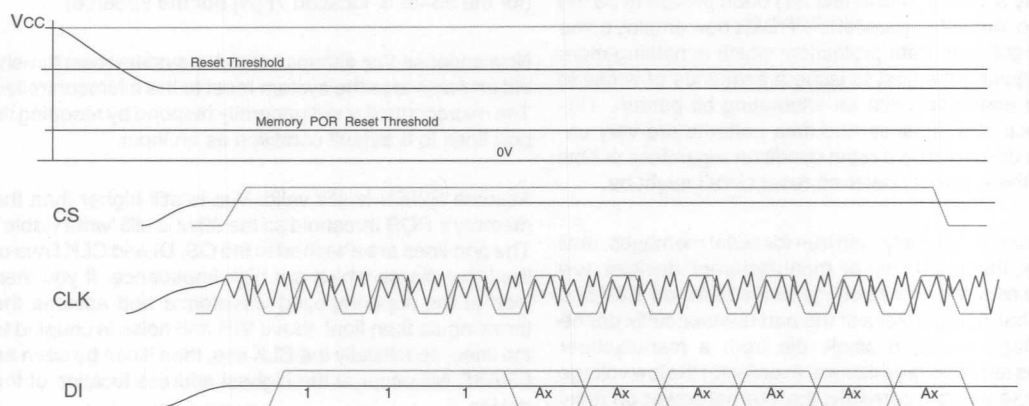


Application Note 3

The only way to protect against this is to coordinate the reset function of the microcontroller with that of the memory. An external reset circuit is not the solution because there is no RESET or DISABLE input to the memory. The best solution is to use the S93663/S93662 or S93VP66 from Summit Microelectronics. This S93663/S93662 is a standard microwire memory, plus it incorporates a precision reset controller. The reset controller is used internally to disable write functions and provide an

open drain output to the system. The S93663 has an active low reset output while the S93662 has an active high reset output.

Alternatively, the S93VP66 could be used. It has the same precision V_{CC} sense circuitry on-board and will disable writes whenever V_{CC} falls below a preset threshold. There are three thresholds currently available to insure proper operation in both 3 Volt and 5 Volt systems.



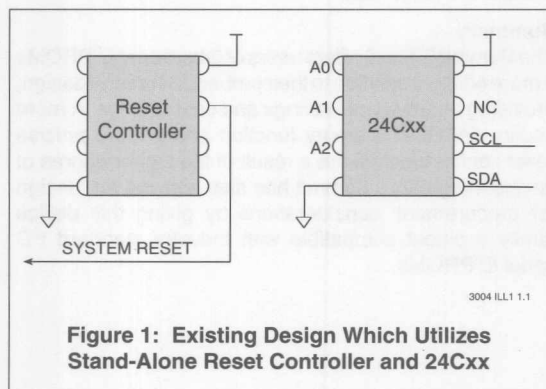
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Using Summit's S24xx3 Precision Reset Controller in Existing Designs

Introduction

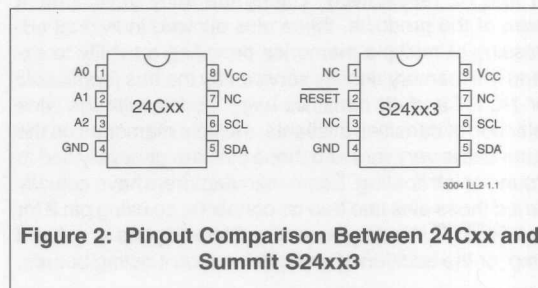
Many existing embedded control systems use a voltage supervisory circuit to provide a reset function for the microcontroller and also use an I²C serial E²PROM (24Cxx) for nonvolatile memory storage. Summit's S24xx3 family of Precision Reset Controllers with I²C E²PROM memory offers a simple replacement for these two devices, not only providing the end user board space savings but most importantly cost savings. This application note illustrates a 'no risk' easy implementation of the S24xx3 devices into existing designs.

Figure 1 illustrates a typical implementation of a reset controller and I²C memory.

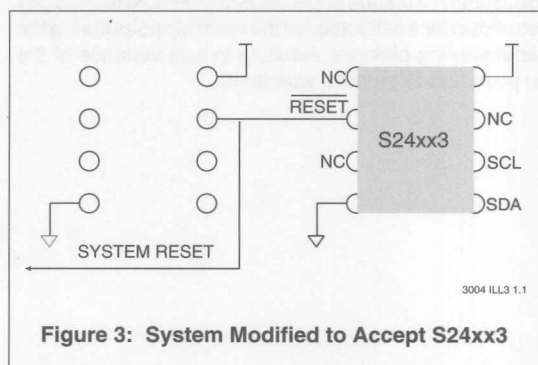


Implementation

The Summit S24xx3 device features a pinout compatible with the I²C serial E²PROM (see Figure 2). The S24xx3 can usually be inserted into the serial E²PROM socket with just one minor



change, the addition of a connection for the SYSTEM RESET signal to Pin 2 of the Summit device (see Figure 3). This may also be accomplished with a jumper wire to preclude revision of the circuit card. No software change is required. Since the S24xx3 provides the precision reset signal required by the microcontroller, the socket reserved for the stand-alone reset controller can now be left vacant (saving substantial cost). Board space savings can be realized by eliminating the reset controller socket altogether.





Miscellaneous Design Issues

The generic I²C memories designate pins 1, 2 and 3 as A0, A1 and A2 respectively. During the early development years of the products, these pins allowed individual addressing of multiple memories providing a facility to expand the memory density serviced by the bus [*applicable for 1K, 2K and 4K densities only*]. Today, with the wide selection of densities available, multiple memories on the same bus is very rare and these pins are generally tied to ground or left floating. Some manufacturers have actually turned these pins into true no connects, so using pin 2 for your RESET should pose no problem beyond a 'cut and jump' or the addition of a single trace on existing boards.

Performance Benefits

The Summit S24xx3 offers users of 24xx serial E²PROMs a more efficient solution to their embedded control design, providing board space savings and cost savings. There are additional benefits that can be realized by using the S24xx3 solution. The V_{CC} sensing circuit, which is used for the reset control function, is now on the same piece of silicon as the E²PROM memory array. This allows the S24xx3 to effectively "shut down" the E²PROM array when V_{CC} drops below the reset threshold. This provides the user with a higher degree of protection against inadvertent writes and data corruption. On the precision reset side, Summit's unique application of E²PROM technology also allows for a calibration of the reset trip point during the manufacturing process, resulting in less variance of the trip point due to process variations.

Second Sourcing

If second sourcing is an issue, Summit's "No Risk Design" will satisfy multiple sourcing requirements. By simply designing a circuit board as shown in Figure 3, the design will feature the S24xx3 as the primary source for the solution. This implementation takes full advantage of component cost savings and reliability enhancements. The second source will be the components that the Summit device replaces: a standard serial E²PROM and a stand-alone reset controller device. Only one minor software change might need to be made to ensure proper communication with the serial E²PROM device. If the replacement memory's A1 input is internally connected then the A1 bit of the I²C protocol will need to be changed from '0' to '1'. This change will match the software protocol to the A1 pin that will now be driven HIGH by the unasserted reset line.

Summary

The Summit S24xx3 offers users of 24xx serial E²PROMs a more efficient solution to their embedded control design, providing board space savings and cost savings. A more secure E²PROM memory function and a more precise reset control function are a result of the higher degree of device integration. Summit has also allowed for 'design for procurement' considerations by giving this device family a pinout compatible with industry standard I²C serial E²PROMs.

Using Summit's S24xx2 Precision Reset Controller in Existing Designs

Introduction

Many existing embedded control systems utilize a voltage supervisory circuit to provide a reset function for the microcontroller; and also use an I²C serial E²PROM (24Cxx) for nonvolatile memory storage. Some systems, especially those that utilize an Intel-style microcontroller (such as an 8051), require an active HIGH reset function. Designs on the higher end of the complexity scale will also contain additional devices that require an externally applied reset signal; most likely an active LOW input. At a minimum, this requires the designer to add an inverter into the microcontroller's reset circuit. The added complexity and additional components mean additional cost. Summit's S24xx2 family of precision reset controllers (with a complementary reset outputs) and an I²C E²PROM offer a simple replacement for the reset control device and the serial E²PROM. Thereby providing the designer with PC board space savings as well as cost savings. Perhaps most important are the technical advantages of having the precision reset control function and the E²PROM function on the same piece of silicon.

The Summit S24xx2 device can be 'designed-into' existing systems with a minimum of effort. This applications note addresses only those systems requiring an active HIGH reset function. For active LOW only reset designs, see Applications Note 004 "Using Summit's S24xx3 Precision Reset Controller in Existing Designs".

The Old Solution

Figure 1, below, represents a typical existing design.

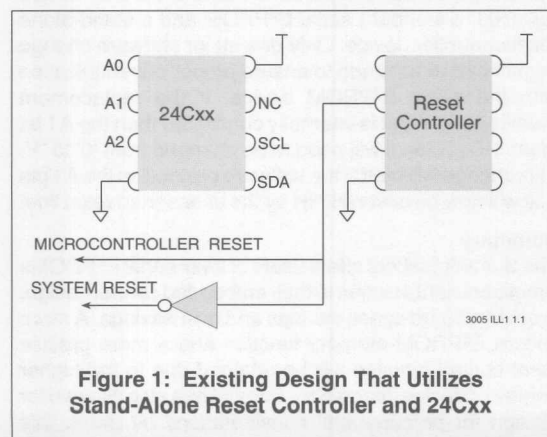


Figure 1: Existing Design That Utilizes Stand-Alone Reset Controller and 24Cxx

Implementation of the Summit Device

The Summit S24xx2 device features a pinout that is compatible with the I²C serial E²PROM (see Figure 2). The S24xx2 can usually be inserted into the serial E²PROM socket with one minor change; the addition of a connection from the RESET signal on Pin 7 to the microcontroller reset input (see Figure 3). This may also be accomplished with a jumper wire to preclude revision of the circuit card. No software change is required. Since the S24xx2 now provides the precision reset signal required by the microcontroller, the socket reserved for the stand-alone reset controller can be left vacant (saving substantial cost). Board space savings can be realized by eliminating the reset controller socket altogether.

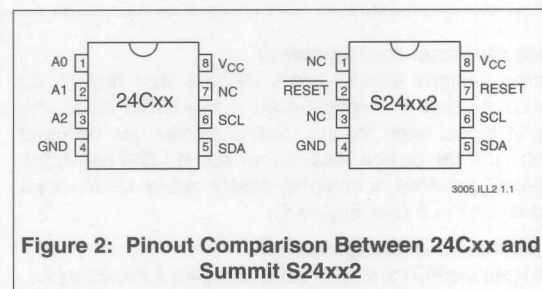


Figure 2: Pinout Comparison Between 24Cxx and Summit S24xx2

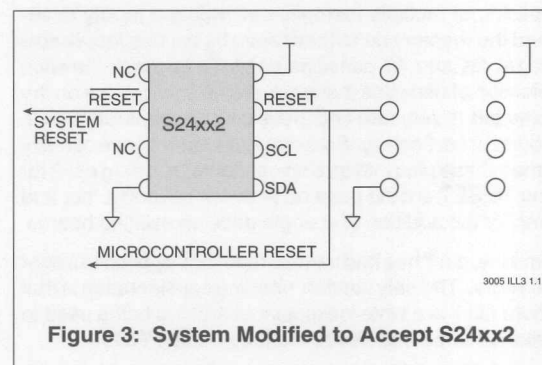


Figure 3: System Modified to Accept S24xx2

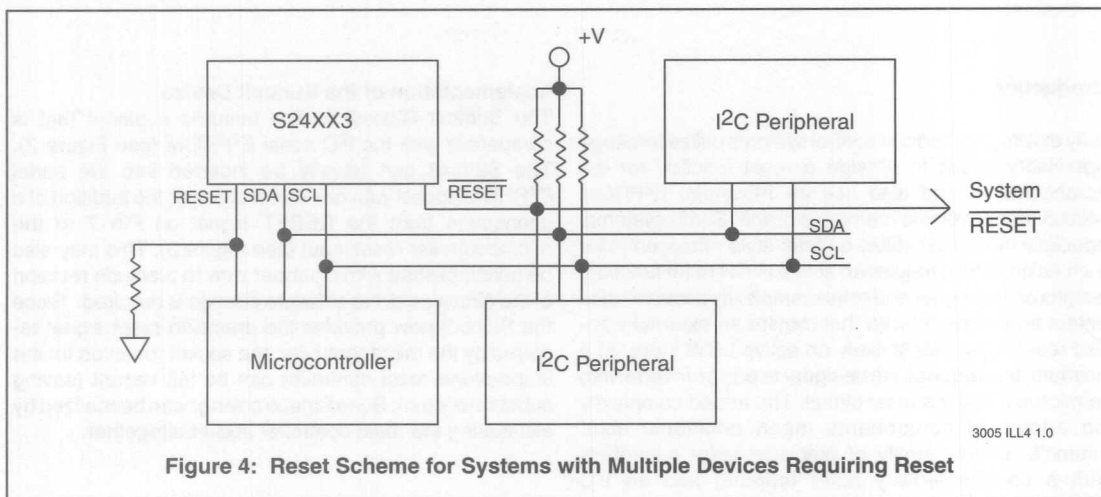


Figure 4: Reset Scheme for Systems with Multiple Devices Requiring Reset

Multiple Reset Requirements

Some designs contain other devices that require an external reset. If it requires an active HIGH reset, the same signal used for the microcontroller can be used (Pin 7). If the device requires an active LOW reset, the S24xx2 provides a complementary active LOW, reset signal on Pin 2 (see Figure 4).

Miscellaneous Design Issues

The generic I²C memories designate pins 1, 2 and 3 as A0, A1 and A2 respectively. During the early development years of the products, these pins allowed individual addressing of multiple memories providing a facility to expand the memory density serviced by the bus [*applicable for 1K, 2K and 4K densities only*]. Today, with the wide selection of densities available, multiple memories on the same bus is very rare and these pins are generally tied to ground or left floating. Some manufacturers have actually turned these pins into true no connects, so using pin 2 for your RESET should pose no problem beyond a 'cut and jump' or the addition of a single trace on existing boards.

Similarly, pin 7 has had various functions applied to it over the years. The only version needing consideration is that where pin 7 is a write lockout input and it is being used to make a normal read/write memory into a PROM.

Performance Benefits

There are technical benefits realized by using the Summit S24xx2 solution. The V_{CC} sensing circuit, which is used for the reset control function, is now on the same piece of silicon as the E²PROM memory array. This allows the S24xx2 to effectively "shut down" the E²PROM array when V_{CC} drops below the reset threshold. This provides

the user with a much higher degree of protection against inadvertent writes and data corruption. On the precision reset side, Summit's unique application of E²PROM technology allows for calibration of the reset trip point during the manufacturing process, resulting in less variance of the trip point due to process variations.

Sourcing

If sourcing is an issue, Summit's "No Risk Design" will satisfy multiple sourcing requirements. By simply designing a circuit board as shown in Figure 3, the design will feature the S24xx2 as the primary source for the solution. This implementation takes full advantage of component cost savings and reliability enhancements. The second source will be the components that the Summit device replaces: a standard serial E²PROM and a stand-alone reset controller device. Only one minor software change might need to be made to ensure proper communication with the serial E²PROM device. If the replacement memory's A1 input is internally connected then the A1 bit of the I²C protocol will need to be changed from '0' to '1'. This change will match the software protocol to the A1 pin that will now be driven HIGH by the unasserted reset line.

Summary

The Summit S24xx2 offers users of 24xx serial E²PROMs a more efficient solution to their embedded control design, providing board space savings and cost savings. A more secure E²PROM memory function and a more precise reset control function will be attained due to the higher degree of device integration. Summit has also allowed for 'design for procurement' considerations by giving this device family a pin-out compatible with industry standard I²C serial E²PROMs.

Using Summit's S93662/S93663 Precision Reset Controller in Existing Designs

Introduction

Many existing embedded control systems utilize a Microwire E²PROM (93Cxx) for nonvolatile memory storage and a reset control device to provide a precision (active LOW) reset function for the microcontroller. Summit's S93663 Precision Reset Controller with 4K bits of E²PROM Memory offers a simple replacement for these two devices, providing the end user board space savings as well as cost savings. In addition, existing designs can be outfitted with the S93663 with a minimum of redesign effort. The S93663 features both an active HIGH output (pin 7) and an active LOW reset output (pin 6). For the purposes of this applications note, examples will relate to designs requiring an active LOW reset, although the contents of this note also apply to designs requiring active HIGH reset functionality. Figure 1 represents a typical existing design.

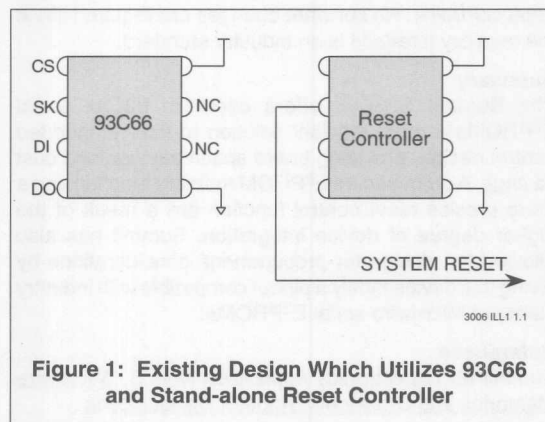


Figure 1: Existing Design Which Utilizes 93C66 and Stand-alone Reset Controller

Implementation

The Summit S93663 device features a pinout compatible with the 93Cxx device (see Figure 2). The S93663 can now be inserted into the serial E²PROM socket with one minor addition, a new

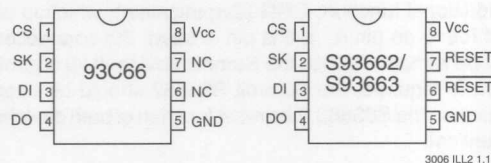


Figure 2: Pinout Comparison Between 93C66 and Summit S93662/S93663

connection for the SYSTEM RESET signal to pin 6 of the Summit device (see Figure 3). This may also be accomplished with a jumper wire to preclude revision of the circuit card. No software change is required. Since the S93663 provides the precision reset signal required by the microcontroller, the socket reserved for the stand-alone reset controller can now be left vacant (saving substantial cost). Board space savings can be realized by eliminating the reset controller socket altogether.

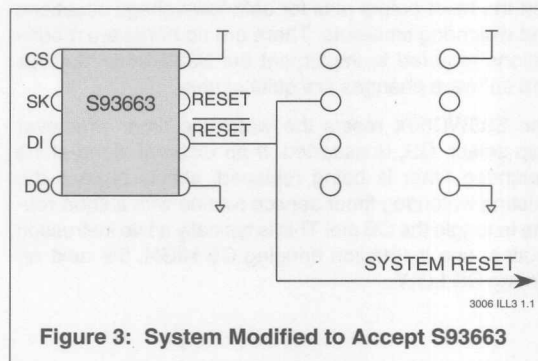


Figure 3: System Modified to Accept S93663



Organization Considerations and the S93662

Most 93C66 devices on the market are internally organized as x16. Some devices offer the user the ability to use the device with a x8 organization. These devices will have an additional function, ORG (Organization), which is an input found on pin 6. If this pin is used, the connection must be removed to use the Summit device. If x8 organization is required, the Summit S93662 should be used rather than the S63663. The reset function of both devices is identical.

Use with Intel and Other Active HIGH Reset Microcontrollers

Some microcontroller products on the market, primarily Intel products, feature an active HIGH reset function rather than active LOW. The S93663 supplies complementary RESET outputs. To implement the Summit device in these systems, tie the system reset line to pin 7 rather than pin 6. Any other devices in your system that may require an active LOW may be reset from the reset output found on pin 6.

Watchdog Timers and the S93WD662/S93WD663

Summit offers versions of the S93662 and S93663 that have an internal 1.6 second (nominal) watchdog timer, the S93WD662 and S93WD663. These devices will assert the reset output pins for both low-voltage situations and watchdog time-outs. There are no hardware modifications required to implement the S93WD66X devices and software changes are quite simple.

The S93WD66X resets the watchdog timer whenever chip select, CS, is asserted. If an external stand-alone watchdog timer is being replaced, simply replace the existing watchdog timer service routine with a short routine to toggle the CS pin. This is typically a two instruction routine, one instruction bringing CS HIGH, the next returning CS LOW.

Performance Benefits

The Summit S93663 offers users of Microwire 93Cxx serial E²PROMs a more efficient solution to their embedded control design, providing board space savings and cost savings. There are additional benefits that can be realized by using the S93663 solution. The V_{CC} sensing circuit, which is used for the reset control function, is now on the same piece of silicon as the E²PROM memory array. This allows the S93663 to effectively "shut down" the E²PROM array when V_{CC} drops below the reset threshold. This provides the user with a higher degree of protection against inadvertent writes and data corruption.

Sourcing

If sourcing is an issue, Summit's "No Risk Design" will satisfy multiple sourcing requirements. By simply designing a circuit board as shown in Figure 3, the design will feature the S93663 as the primary source for the solution. This implementation takes full advantage of component cost savings and reliability enhancements. The second source will be the components that the Summit device replaces: a standard serial E²PROM and a stand-alone reset controller. No software changes are required since the memory interface is an industry standard.

Summary

The Summit S93663 offers users of 93Cxx serial E²PROMs a more efficient solution to their embedded control design, providing board space savings and cost savings. A more secure E²PROM memory function and a more precise reset control function are a result of the higher degree of device integration. Summit has also allowed for 'design for procurement' considerations by giving this device family a pinout compatible with industry standard Microwire serial E²PROMs.

References

Summit Microelectronics Application Note 3. Microwire Memories and Brownouts: Another Danger Zone

Eliminate Your Data Corruption Problems with Voltage Protected Serial E²PROMs

Introduction

Users of serial E²PROMs have often been faced with occasional instances of data corruption. The problem is usually not repeatable but happens often enough to make the determination that it is more than a fluke event. Indeed, once an understanding of the internal workings of the serial E²PROM is achieved, it is easy to see how data corruption can occur from time to time. Summit Microelectronics, Inc. has published several applications notes discussing the causes of data corruption. Consult Applications Note 001, "Preventing Data Corruption in E²PROM Memory Applications" for good general information. Users of I²C serial E²PROMs (24Cxx) should also consult Applications Note 002, "Data Corruption in I²C Serial E²PROMs", while users of Microwire serial E²PROMs (93Cxx) should consult Applications Note 003, "Microwire Memories and Brownouts: Another Danger Zone". The Summit family of Voltage Protected E²PROM devices offers the user a drop-in replacement to commodity serial E²PROMs and will eliminate the problem of data corruption.

Implementation

The Summit family of Voltage Protected serial E²PROMs have been designed as 100% drop-in replacements for industry standard serial E²PROMs. This is true for both hardware and software considerations. The table below shows which Summit Voltage Protected device replaces which problem E²PROM.

Generic E ² PROM	Summit Device
24C01	S24VP02
24C02	S24VP02
24C04	S24VP04
24C08	S24VP16
24C16	S24VP16
93C46	S93VP66
93C56	S93VP66
93C66	S93VP66

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Cross Reference from Unprotected Serial E²PROM to Voltage Protected Serial E²PROM

Virtually all data corruption in serial E²PROMs occurs in low-voltage situations, whether it is during a power-up or power-down cycle or a brownout situation, even when a separate reset controller is used with the microcontroller. The Summit Voltage Protected E²PROM will disable the internal write circuit to the memory array whenever the V_{CC} drops below its lockout voltage, V_{LOCK}. The Summit device has an on-chip precision V_{CC} sense that establishes V_{LOCK} just outside of the users V_{CC} operating range. The Voltage Protected device will remain in lockout for approximately 130mS after V_{CC} has stabilized above V_{LOCK}. This is applicable whether this is a power-up situation or a brownout situation. On power down, the device will lockout all writes when V_{CC} falls past the V_{LOCK} threshold and will remain locked for the remainder of the power down curve (<1V). In all cases, the device is still accessible for read operations but all writes will be ignored.

Hardware Write Protection?

Some standard serial E²PROMs utilize pin 7, normally unused, as a Write Protect pin. This provides adequate protection only when the device is used as an OTP and is not foolproof even then. When used in a normal system, the same conditions that cause inadvertent writes to the serial E²PROM occur that effectively disables the Write Protect pin. In other words, the control of the Write Protection function becomes unreliable when V_{CC} drops out of the proper operating range. Hence, the device is still susceptible to data corruption in all low voltage situations. The best hardware prevention is the *internal* hardware protection offered by the Summit Voltage Protected serial E²PROM.

Summary

Data corruption is a growing issue with standard serial E²PROMs due to the wide range of voltages at which they are designed to operate. Data corruption can prove very costly to both the manufacturers and users of the systems in which the situation occurs. Summit's Voltage Protected serial E²PROM family offers the user of serial E²PROMs an effective solution that will end data corruption problems with no redesign.



Application Note 7

Reset Signal Conditioning Enhances Operation of Modems, LAN NICs, and Other PC Add-in Cards

Introduction

Manufacturers of modems, network interface cards, and other PC add-in cards are faced with the daunting task of designing products which must work around a very broad set of specifications. These units must be able to operate reliably with any machine on the market, regardless of the manufacturer. Performance of these machines may vary greatly and have a great affect on the operation of the add-in card. One area where wide variance of performance has a potentially large impact is the reset function provided by the host machine. The timing and duration of this function coming to the card socket varies greatly and makes it difficult for the engineer to design a card which operates properly in all systems. New requirements such as hot-socketing exacerbate the situation by making the initial operating environment less predictable. This applications note will show how adding a reset conditioning function to the add-in card using Summit's unique precision reset control devices can increase system performance and reliability.

Importance of Reset Control

Reset control has long been a critical aspect of embedded control design and many semiconductor products have been introduced to perform this function reliably. Virtually every microcontroller design now utilizes an external precision reset control circuit. Upon power up, proper reset control ensures that the environment (power, external system, etc.) is stable before the microcontroller is allowed to perform its initialization routines. Failure to do this may result in unreliable operation or system lock-up. Also, the reset control function protects the system during power-down and supply voltage brown-out situations. A single bit being misinterpreted due to marginal thresholds could cause many problems, including the execution of unintended routines, potentially wreaking havoc in the overall system. Data corruption is also a common result of these situations. For these reasons, the use of discreet precision reset controllers has become a standard element of embedded control design. Designers of PC add-

in cards face these same issues plus more worrisome problems relating to the host interface. Insufficient reset from the host machine (and some platforms often give the card no reset at all) may cause the chipset processor to latch-up, a potentially catastrophic situation!

Unfortunately for designers of PC add-in cards, reset devices have traditionally been designed for microcontroller environments where the system is closed and the reset function can be implemented by monitoring the supply voltage. Systems such as PC add-in cards, which are part of a larger system over which the engineer usually has no control, must also consider external signals, impulses, and conditions. The most important of these is the system reset signal. This leaves most semiconductor reset control devices lacking in their ability to perform adequately in the add-in card environment. This problem is exacerbated by the fact that reset control functionality is seldom included in reference designs provided by chipset manufacturers. This puts the designer in a position of incorporating additional, unfamiliar devices to his system (especially painful for PCMCIA designs) which add complexity and cost.

Summit Microelectronics, Inc. has introduced a family of precision reset controllers with advanced features that provide a good fit to the PC add-in card environment. Moreover, these devices allow the user to add reset control functionality without adding a single component to the design! Summit's ability to add E² memory to the reset device provides the user a means to replace the serial E²PROM (typically specified by the chipset manufacturer in the reference design) and also provide a reset control function.

Adding Reset Control

The incorporation of the Summit reset control device into the PC add-in card is quite simple. The system reset signal (RST) coming from the edge-connector is active high and is buffered on the board, usually by an inverter (see Figure 1). Instead of using this buffered input as the card's



Application Note 8

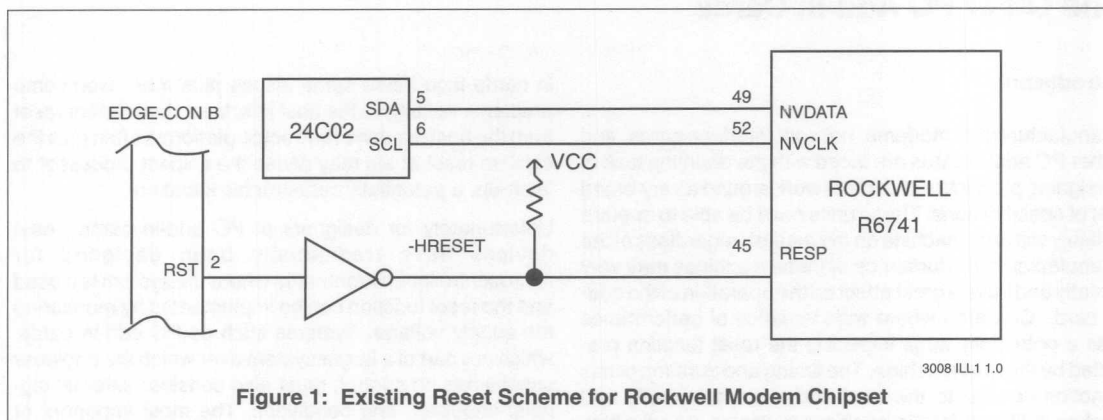


Figure 1: Existing Reset Scheme for Rockwell Modem Chipset

reset signal, it is now used as an input to the Summit device. The Summit device features bi-directional reset pins allowing the system reset signal to be used as an input to the Summit device (see Figure 2). Upon receiving a reset signal from the host system, the Summit device will assert the reset outputs and hold the reset state until a) the reset signal input is unasserted, or b) the t_{PURST} timeout period expires (130mS min), whichever period is longer. This is a critical aspect of the design. The pulse width of the incoming system reset signal varies greatly from machine to machine. Some PC platforms give the card slot a very short reset pulse, a pulse that is not long enough to ensure a reliable reset function for the

chipset(s). In this case, the Summit precision reset controller is now acting as a reset signal conditioner, providing the chipset with an accurate and reliable reset pulse. This will eliminate issues related to platform variances of the reset signal and, more important, give the card designer control over this function. The Summit device will also act as a supply voltage monitor, ensuring that the chipset is operating in a stable environment. When V_{CC} drops below the threshold voltage, V_{TRIP} , the Summit device will assert reset until V_{CC} stabilizes for a period no less than t_{PURST} . Summit Microelectronics, Inc. offers devices with a variety of V_{TRIP} settings and a unique process allows for user-specified trip points.

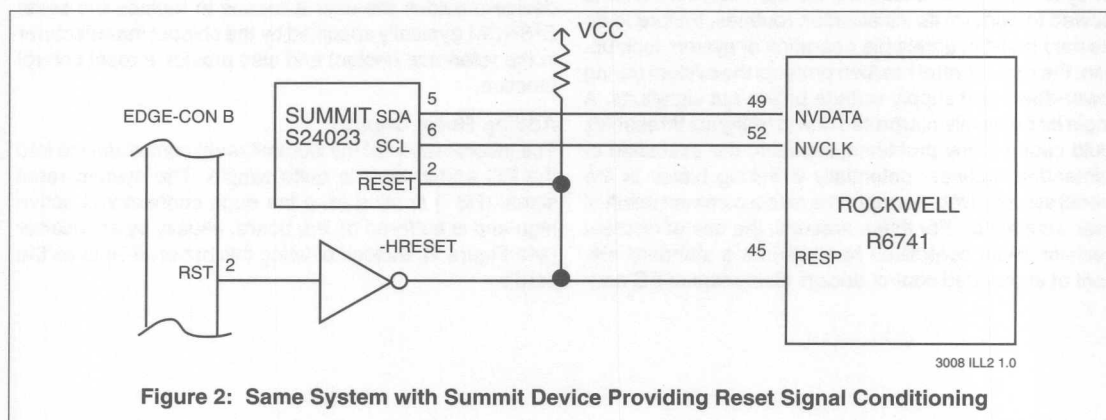


Figure 2: Same System with Summit Device Providing Reset Signal Conditioning

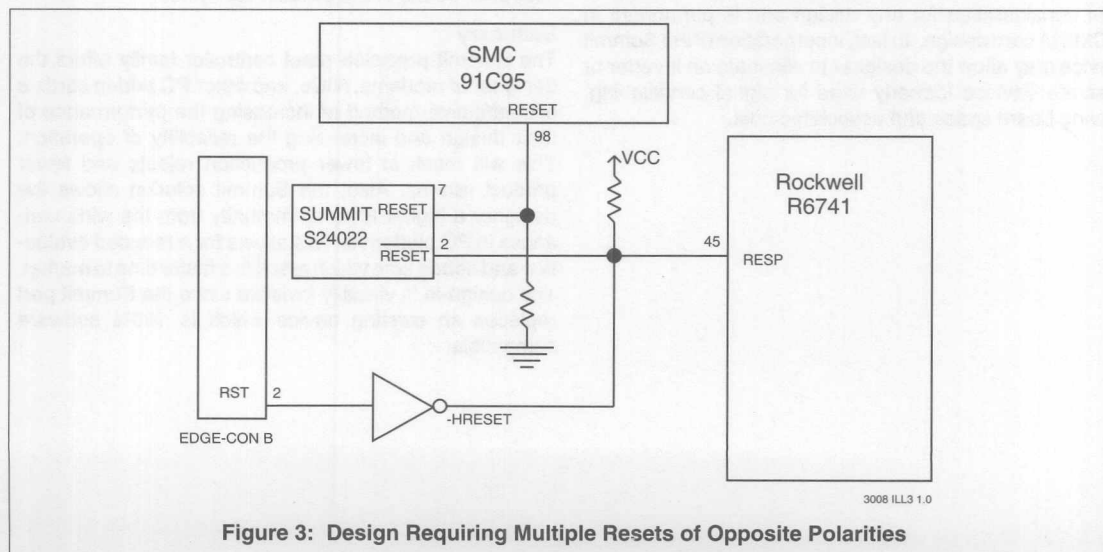


Some designs may have multiple devices requiring reset, such as a PCMCIA card with both LAN NIC and modem capabilities. Both the Ethernet chipset and the modem chipset require reset signals. The characteristics are not always identical. Some devices require active high reset signals while others require active low. Summit's devices feature complementary reset outputs that resolve this problem. When the Summit device receives the system reset pulse, both the reset line used as the input and the complementary reset line will be asserted and will stay asserted as described earlier. This scheme also eliminates the need to invert the incoming reset signal as an active high reset input will be connected to RESET pin (active high) of the Summit device and an active low reset input will be connected to the RESET BAR pin (active low).

It should be noted here that the S24022 device is used in this example as it replaces a serial E²PROM device used by the Rockwell modem chipset. The same result can be achieved by using the S93663 device and replacing the serial E²PROM used by the SMC Ethernet controller. The performance of the reset function is independent of the memory array and interface logic and the user will not see a difference between the two methods.

Until recently, it was required of PC users to turn the power off to a socket prior to insertion of a new card. Failure to do so could have caused the card to operate in an unpredictable manner or possibly do permanent damage to the circuits on the card. This is no longer the case as hot-socketing capabilities are now the norm. This means that the PC add-in card manufacturer must design a circuit that will initialize properly and operate without the benefit of a reset signal from the host. The Summit precision reset controller offers an ideal solution for this situation.

When the card is inserted into the powered socket, the supply voltage will fluctuate wildly due to contact bounce and loading characteristics. This fluctuation may cause the chipset processor to come up in an unknown state, at which point, an external reset must be generated to recover. If the Summit device is used, the system will be held in a reset state until V_{CC} is stabilized and the processor is allowed to initialize under normal conditions. The Summit device will assert the reset lines until V_{CC} has stabilized.





Implementation

The Summit precision reset control device can be incorporated into a typical PC add-in card design without adding a single component. Any modem design or NIC design (and most PC add-in cards in general) will utilize a small serial E²PROM to store set-up data, configuration data, address data, identification data, and possibly some user-defined parameters. This device will interface to the chipset via one of two industry standard serial busses, I²C (two-wire) or Microwire (4-wire). The chipset manufacturer's reference design will call out which interface and what density is required.

Summit's precision reset controllers are unique in that the E²PROM memory array has been incorporated into the silicon. Summit offers these devices with both I²C (S24xx2) and Microwire (S9366x) interfaces so that it becomes a drop-in replacement for the serial E²PROM. The unused pins of the serial E²PROM device are used to provide the reset I/O's. Table 1 shows which Summit Microelectronics device should be used given the serial E²PROM called out in the reference design. The software used to communicate with the generic E²PROM is 100% compatible with the Summit device. For more information regarding the drop-in compatibility of the Summit device with the serial E²PROM, consult Summit Application Note 005, "Using Summit's S24xx2 Precision Reset Controller in Existing Designs" for I²C interfaces or Summit Application Note 006, "Using Summit's S93662/S93663 Precision Reset Controller in Existing Designs" for Microwire interfaces.

Because the Summit device drops into an existing socket, no additional components are required. This is an important consideration for any design and is paramount in PCMCIA card design. In fact, incorporation of the Summit device may allow the designer to eliminate an inverter or discrete devices formerly used for signal conditioning, saving board space and associated cost.

	Generic E ² PROM	SUMMIT Device
I ² C	24C01A	S24022
	24C02	S24022
	24C04	S24042
	24C08	S24163
	24C16	S24163
Microwire	93C46	S93663
	93C56	S93663
	93C66	S93663

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Table 1: Cross Reference from Serial E²PROM to Summit Reset Controller Device

Additional Benefits of Summit Solution

The integration aspect of the Summit device offers additional benefits that are very important to the overall reliability and performance of the system. Stand-alone serial E²PROMs are inherently susceptible to data corruption, especially during brown-out (low V_{CC}) situations, power-up sequences, and power-down sequences. The Summit device features an internal lock-out feature that shuts down the write capabilities of the chip when the system is in reset. This protects the E² memory array from data corruption much more effectively than external write control pins. Data corruption can be, at best, a nuisance to the user, and at worst, catastrophic. Elimination of even small incidents of data corruption can save considerable cost at all points of the product life cycle.

Summary

The Summit precision reset controller family offers the designer of modems, NICs, and other PC add-in cards a cost-effective method of increasing the performance of their design and increasing the reliability of operation. This will result in fewer production rejects and fewer product returns. Also, the Summit solution allows the designer a higher level of immunity from the wide variances in PC platforms. This allows for a reduced evaluation and debug time which result in a faster time to market. The design-in is virtually invisible since the Summit part replaces an existing device which is 100% software compatible.

Using the S39421 as the Primary Control Circuit on a VME Live Insertion Card

High availability is a key feature of many types of systems today. Whether the system is a central office switch, a private branch exchange or a server it is important the system stay up and running while adding new services (add-in cards) or replacing faulty boards. Therefore, a means for inserting and removing cards while the entire system is powered-on (live) is a necessity.

Live insertion poses a number of challenges for the add-in card designer. For live insertion to be trouble free we first need to prevent damage to components on the add-in card due to improper supply sequencing. Secondly, voltage drop on the system power busses must be prevented in order to avoid unwanted system reset condition. Lastly, the integrity of the system's signals needs to be maintained when additional circuitry is connected to the bus.

Based upon the proposed Live Insertion System Requirements the S39421 is an ideal candidate as the add-in card's live insertion controller.

Sequencing the Voltages

The proposed live insertion specification¹ outlines 26 operational steps during the insertion of a card. These are broken down into two major categories; the "Insertion Process" and the "Typical Board Recognition Process."

The first 6 steps have to do with the insertion of the card and sequencing the discharge of any voltage potentials so that by the time the board is ready to make contact with the backplane no ESD discharges will occur. Even though the balance of the actions tend to overlap they can be

viewed as two operations: the add-in card/backend logic sequencing and the backplane/add-in card interface sequencing.

Add-in Card/Backend Logic Sequencing

The process of electrical insertion begins with the contact of special ground and voltage pins. These are longer than the signal and power pins and they are physically located at opposite ends of the connector. The voltage pins are labeled Vpc (pre-charge Voltage), this is the backplane's 5 volt supply and the intent is for this voltage to be used to power the sequencing circuitry, any ASICs that interface to the bus and to pre-charge the 'bus-side' lines of the signal transceivers.

The PC board should be laid out so that ground is routed to all circuits, i.e. grounds should not be linked via the PCB connector. Vpc should be tied directly to the VCC5 pin on the S39421 and the device will immediately begin driving its backend circuit control signals [SGNL_VLD, CARD_V_VLD, RESET and RESET] and it will place the voltage ramp control signals [VGATE3, VGATE5 and DRVREN] in the off state.

The next step is for the controller to recognize that the board is properly seated in the connector. VME has an optional feature that lends itself ideally to this step of the operation; the ejector handles can be used to activate a switch when they are fully rotated and locked. Switch closure can be used as the PND1 and PND2 inputs on the S39421. The pull-up resistor used for this implementation must be tied to Vpc because the backend voltages will not yet have been switched on by the S39421.

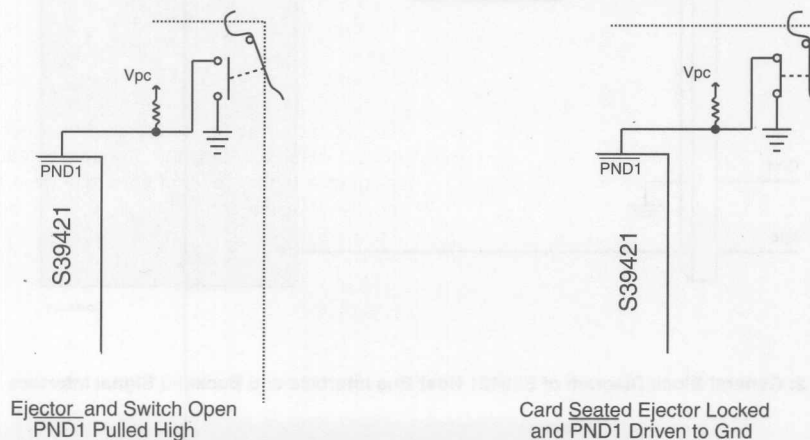


Figure 1: Illustration of Card Injector/Ejector Switch Circuit.



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The board's pins should now be mated with the backplane connector which in turn will bring the host LI/I^* and $RESET^*$ signals to the S39421. These signals should be tied to the device's HST_PWR and HST_RST inputs respectively. Whenever HST_PWR is low the outputs controlling the backend power on sequencing will be inhibited; it does not impact the reset outputs or reset timer. When low, the HST_RST input will force the reset outputs active; once it is released the reset timer will be started and it will keep the reset outputs active for t_{PWRST} .

At the same time the signal pins are making contact, the backend voltages are applied to the card (3.3V, 5V, +12V and -12V on short pins), but, they are blocked by FETs under the control of the S39421 (see figure 3). Depending upon the state of the $VSEL$ pin, the S39421 will monitor either the bussed +5V only, the bussed +3.3V only or both the bussed +5V and +3.3V. Once the S39421 has determined these supply voltages are at or above V_{trip} , (and LI/I^* has released HST_PWR) it will release the $VGATE$ outputs and effectively turn them on at a rate equivalent to 250V/second. At the same time it will force $DRVREN$ active thus providing power to the backend circuits.

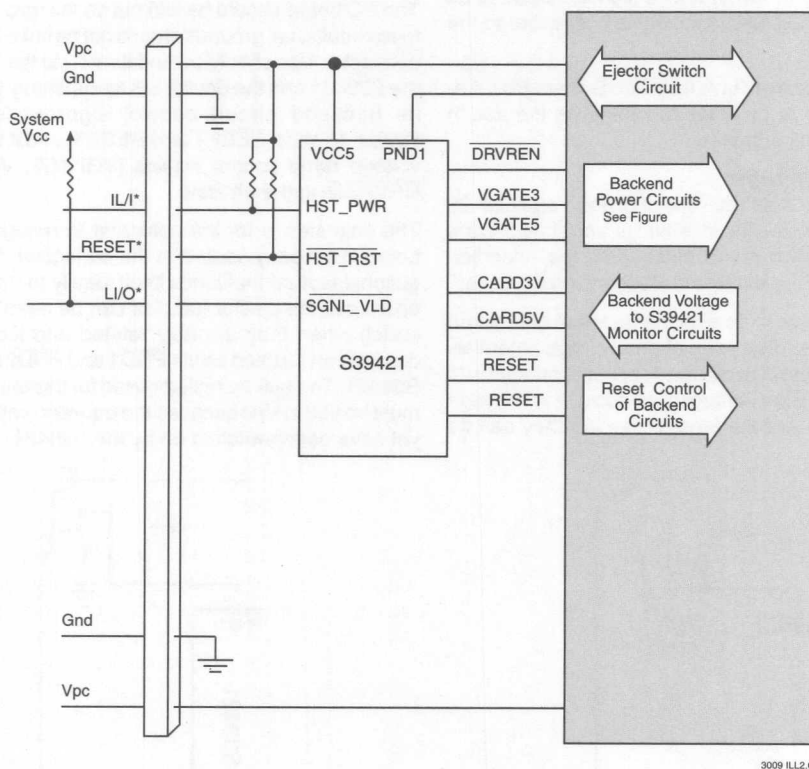


Figure 2: General Block Diagram of S39421 Host Bus Interface and Backend Signal Interface

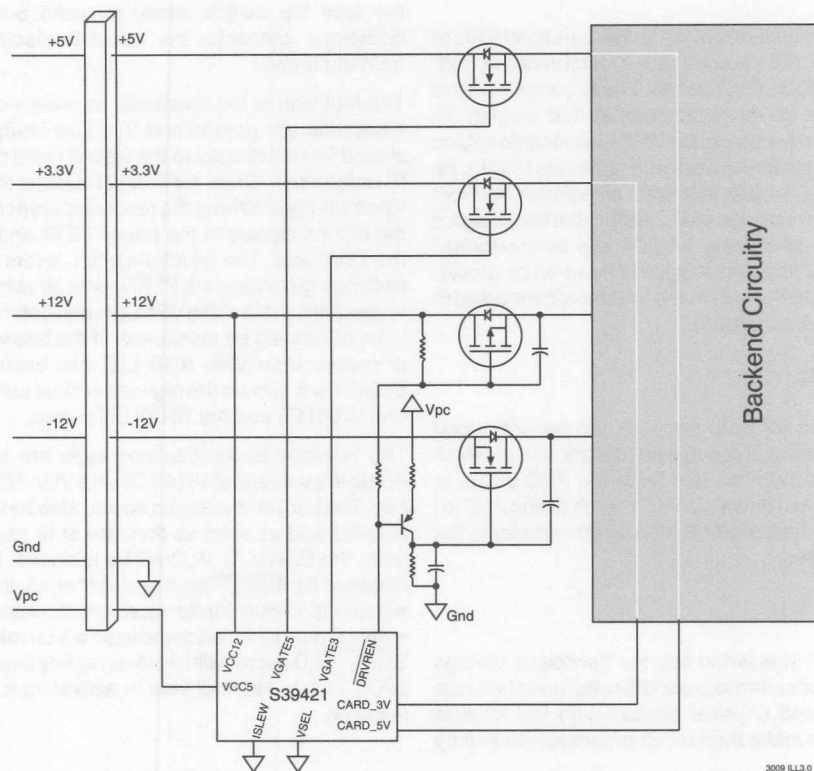


Figure 3: Backend Voltage Control Circuit

The S39421 will now begin monitoring the backend circuit voltages and when they are at or above V_{trip} the reset timer will be released to begin the time out period and $CARD_V_VLD$ will be released. After t_{PURST} has expired, the reset outputs will be released and $SGNL_VLD$ will be driven active. The $SGNL_VLD$ signal can be tied to the host LI/O^* signal pin to indicate the card has been fully powered, cleanly reset and is ready for action.

Backplane/Add-in Card Sequencing

A more complicated problem than the sequencing shown above is the signal bus interface. Inserting unpowered circuits onto the signal bus could lead to a situation of damaging components and much more likely disrupting the signals on the backplane. This will involve a rigorous evaluation and selection process by the design engineer to determine the best solution for the individual application. However, we can examine a product family that should resolve most of the issues the designer might encounter. The proposed VME Live Insertion spec actu-

ally helps us narrow this down quickly by recommending the use of ABTE logic. This is available from at least two large manufacturers of semiconductors.

Avoidance of Bus Conflicts

Bus conflicts arise when two or more interface circuits attempt to drive the bus simultaneously with one circuit driving high and the other driving low. The device trying to drive low will most likely not incur damage. But the device trying to drive high will be dropping 5Volts on its output at up to 120mA current. Even for very short periods of time the high temperatures this will generate can either destroy the device or adversely affect the long-term reliability of the device. The best solution is to insure the transceiver's enable input is actively driven before the transceiver is powered-on. Using one of the reset outputs (as shown in figure 4) as a gating signal to a single enable input style transceiver is one solution. With a dual enable transceiver one of the reset outputs can be tied directly to appropriate enable input.



Pre-bias

The switching capacitance of the individual signal lines at the interface must be charged to the instantaneous voltage on the corresponding bus line. These currents distort the signal that is being transmitted at that instant. To address this issue the proposed VME Live Insertion Spec states: "All VME system drivers and receivers SHALL be pre-biased to 1.7 ± 0.2 Vdc with a resistive network powered by the pre-charge +5V... before the board signal pins contact the backplane VME64 bus connector(s)." The ABTE logic addresses this issue head-on by providing a separate VCCBias pin that is internally connected to a pre-charge resistor network.

CARD REMOVAL

A clean transition for card removal can be performed either by the opening of the injector/ejector levers which in turn opens the switches that force the $\overline{\text{PND}}$ inputs to ground or by the host driving LI/I^* low. Both actions will tell the S39421 to disable the high side drivers and force the reset outputs active.

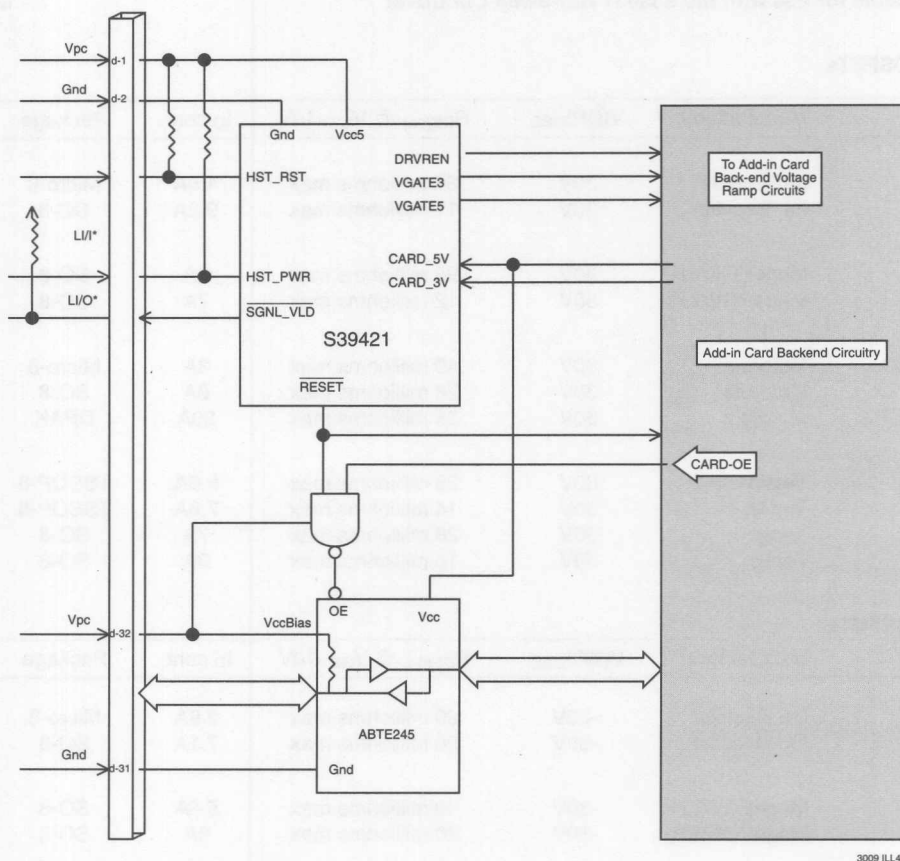
RECAP

As the board is first inserted into the backplane voltage potentials on are shunted to ground thru the use of various bleed resistors and physical contact with the chassis frame. These are made then break processes so that by

the time the card is ready to make contact with the backplane connector the board is electrically isolated from the frame.

The first pins of the connector to make contact with the backplane are ground and Vpc (pre-charge VCC). Vpc should be tied directly to the S39421 and the transceiver BiasVcc input. Once the S39421 detects the presence of Vpc it will begin driving the reset outputs active, shut off all the control signals to the power FETs and begin driving the LI/O^* low. The injector/ejector levers will close the switches grounding the $\overline{\text{PND}}$ inputs allowing the S39421 to check the state of the VSEL pin and determine what bus voltages should be monitored. If the bus voltages are at or greater than Vtrip AND LI/I^* has been released the S39421 will turn on the high side driver outputs VGATE3 and VGATE5 and the $\overline{\text{DRVREN}}$ output.

The voltages to the backend logic are applied with a nominal slew rate of VGATE3 and VGATE5 set at 250V/sec. The backend voltages should also be fed back to the S39421 and as soon as they are at or above their Vtrip level, the CARD_V_VLD will be released. If the host has released its $\overline{\text{RESET}}$ input and LI/I^* input, the S39421 will release the timer for its reset circuit. After tPURST the reset outputs to the backend logic will be released and the SGNL_VLD output will be driven active [backplane signal LI/O]. This is the final step in activating a board for live insertion.



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Figure 4: A Bus Interface Solution



Appendix A

MOSFETs suitable for use with the S39421 Hot-Swap Controller

Mar-98

N-Channel MOSFETs

Part Number	Manufacturer	V(BR) _{DSS}	R _{DS(on)} @ V _{GS} =10V	I _D cont.	Package
IRF7603	Int. Rectifier	30V	35 milliohms max	4.5A	Micro-8
IRF7413	Int. Rectifier	30V	11 milliohms max	9.2A	SO-8
Mi4412	MagePOWER	30V	28 milliohms max	7A	SO-8
Mi4410	MagePOWER	30V	12 milliohms max	7A	SO-8
MTSF3N03HD	Motorola	30V	40 milliohms max	3A	Micro-8
MMSF7N03HD	Motorola	30V	28 milliohms max	8A	SO-8
MTD20N03HDL2	Motorola	30V	35 milliohms max	20A	DPAK
Si6434DQ	Temec	30V	28 milliohms max	5.6A	TSSOP-8
Si6410DQ	Temec	30V	14 milliohms max	7.8A	TSSOP-8
Si4412DY	Temec	30V	28 milliohms max	7A	SO-8
Si4416DY	Temec	30V	18 milliohms max	9A	SO-8

P-Channel MOSFETs

Part Number	Manufacturer	V(BR) _{DSS}	R _{DS(on)} @ V _{GS} =10V	I _D cont.	Package
IRF7606	Int. Rectifier	-30V	90 milliohms max	2.9A	Micro-8
IRF7416	Int. Rectifier	-30V	20 milliohms max	7.1A	SO-8
Mi4431DY	MagePOWER	-30V	40 milliohms max	5.8A	SO-8
Mi4435DY	MagePOWER	-30V	20 milliohms max	8A	SO-8
MTSF2P03HD	Motorola	-30V	90 milliohms max	2.4A	Micro-8
MMSF3P02HD	Motorola	-20V	75 milliohms max	3A	SO-8
MTD20P03HDL2	Motorola	-30V	99 milliohms max	19A	DPAK
Si6435DQ	Temec	-30V	90 milliohms max	4.5A	TSSOP-8
Si6415DQ	Temec	-30V	19 milliohms max	6.5A	TSSOP-8
Si4431DY	Temec	-30V	40 milliohms max	5.8A	SO-8
Si4435DY	Temec	-30V	20 milliohms max	8A	SO-8

References:

VITA Standards Organization, November 1997, *VME64x Live Insertion System Requirements Draft Standard*

Summit Microelectronics, Inc. S39421 Data Sheet

Texas Instruments Application Note SDYA012, October 1996, *Live Insertion*

Using Summit Reset Controllers in Multi-Microcontroller Systems

Introduction

In many systems today, the control algorithm is divided among more than one microcontroller. This distributed processing approach provides greater overall processing bandwidth as well as a modularization of the design for various versions of the end product. In these systems care must be taken to insure that all microcontrollers in the system are properly reset during power-up, power-down and brownout conditions; especially in systems which utilize a nonvolatile memory such as a serial E²PROM. In addition to insuring that the individual microcontrollers are reset properly, the microcontrollers must also be synchronized to insure proper operation. This application note will outline the utilization of the SUMMIT S24042 Precision Reset Controller and nonvolatile memory in a dual MCU television chassis.

Requirements

In many television chassis today, a separate MCU is used to control the on-screen display for control of the television parameters through the use of user-friendly menus. This MCU is often referred to as the On Screen Display processor or OSD MCU.

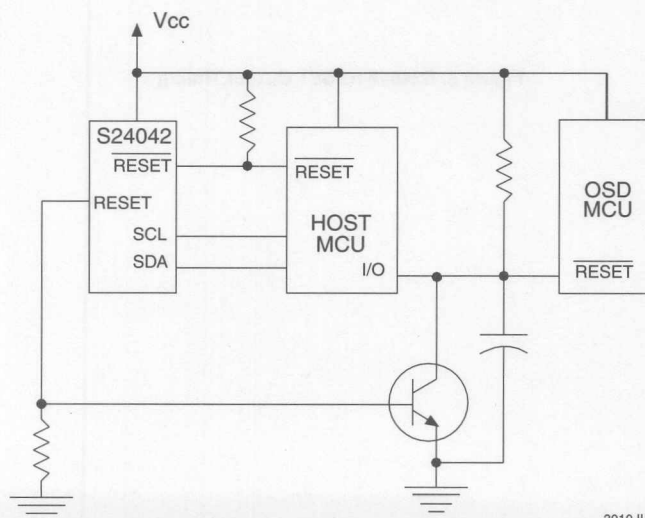
The main MCU in the television controls the operation of the tuner, display and user interface and is often referred to as the Master MCU; since it can control all other circuitry in the television including the OSD MCU. The Master MCU uses an I²C serial E²PROM to store various user

and factory programmed setup parameters including those controlled through the menus displayed by the OSD MCU.

During power up, both MCUs must be reset and it is often desirable that the Master CPU is released from the reset after the supply voltages are stable, but before the OSD MCU is released from reset. In addition to this, the Master MCU must be able to generate a reset condition to the OSD MCU via software control, and once this condition is triggered, the OSD MCU must be held in the reset state for the proscribed interval. During power-down, both MCUs should be held in reset as soon as V_{CC} drops below the operational voltage of the chassis; and, during a brown-out situation, both CPUs will need to be reset and re-synchronized. During a brown-out situation, it is imperative that the V_{CC} sensor used to generate the RESET signals to the MCUs is the same, in order to prevent a situation where one MCU might get reset while the other does not.

Implementation

Figure 1 [on the following page] shows a solution to this multi-MCU design. The S24042 precision reset controller is connected directly to the RESET input of the master microcontroller. The I²C interface from the S24042 is also tied to two I/O ports of the master microcontroller. The S24042 RESET and RESET outputs will be active on power-up as soon as V_{CC} is above 1.0 volts.



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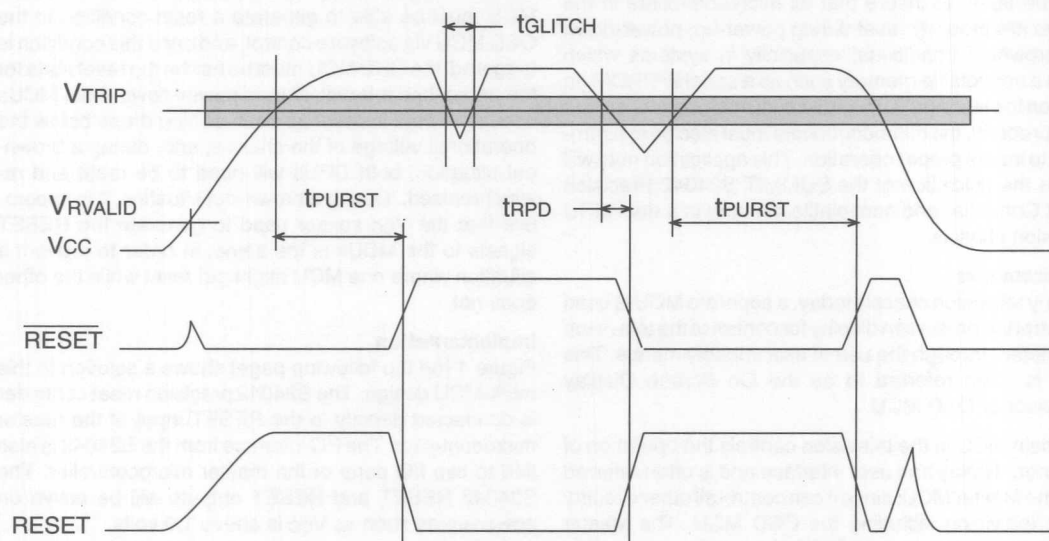
Figure 1. Multi-MCU Reset Circuit Solution



Application Note 10

The S24042 will hold RESET low until V_{CC} reaches the reset controller trip point of 4.4 volts. An internal timer then begins to time the reset interval of t_{PURST} which is typically 120 msec. After this time has elapsed, the Master MCU

will be released from the Reset state. If V_{CC} drops below the reset trip point for longer than 50 nsec, the S24042 will again assert the reset signal. Figure 2 shows the output of the S24042 Reset Controller at the various supply conditions.



3010 ILL2.0

Figure 2. S24042 RESET Output Timing



The slave MCU's reset signal is further delayed by the capacitor on the reset line. This capacitor and its related pull-up resistor should be chosen to insure that the RC time constant will give the adequate reset pulse time for the slave MCU. Reset signals for the slave which are generated by the S24042 reset controller will have a duration of t_{PURST} + the rise time of the RC network.

The Host MCU resets the slave MCU by driving the I/O line low. Once the I/O line is released, the capacitor will time out a reset interval based upon the RC time constant. Care should be taken to insure that the I/O controlling the

reset line is driven low long enough to discharge the capacitor, and in no case should this I/O should be configured to output a High logic level. Rather, to deassert the reset, this I/O should be left in high impedance state or configured as an input, see Figure 3 below.

During a brown-out situation, the S24042 will drive the master reset line low for 120 msec to insure that the timing capacitor is fully discharged. Once the master reset line is driven high, the timing capacitor will generate the proper reset timing for the slave MCU.

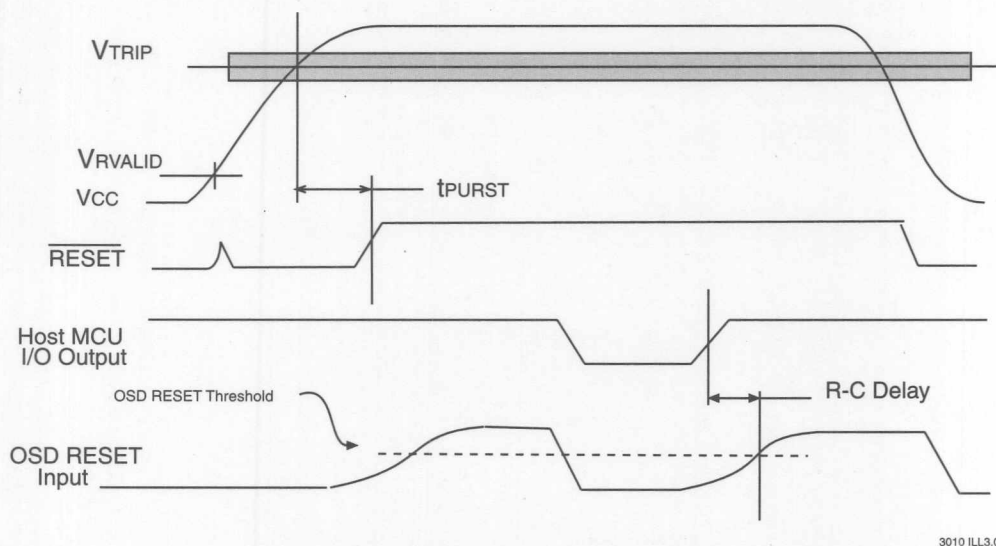


Figure 3. Delay Reset Timing to the OSD MCU



The first step in the process of determining the concentration of a substance in a sample is to weigh a known amount of the sample. This is done by placing a small amount of the sample in a weighing boat and weighing it on a balance. The weight of the sample is then recorded. The next step is to dissolve the sample in a known volume of solvent. This is done by adding the sample to a volumetric flask and filling it to the mark with solvent. The volume of the solution is then recorded. The concentration of the solution is then calculated by dividing the weight of the sample by the volume of the solution.



Figure 1: Response of the detector to various input signals.

A Comparison of Reset Control Methods

Introduction

There are a wide variety of devices on the market that can be used to provide the reset control function for microcontrollers and chipset processors. As with any other functional block in a system, the traditional inverse relationship of functionality versus cost has applied. In situations such as this, designers have been faced with choosing a circuit that provided a minimum of protection to incur a minimum of cost. This has proved to be a difficult task as the type of problems that the reset control function protects against are intermittent and are influenced by a myriad of unpredictable conditions. Summit has approached this problem by integration, resulting in devices featuring a robust reset control function with features sufficient to resolve most issues designers face while remaining a low-cost solution. This application note will take a look at what features are important to reset control and why and provide a comparison between the Summit reset control device and other solutions available to the designer.

Feature Comparison

The following table lists the most common solutions to the microprocessor reset control function and a comparison of features.

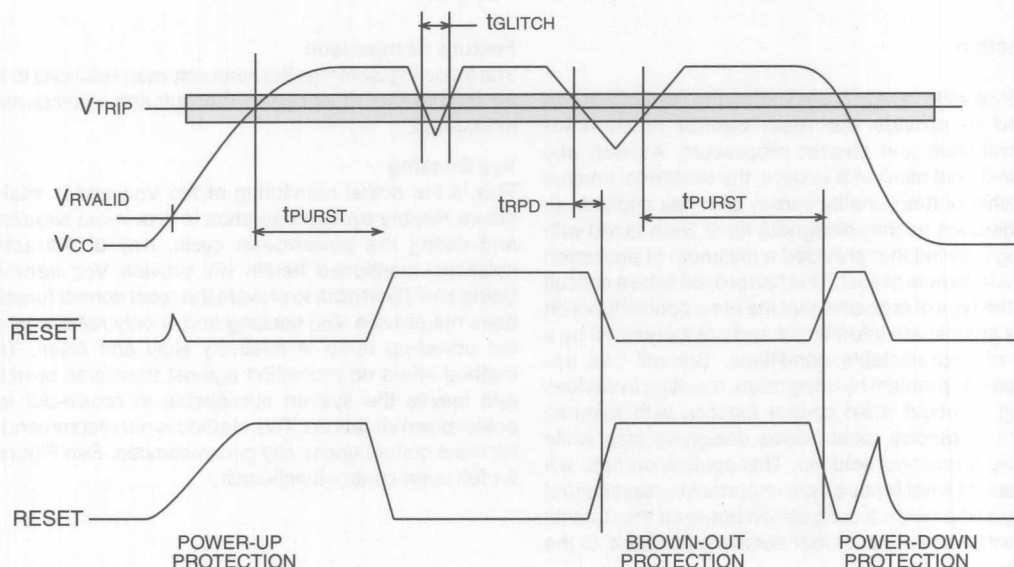
V_{CC} Sensing

This is the actual monitoring of the V_{CC} and is vital to insure reliable system operation in brown-out situations and during the power-down cycle. Any of the active solutions mentioned herein will provide V_{CC} sensing. Using an RC network to provide the reset control function does not provide V_{CC} sensing and is only reliable when the power-up ramp is relatively slow and clean. This method offers no protection against transients or noise and leaves the system susceptible in brown-out and power down situations. This method is not recommended for reset control under any circumstances. See Figure 1 for full reset control functionality.

	V _{CC} Sensing	Reset Valid <1V	Reset Pulse Timing	Reset Valid on Power Down	External Reset	External Reset Filtering	Brownout Protection	Tri-State Protection
SUMMIT RESET CONTROLLER	X	X	X	X	X	X	X	X
R/C NETWORK			X					
VOLTAGE SENSOR	X	X		X				
SUPERVISORY CIRCUIT	X	X	X	X	X		X	

3011 ILL T1.0

Table 1: Comparison of Common Reset Control Options



3011 ILL1.0

Figure 1: Protection Provided by Reset Control Circuits

Reset Valid <1V

The ability of the reset control functional block to guarantee a valid reset signal lower than 1 volt is important to the overall system operation and integrity. The various devices in a given system will be operable to voltages much lower than specified. Problems occur when a microcontroller, or other device relying on the system reset function, is running but the voltage levels are not sufficient to determine HIGH and LOW states reliably. This can result in errant op-code fetches, jumps to incorrect locations, the storage of incorrect data, etc. If incorrect data is written to a nonvolatile memory such as a serial E²PROM, which are capable of accepting writes to voltages as low as 1.5V, the damage inflicted cannot be recovered by a subsequent reset cycle or power cycle. The correct data is lost.

The active solutions to reset control will feature a reliable reset to below 1V. Once again, the RC network solution does not and should be considered too high a risk to use in good microcontroller design.

Reset Pulse Timing

Once reset is detected, the reset control function asserts a reset signal on the output. A voltage detector solution will only assert the reset as long as the V_{CC} is below the threshold voltage and will unassert the reset signal immediately upon V_{CC} reaching the threshold voltage. In power-up and power-down situations, the V_{CC} ramp may not be linear. In brownout situations, the V_{CC} level may waver and criss-cross the threshold repeatedly. The reset output of the voltage detector solution will oscillate in these situations. This will also happen in systems when a mechanical power switch is used where switch bounce upon power-up causes dramatic swings in the V_{CC} level before it stabilizes. These oscillations, or bounces, of the reset output are potentially hazardous. The microcontroller might lock-up and require a manual reset of the system or, worse yet, may latch-up causing permanent damage. The reset signal should be long enough to ensure that the condition requiring reset is cleared and long-enough that the microcontroller can respond reliably to the input.



Reset Valid on Power-Down

Many of the failure modes that proper reset control protects against are of a permanent nature, such as corruption of nonvolatile memory, which are especially susceptible at power-down. Without proper power-down protection, the system allows V_{CC} to decay to zero and the microcontroller is allowed to run freely until it is no longer capable of clocking itself internally. There is a range of V_{CC} where the microcontroller will still be able to process information but the data it reads, including op-code fetches, may be misinterpreted due to ambiguous levels. This is one of the primary causes of data corruption in nonvolatile memories such as serial E²PROMs. Any active solution of reset control will provide this protection but an RC network solution will not.

External Reset

Some applications require system reset from more than one source. For example, a system software signal may be provided to generate a local card reset, or, a mechanical reset button that a user can depress to cause a master reset may need to be implemented. The only clean and reliable way to implement this is with active reset control devices. The ability to tie these all together can be found on a few of the active reset control devices. The Summit device RESET lines are bi-directional and can accept a reset input (see Figure 2).

External Reset Filtering

The reset pulse generated by a reset controller in a low-voltage condition is very reliable. External reset signals, however, can be unreliable and the designer often has little control over their characteristics. Designers of PC add-in cards must design circuits that react to reset pulses originating from the ISA bus which may be a few nanoseconds in width (see App Note 008, "Reset Signal Conditioning Enhances Operation of Modems, LAN NICs, and

Other PC Add-in Cards"). Reset signals originating from an external RESET button are usually quite long but are initially unstable due to switch bounce. Very short reset signals or bounces in the reset signal may cause the microcontroller to lock-up or even latch-up (see Figure 3).

Where there is a requirement for combining low-voltage reset with an external reset, the Summit reset control provides filtering for the incoming signal. A short incoming reset pulse (<40nS) will trigger the reset output of the device with identical timing as if the reset originated from a low voltage condition. The Summit reset control function provides a debounce function to the switch reset input and gives reliable system reset signal, preventing latch-up. The more rudimentary forms of reset control, such as voltage detectors and RC networks, do not provide reset filtering, nor do the other stand-alone reset devices and supervisory circuits on the market.

Brown-out Protection

Many methods of reset control are capable of generating a reset signal upon power-up and power-down but not all methods provide protection in brown-out situations where the V_{CC} dips just below the proper operating threshold. This condition may cause unreliable system operation. Problems may occur due to misinterpretation of an op-code or a memory location by the microcontroller resulting in the unintentional execution of random modules or the writing of incorrect data. Overall system operation becomes unreliable and unpredictable and this is a significant cause of data corruption in nonvolatile memory. In addition, other devices in the system may not operate properly outside the recommended range of V_{CC} . Only active devices designed for reset control have brown-out protection. Use of RC networks and voltage detectors leave the designer at risk in these unpredictable situations.

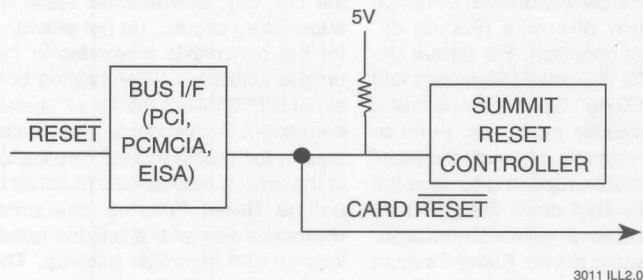


Figure 2: External Reset Utilizing Summit's Bi-Directional Reset Line



MECHANICAL RESET SWITCH

switch bounce may cause latch-up

EXTERNAL RESET

200nS - Too Short for Proper Card Reset

EXTERNAL RESET

FILTERED RESET

150 mSec

3011 ILL3.0

Figure 3: Reset Filtering

Tri-State Protection

This is perhaps one of the most important aspects of reset control. When a microcontroller is put into a reset condition, the port pins go are tri-stated. Control lines to peripheral devices are therefore left floating and are much more susceptible to noise and transients coupling onto them. One of the most common causes of data corruption in serial E²PROMs, especially Microwire (93Cxx) devices, occurs in this tri-stated condition. For further details, see Application Note 003, "Microwire Memories and Brownouts: Another Danger Zone". Good reset control is essential for protecting nonvolatile memories. In these situations however, it is not enough. The only foolproof way to prevent this type of data corruption is to have the reset control function directly shut down the E²PROM memory array. This can only be accomplished by incorporating both functions on the same silicon. Summit's reset control family are the only products capable of providing this critical protection against data corruption.

Summary

Good reset control design is essential to ensure proper operation of an embedded control system. "Cheap and dirty" solutions leave the designer susceptible to numerous potential hazards, many of which are unpredictable and may only manifest themselves in the field rather than the lab. Still, conventional reset controller devices, or supervisory circuits, do not provide complete protection for the nonvolatile memories in the system. Summit's unique solution if incorporating both reset control with serial E²PROM eliminates *all* causes of low-voltage data corruption. Conventional reset controllers are also inadequate for "multiple reset" applications where the nature of the reset is inconsistent (such as ISA cards). Summit's unique Reset Filtering characteristics provide the microcontroller with a reliable reset, preventing system lock-up and controller latch-up. The traditional inverse relationship of cost vs. features is defeated as Summit's considerable degree of added protection is often less expensive than the other methods of implementing reset control.

Streamline Your TI X2 Modem Design

Introduction

Designers of embedded control systems regularly take advantage of the benefits offered by Summit's Precision Reset Controller family as reset control is a necessary and important element of reliable microcontroller design. The overall function of the reset control, or supervisory circuit, and the serial E²PROM memory are understood and the improvements offered by the Summit device are summarily recognized. This recognition does not come quite as easily to engineers who design with chipsets rather than common microcontrollers. This applications note will explain how using the Summit S24022 Precision Reset Controller can enhance modem designs based on the TI X2 chipset.

X2 Requirements

The X2 chipset processor requires an external precision reset control device, or supervisory circuit, to provide a reliable reset signal to the chipset processor. This insures proper modem operation by 1) controlling the critical voltage conditions on power up, 2) protecting the system from improper operation during brown-out situations, and 3) allowing the modem to power-down in a controlled manner. Of all these functions, the power-up aspect is probably the most critical to modem designers.

Reset control has long been a critical aspect of embedded control design and many semiconductor products have been introduced to perform this function reliably. Virtually every microcontroller design now utilizes an external precision reset control circuit. Upon power up, proper reset control ensures that the environment (power, external system, etc.) is stable before the microcontroller is allowed to perform its initialization routines. Failure to do this may result in unreliable operation or system lock-up. The reset control function also protects the system during power-down and supply voltage brown-out situations. A single bit misinterpreted due to marginal thresholds could cause many problems, including unintended jumps to executable routines, potentially wreaking havoc in the overall system. Data corruption of the nonvolatile memory (93C66 serial E²PROM for X2 designs) is also a common result of these situations. For these reasons, the use of discreet precision reset controllers has become a standard element of embedded control design.

Designers of PC add-in cards face these same issues plus more worrisome problems relating to the host interface. Inadequate reset from the host machine (and some platforms often give the card no detectable reset at all) may cause the chipset processor to latch-up, a potentially catastrophic situation! In addition, the slew rate of V_{CC} upon system power-up can vary greatly from platform to platform, from machine to machine within a given platform, and can vary significantly within the same machine. Glitches or perturbations in the V_{CC}, particularly in the range of the chipset processors operating threshold can potentially lock-up the processor or, much worse, cause device latch-up. It is for these reasons that the reset control function is required for X2 modem designs.

Unfortunately, reset devices have traditionally been designed for microcontroller environments where the system is closed and the reset function can be implemented by monitoring the supply voltage. Systems such as PC add-in cards, which are part of a larger system over which the engineer usually has no control, must also consider external signals, impulses, and conditions. The most important of these is the system reset signal. This leaves most semiconductor reset control devices lacking in their ability to perform adequately in the add-in card environment.

Summit Microelectronics, Inc. has introduced a family of precision reset controllers with advanced features that provide a good fit to the PC add-in card environment. Moreover, these devices allow the user to improve reset control functionality while requiring fewer components! Summit's unique characteristic of incorporating E² trimmability in the reset circuitry allows the addition of industry standard E² memory to the device. The separate serial E²PROM can thus be eliminated from the circuit.

Implementing the SUMMIT Device

The incorporation of the Summit reset control device into the X2 modem design is quite simple. The X2 reference design published by Texas Instruments uses a Maxim 809 reset controller and a 93C66 Microwire serial E²PROM. The connections are shown in Figure 1.

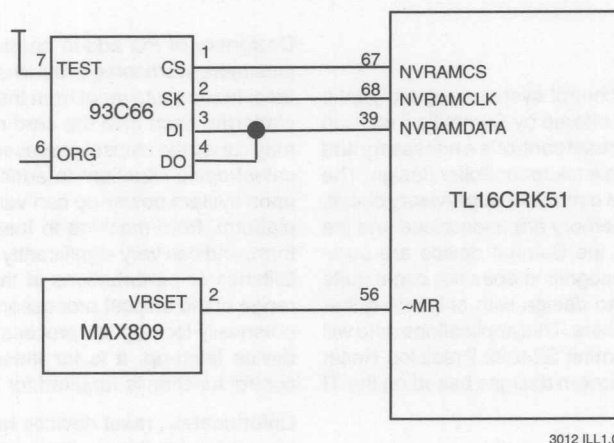


Figure 1: Existing Reset Scheme for X2 Chipset Processor

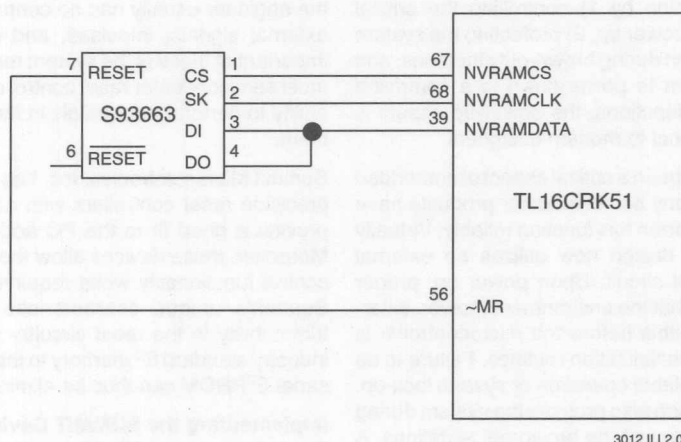


Figure 2: X2 System with Summit Device Providing Reset & Memory Functions

The Summit reset controller features a very convenient pinout for this situation. Since the reset control function requires only one active pin, the device was given the industry standard pinout of the 93C66 serial E²PROM. The only difference is pin 7, which, though unused, is tied high in the reference design (some 93C66 suppliers require a high input to disable test modes, with others is a No Connect). With the Summit S93663 Precision Reset Controller, this pin is the RESET output. The user

can now replace the 93C66 with the S93663 by changing one signal. Rather than tying pin 7 high, it is now tied to the Master Reset line (~MR) of the chipset processor. Since the S93663 now provides the reset function, the MAX809 can be eliminated, saving cost and board space (see Figure 2). The protocol of the S93663 is identical to the 93C66 so this becomes an "invisible" change to the processor.



Additional Advantages: Reset Filtering

To this point, we have discussed the RESET pin of the Summit S93663 as an output. It is actually a bidirectional pin. The user can tie a reset input (from a manual reset button, for example) to the RESET pin and the S93663 will detect, filter, and act upon this input. This "reset filtering" capability gives the X2 modem designer increased reliability for free.

The system reset signal (RST) coming from the edge-connector is active high and is buffered on the board, usually by an inverter. Instead of using this buffered input as the card's reset signal, it is now used as an input to the Summit S93663. Upon receiving a reset signal from the system reset, the Summit device will assert the reset outputs and hold the reset state until a) the reset signal input is unasserted, or b) the t_{PURST} timeout period expires (130mS min), whichever period is longer. This is a critical aspect of the design. The pulse width of the incoming system reset signal varies greatly from machine to machine. Some PC platforms give the card slot a very short reset pulse, a pulse that is not long enough to ensure a reliable reset function for the chipset(s). In this case, the Summit precision reset controller is now acting as a reset signal conditioner, providing the chipset processor with an accurate and reliable reset pulse. This will eliminate issues related to platform variances of the reset signal and, more important, give the card designer control over this function.

The Summit device will still act as the supply voltage monitor, ensuring that the chipset is operating in a stable environment. When V_{CC} drops below the threshold voltage, V_{TRIP} , for longer than 10nS, the Summit device will assert reset until V_{CC} stabilizes for a period no less than t_{PURST} . Summit Microelectronics, Inc. offers devices with a variety of V_{TRIP} settings and the unique "E²Analog" process allows for user-specified trip points.

Additional Advantages:

Multiple Reset Requirements

Some designs may have multiple devices requiring reset, such as a PCMCIA card with both LAN NIC and modem capabilities. Both the Ethernet chipset and the X2 chipset require reset signals. The characteristics are not always identical. Some devices require active high reset signals while others require active low. The S93663 features complementary reset outputs that resolve this problem. When the Summit device receives the system reset pulse, both the reset line used as the input and the complementary reset line will be asserted and will stay asserted as described earlier. This scheme also eliminates the need to invert the incoming reset signal as an active high reset input will be connected to active high RESET pin (pin 7) of the Summit device and an active low reset input will be connected to the active low RESET (pin 6).

Figure 3 shows how the Summit device can be incorporated into a LAN NIC/modem design that incorporates multiple chipsets. The example shows the Ethernet controller, requiring an active low reset, and the X2 modem controller which requires an active high reset. Note that if it were convenient for the incoming system reset signal to be inverted, the connection would be made the RESET BAR I/O on pin 6 of the Summit S93663 device. Both the Ethernet controller and the X2 modem controller will be reset in the same manner. Any additional devices in the circuit, such as an I/O controller, speech CODEC processor device (for DSVD), Plug-and-Play controller, etc. that require reset inputs for reliable operation will have access to a reset signal of the desired polarity.

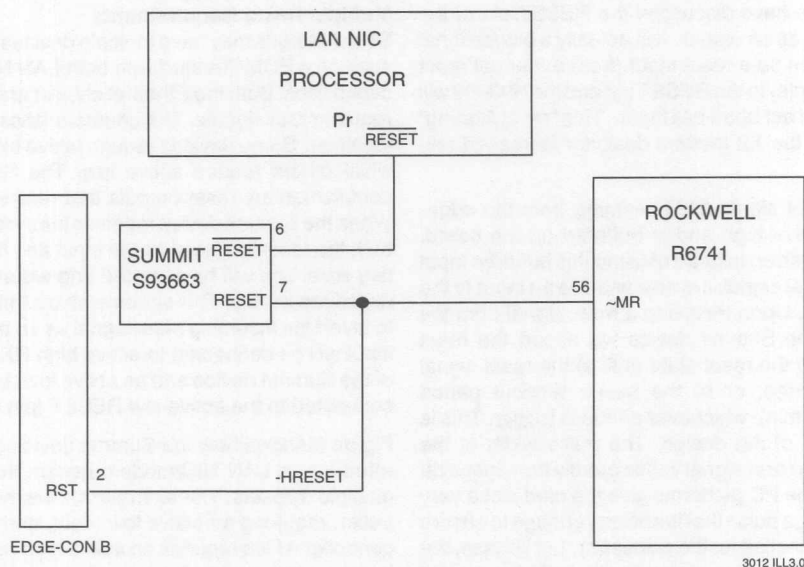


Figure 3: Design Requiring Multiple Resets of Opposite Polarities

Reliability Enhancement: Protection Against Data Corruption

The integration aspect of the Summit device offers additional benefits that are very important to the overall reliability and performance of the system. Stand-alone serial E²PROMs are inherently susceptible to data corruption, especially in brown-out (low V_{CC}) situations, power-up sequences, and power-down sequences. The S93663 features an internal lock-out feature that shuts down the write capabilities of the on-board memory when the system is in reset. This protects the E² from data corruption, doing so much more effectively than external write control pins. Data corruption can be, at best, a nuisance to the user, and at worst, catastrophic to unit operation. Elimination of even small incidents of data corruption can save considerable cost at all points of the product process.

Summary

Reliability Enhancements

- More Precise Reset Threshold
- Reset "Filtering" of External Reset
- Protection Against E² Data Corruption

Logistical Enhancements

- One Less Chip
- Less Board Space
- More Functions
- Lower Cost

The Summit precision reset controller family offers the designer of X2 modems a cost-effective method of increasing the performance of their design and increasing the reliability of operation. This will result in fewer production rejects and fewer product returns. If reset filtering is utilized, the Summit solution allows the designer a higher level of immunity from the wide variances in PC platforms. This allows for a reduced product evaluation and debug times which result in a faster time to market. The design-in is virtually invisible since the Summit part replaces an existing device which is 100% software compatible.

Preventing Data Corruption During Power Failures

Introduction

The loss or corruption of data stored in a nonvolatile memory is the reason that the reset controllers with integrated E²PROM were developed by Summit Microelectronics. These devices insure that an inadvertent write cycle cannot be initiated during the periods of power transitions. This capability has virtually eliminated the possibility of a write cycle occurring during the period of power instability, the devices do not answer the question of what happens if the power failure occurs during the internal write cycle of the device.

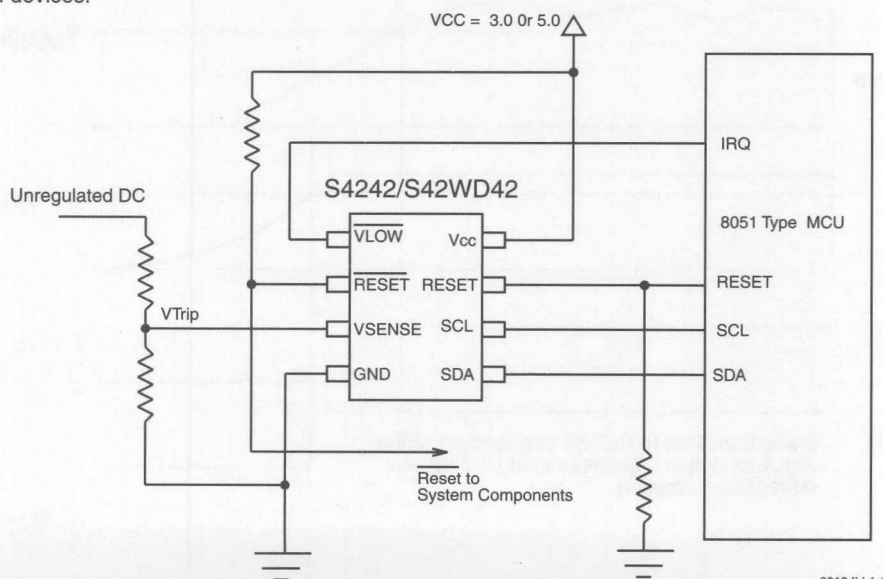
Background

Once the more common problem of inadvertent write cycle initiations is eliminated from the application, there is still one more circumstance which could result in improper data stored in the E²PROM. If a power failure should occur during a write cycle that was initiated prior to the power failure, the question arises, what is the final state of the nonvolatile data? Unfortunately, the answer will vary depending upon the internal architecture of the E²PROM, which varies from manufacturer to manufacturer, as well as the decay rate of the supply voltage. Since it is virtually impossible to predict every power supply failure mode and how it will affect the internal operation of the device, the problem has not been left addressed by the suppliers of E²PROM devices.

Solution

Summit has designed a family of microcontroller supervisory circuits that can be used to prevent all issues of data corruption in the serial E²PROM. The devices feature both a VCC sensor to detect when VCC is within tolerance or not as well as a second voltage sensor which can monitor another voltage in the system. In the case of the S4242 device, this second voltage sensor is called V_{SENSE} which is set to sense voltages below 1.25 Volts. Whenever the sense input is below this voltage, an active low open drain output called V_{LOW} is asserted.

The voltage sensor is used to monitor the unregulated DC in the system and the V_{LOW} output is connected to an interrupt on the microcontroller. A resistor divider is used on the V_{SENSE} input to set the desired level of unregulated DC which will correspond to the 1.25 Volt input level. The block diagram of this system implementation is shown in figure 1. The serial interface to the 4K bit E²PROM is an I²C interface utilizing the standard SCL and SDA interface connections to the microcontroller I/O ports.



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Figure 1: Typical 8051/S4242 Implementation

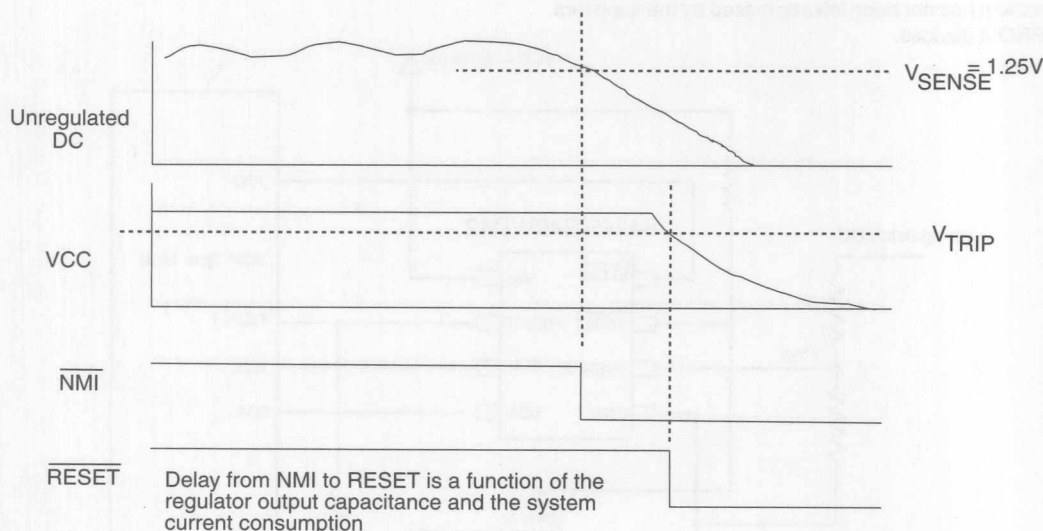


The S4242's VCC sensor monitors the condition of the VCC supply and will generate a RESET to the microcontroller whenever VCC is below a selected voltage, 4.35 volts for example, which will prevent the microcontroller from getting "confused" during a power down situation and generating write operations to the E²PROM. The voltage sensor on the VCC input is also used to disable write operations to the E²PROM whenever VCC is below the selected voltage.

In order to guard against the loss of power during an E²PROM write cycle, the MCU must determine if the unregulated DC is still in spec, which can be sensed by the status of the VLOW signal. The interrupt service routine for this sets a flag to tell the MCU that power is failing in the system. The subroutine which performs a write to the E²PROM will always check the status of this flag prior to the initiation of a write cycle.

Care must be taken to design the output stage of the regulator to insure that the fall time of the system VCC from the normal operation range to the trip point of the S4242 VCC sensor is longer than 10 ms after the power failure level of the unregulated DC is reached. This will insure that any write cycles which are initiated while the unregulated DC is within tolerance will be completed before the system enters the reset state. The maximum write cycle time for the Summit E²PROMs is 10 ms, although the typical value is closer to 5 ms. Therefore, the power down routine must add in the write operation interface period and any other routines which will be executed between the querying of the power status flag and the stop bit of the write instruction to the serial E²PROM. Figure 2 shows the timing diagram for this implementation.

Another benefit of this implementation is that the VLOW interrupt can actually be used to warn the micro of impending power failure. At this time, the micro can perform important housekeeping functions including the updating of system parameters in the S4242's E²PROM data storage so that when power returns to the system, the system will know the status when the power failure occurred.



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Figure 2: Sequence of Voltages Dropping and the S4242 Signal Response to the System



SECTION 11 **Frequently Asked Questions**

Frequently Asked Questions	11-3
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Frequently Asked Questions About E²PROM Devices

General

Microwire (93xxx)

I²C (24xxx)

SPI (25xxx)

General

Q: I do not have a Microwire, I²C, or SPI port on my microcontroller. Which is better to use?

A: It is a matter of trade-offs, though I²C and SPI are the preferred interfaces for today's designers that must "bit-bang". Microwire and SPI require four port pins and I²C only two. I²C, however, requires one line to be bi-directional which is difficult with some microcontroller architectures. I²C has the capabilities to communicate with more than one device over the same two wires. SPI devices usually feature the fastest interface clock rates and have more features available. SPI and I²C are easier to implement with microcontrollers that have normally high outputs and Microwire with microcontrollers with normally low outputs.

Q: If I²C and SPI are so much better, why do manufacturers still make the Microwire devices?

A: Because they are the cheapest! If the application only requires 1K or less of memory, the Microwire 1K device (93x46) is the lowest cost alternative.

Q: Are E² devices with the same generic part number interchangeable?

A: Unfortunately, no. There can be subtle differences from manufacturer to manufacturer. These involve timing differences, page modes, pinouts, and special modes of operation.

Q: What is "bit-banging"?

A: "Bit-banging" is the term used for emulating the serial protocol with code. The E² device is connected to I/O pins, which are manipulated by bringing them HIGH and LOW to simulate the proper sequence of bits. This is the common method of communication with serial E² devices when used with a microcontroller that does not have a Microwire, I²C, or SPI port. Example code is available from many commodity E² manufacturers.

Q: What are page modes?

A: Page modes allow the user to write more than one byte for a given write cycle. The typical write cycle is 5mS in duration. Page sizes vary with array density and from manufacturer to manufacturer.



Frequently Asked Questions

Q: How reliable are an E² manufacturer's endurance specifications?

A: This is a very subjective area among commodity E² suppliers and the specifications are sometimes vaguely worded. There is some good reason for this. Many factors will impact the endurance of the E² in your particular system. Your best bet is to ask the potential supplier what their part will do in your system and provide them with information as to how the device will be written to in the course of its lifetime.

Q: Which is better, software write protection or hardware write protection?

A: The answer, unfortunately, is neither. Hardware write protection for a serial E² device is only effective when using the device as an OTP and hard-wiring the control pin to the disabled state. Other times, the event causing the microcontroller to inadvertently write to the E² will also enable the write protection (hardware or software).

Q: What is V_{CC} Sense and how well does it protect against inadvertent writes?

A: V_{CC} Sense is offered by some commodity E² suppliers as a preset threshold voltage below which no operations are allowed. Sensitivity to temperature and process variations cause wide fluctuations in the threshold and, therefore, make it extremely unreliable for inadvertent write protection.

Q: How susceptible are serial E² devices to noise?

A: This varies from manufacturer to manufacturer and, for any given manufacturer, from lot to lot. Noise suppression specifications of 100nS and greater are considered adequate.

Q: I am experiencing data corruption with my serial E² device. My code is perfect. How can this be?

A₁: Most commodity E² manufacturers use one device to satisfy many voltage ranges of products offered. In other words, the same device is manufactured to be used as the 5V±10% part, the 2.7-3.3V part, etc. It simply becomes a question of yield to the manufacturer. However, this means that a device used in a 5V±10% application may operate to very low voltages, where a number of things can cause inadvertent writes. Among these are an increased susceptibility to noise at the lower voltages, transient noise caused by system instability, or unreliable operation of the microcontroller (see A₂). Voltage protected E²PROMs will eliminate this failure mode.

A₂: This may be a problem with the microcontroller. Serial E² devices usually operate to lower voltages than microcontrollers. In power down or brown out situations, the microcontroller may misinterpret code and perform an unintended write operation to the serial E² causing data corruption. Designing proper reset control into the system can prevent this. Using an external precision reset controller is a must.

Q: My design used to be problem free but now I experience occasional data corruption with my E² device. Why is this?

A: This could be due to minor process improvements made by the manufacturer. The device you are using may now operate at lower voltages or respond to smaller noise spikes than in the past. These can result from die shrinks, design changes, process enhancements, or smaller geometries. Using a voltage protected E²PROM may eliminate these problems.



Frequently Asked Questions

Microwire (93xxx)

- Q: I cannot establish communications with my Microwire device.
- A: Check your protocol to see on which edge you clock data in and out of the device. Microwire devices clock data in (DI pin) on the *rising* edge of the SK and data out (DO pin) on the *falling* edge of SK.
- Q: The instructions for my Microwire device are 9 to 11 bits long but my microcontroller has a fixed 8-bit shift register. How do I communicate with the E² device?
- A: By writing twice with the data being the last 9 to 11 significant bits. The most significant bits should be zero's so they'll be ignored by the device.
- Q: Sometimes my Microwire device fails to accept a write operation.
- A: You have probably deselected the device without completing the clock cycle by giving it a falling edge. This is common in microcontroller systems where the port pin is normally in a logic '1' state. Adding an extra clock cycle will complete the operation.
- Q: When reading my Microwire device, the data bits appear shifted right by 1 bit.
- A: You are probably clocking the first data bit in on the falling edge of the same clock cycle that clocked the last address bit out on its rising edge. You need to wait until the falling edge of the next clock cycle.
- Q: How can I tell if my Microwire E² device has completed its internal write operation?
- A: The DO pin can be polled to obtain the write status. By bringing the CS pin HIGH after the write operation has commenced, the DO pin will read '0' until the operation has completed. It will then read '1'.
- Q: My Microwire device sometimes "blanks out" on occasion and the data is all FFH. Why is this?
- A: This sometimes occurs when a Write Enable (WREN) command or Write All Registers (WRAL) Command is interpreted as an Erase All Registers (ERAL) command. There is only one bit difference between the three commands.
- Q: I sometimes experience the top memory location change to FFH in my Microwire device. Why is this?
- A: This could be due to the reset conditions of your microcontroller. Some microcontrollers will tri-state their I/O pins during a reset condition, which is interpreted as a logic HIGH by the E² device. A HIGH on the CS line will enable the device. Since the lines are actually in a high-Z state, this makes the signals especially susceptible to noise. If any noise appears on the SK (clock) line, the enabled device will clock in all '1's which translates to the ERASE command for address location FFH (or top memory location). A 93663-type device will eliminate this problem.



Frequently Asked Questions

I²C (24xxx)

Q: Where did I²C come from?

A: I²C was developed by Philips Semiconductor to provide a low cost interface between different chips. It provides a comprehensive interface which is similar to the Ethernet on a logical level. As such, each device on the bus must have a unique address and provisions are included for detection and correction of communications collisions on the serial interface. In this manner, the I²C is truly a serial bus, while the Microwire and the SPI are more serial interfaces.

Q: Do I need a license for using I²C in my system?

A: Good question. Philips has licensed the I²C bus to several manufacturers. If the manufacturer of any of the devices on the I²C bus in a system are licensees, then this license is passed on to the users of the chips. This could be the serial E²PROM, the microcontroller, or a display module. Many manufacturers of I²C serial E²PROMs are, indeed, not licensed by Philips, and as a result utilization of these devices could put one at risk of violation of the Philips patents. The safest approach is to contact your vendors to insure that they are licensed to sell I²C devices.

Q: Are all I²C devices hardware (pin-for-pin) compatible?

A: No. Different manufacturers use pin 7 for miscellaneous uses. Sometimes it is a TEST pin, other times a hardware Write Control. In reality, these functions are of little or no use to the user. I²C E² devices that have integrated precision reset controllers use pin 7 as a RESET output.

Q: Are all I²C devices software compatible?

A: No. The generic protocol is consistent from 2K-bits to 16K-bits. There are, however, differences in the page size (see *What are page modes?* of the General section) from manufacturer to manufacturer. There are protocol differences at the 1K density (see *What is the difference between a 24x01 device and a 24x01A or 24x01B device?* of this section) and above 16K. Above 16K, some manufacturers use an additional addressing byte while others reassign slave address bits as extended addressing bits.

Q: What are the address inputs A0-A2 used for?

A: The I²C protocol defines each device on the bus as having a unique slave address. This slave address is made up of a device identifier ("1010" on E²PROMs) and a device address. The device address is set by pulling the address inputs HIGH or LOW to give up to eight different combinations. This feature was of great benefit in the early days of serial E²PROMs, since it allowed an extension of the density of the devices through the utilization of multiple devices on the same bus. The address inputs become somewhat useless now that capacities are available for almost all systems requirements. Since these "unused" inputs are often used for manufacturer's test modes, it is always a good idea to connect them to ground.

Q: What is the ACK bit and why is it important?

A: The I²C bus has been developed as an Inter-Integrated Circuit serial bus (hence the name I²C). The full protocol extends far beyond the requirements for a serial E²PROM and an MCU. Full I²C allows for multiple master devices to be on the same bus and includes a method of transmission collision detection. In a full implementation of an I²C bus, the ACK signal is used to acknowledge that the last data transfer



Frequently Asked Questions

was completed properly, and that no collision has occurred on the bus.

Q: Is the ACK (acknowledge bit) required when simply 'bit-banging' to communicate with the device.

A: Yes. When reading data from the device, the host must acknowledge the device before receiving the next byte. When sending data to the device, the ACK that the device sends back may be ignored, but the clock cycle must be given in order to proceed further.

Q: Can I ignore the ACK (acknowledge bit) sent by the E² after I send it data?

A: Yes. Nevertheless, you must still give the 9th clock cycle so the device can perform the ACK operation. It is generally a good idea to monitor the ACK/NACK bit to ensure reliable operation.

Q: My E² device fails to acknowledge. I cannot communicate with the device.

A₁: Check the value of your pull-up resistors. The signal voltage may be insufficient to register a '1' state.

A₂: Check for a valid START condition. A START condition is given when the SDA line is brought from a HIGH state to a LOW state when the SCL line is in the HIGH state.

A₃: Check data stream to ensure that the control byte is correctly given. I²C devices are selected through the protocol and will ignore an incorrect slave address.

A₄: Make sure that a 9th clock cycle is given so the device can send the ACK (acknowledge) bit.

A₅: Make sure that the host releases the bus before issuing the 9th clock cycle so the device can pull the line LOW for a proper ACK operation.

A₆: Make sure that the SDA line is always stable when the SCL line is in the HIGH state. If not, the device will interpret the transition as either a START or STOP bit, either of which will prevent proper communication.

Q: Is the STOP bit necessary?

A: In truth, not always – but it is good practice to use it. Not using a STOP bit could leave the device in an unknown state and could possibly cause the device to interpret signals on the bus as a write command or additional write data.

Q: How can I tell if my I²C E² device has completed its internal write operation?

A: By using 'Acknowledge Polling'. Simply send the device a dummy read command. If the device does not acknowledge the command, it is still performing its internal write operation.

Q: Why must I write to the E² device when I want to read a random memory location?

A: The random address read operation is actually a two-cycle instruction. The first cycle is a write of the slave address and memory location of the device to be read. This sets the address pointer at the proper value. The second cycle is actually a current address read operation. The START condition which separates the two cycles is very important since it prevents the two cycles of a random read operation from being misinterpreted as a write operation (see *When I attempt to read my device, the location I attempt to read*



Frequently Asked Questions

sometimes appears corrupted to read the address or FFH? Why is this? of this section).

Q: When I attempt to read my device, the location I attempt to read sometimes appears corrupted to read the address or FFH? Why is this?

A: The first operation of the random read sequence is actually a *write* operation, which is required to set the address pointer. Once the address is given, a new START bit is required to reset the device and then a read operation is performed. Sometimes noise can cause the START condition to be misinterpreted (i.e. ignored). The next byte in the random read sequence is the slave address byte, which now is written into the memory location addressed. If additional byte reads are attempted, the clock cycles that should be clocking data into the buffer are, in actuality, clocking data into the E² memory. Since the bus is released for the intended read operation, the E² device reads all '1's from the pulled-up bus, or FFH.

Q: What is the difference between a 24x01 device and a 24x01A or 24x01B device? A 24x02 and a 24x02B device?

A: The generic 24x01 device does not have slave addressing. This means that the two wires used to communicate with the 24x01 must be dedicated. There are also fewer sources for the 24x01. The 24x01B and 24x02B are devices which still use the slave address in their protocol, but they respond to *all* slave addresses *regardless* of the status of the A0-A2 inputs.

SPI (25xxx)

Q: What are modes and how do I know which one is correct?

A: SPI modes 0,1,2, and 3 concern the clock phase and which edge data is clocked on. Most commodity SPI serial E² devices operate in Modes 0 and 2.

Q: How can I tell if my SPI E² device has completed its internal write operation?

A: The status register contains a WIP (Write In Process) bit that can be polled during this operation.

Q: Microwire E² devices have a pin-out that mirrors SPI port pin-outs. Can I use a Microwire device with an SPI port?

A: Yes, but it is not the optimum solution. The fact that Microwire communication involves different edge triggering for data in and data out operations makes "bit-banging" a must. The code required interfacing a Microwire device to an SPI port is typically 3X that of code required for an SPI device.



SECTION 12 **Packaging Information**

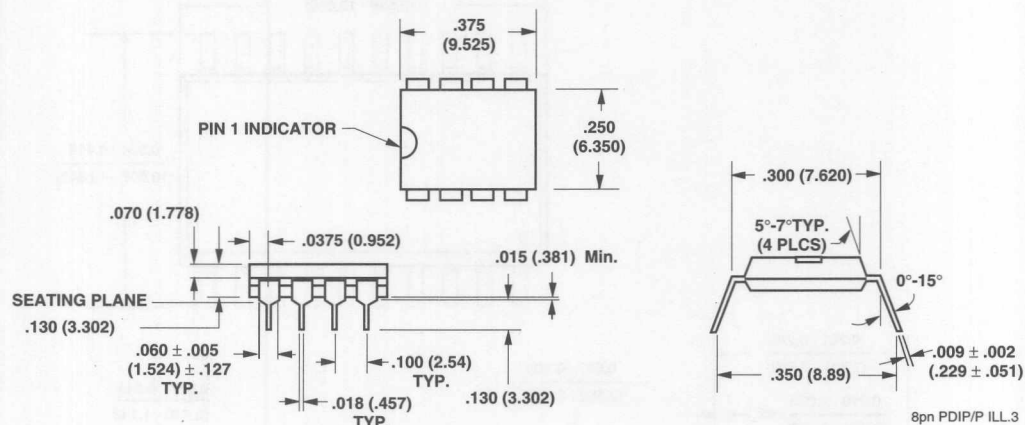
8ld DIP, 8ld SOIC, 20ld SOIC, 24ld SOIC, Solder Profiles, Tape & Reel 12-3



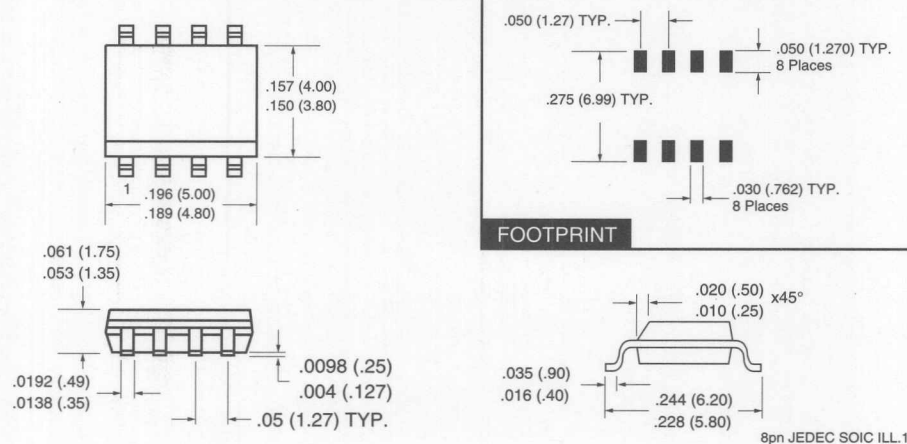
SECTION 12 - Packaging Information

12-1. The following information is required for the packaging of the product:

8 Pin PDIP (Type P) Package



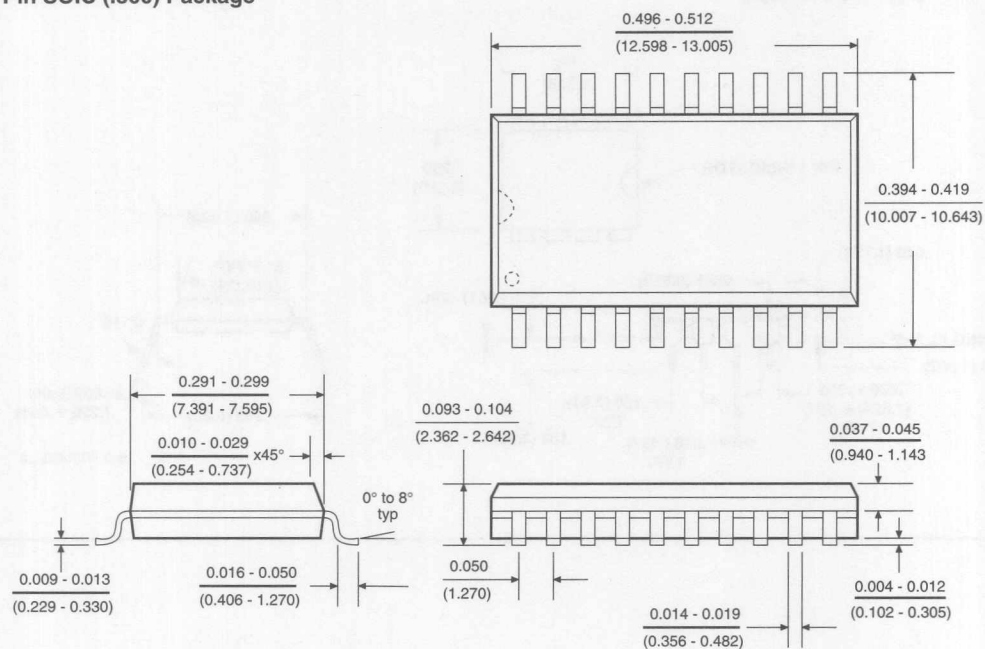
8 Pin SOIC (Type S) Package JEDEC (150 mil body width)





Packaging Information

20 Pin SOIC (.300) Package

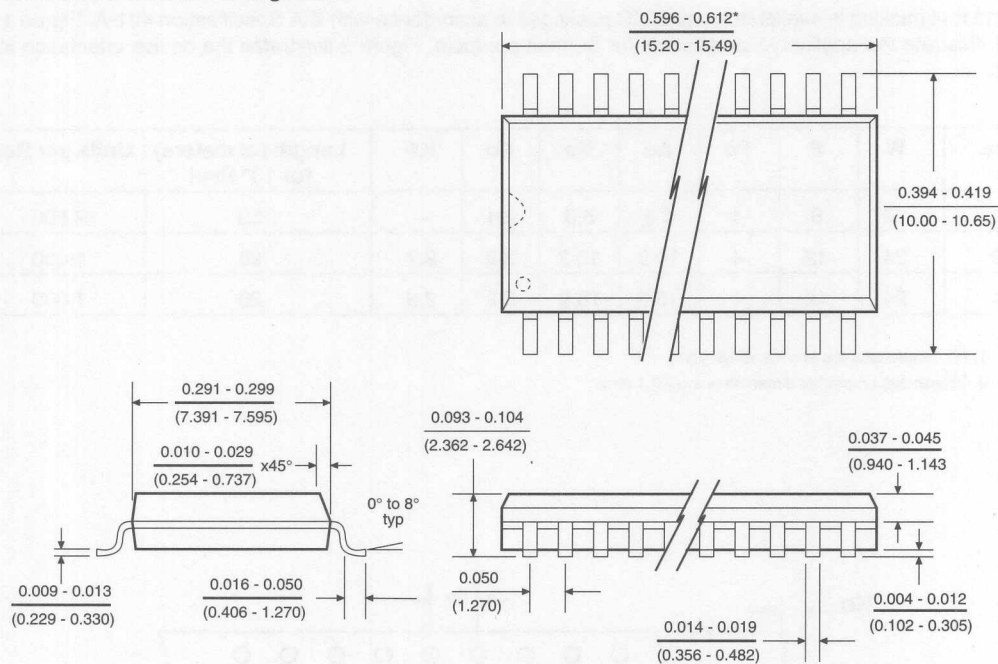


20pin SOIC ILL.1



Packaging Information

24 Lead Small Outline Package SOIC



24pn SOIC ILL.0



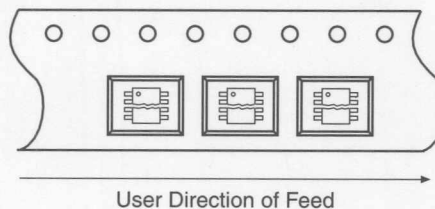
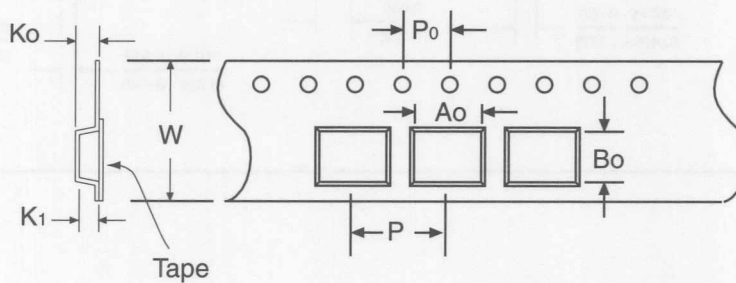
Packaging Information

Tape and Reel Packing

Tape and reel packing is available for all SOIC packages in accordance with EIA Specification 481-A. Figure 1 and Table 1 illustrate the applicable dimensions for Summit products. Figure 2 illustrates the device orientation in the pockets.

Device Type	W	P	Po	Ao	Bo	Ko	K1	Length (in meters) for 13" Reel	Units per Reel
SO-8	12	8	4	6.5	5.3	2.1	—	30	2,500
SO-20	24	12	4	10.9	13.3	3.2	2.7	20	1,000
SO-24	24	12	4	10.9	15.9	3.2	2.8	20	1,000

Notes: 1. All Dimensions are in millimeters (mm).
2. Tolerances on pocket dimensions are ± 0.1 mm.





Packaging Information

WAVE AND REFLOW SOLDERING

Following are the recommended procedures for soldering surface mount packages to PC Boards.

Wave Soldering

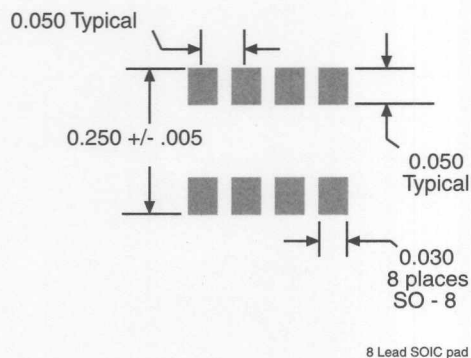
1. Use solder plating boards
2. Dispense adhesive to hold components on the PC board
3. Place components on the PC board
4. Cure adhesive per the adhesive manufacturer's specification
5. Foam flux using RMA (Rosin Mildly Activating) flux
6. Wave solder using a dual wave soldering system at 240°C to 260°C for 2 seconds per wave.
7. Clean Board

Reflow Soldering

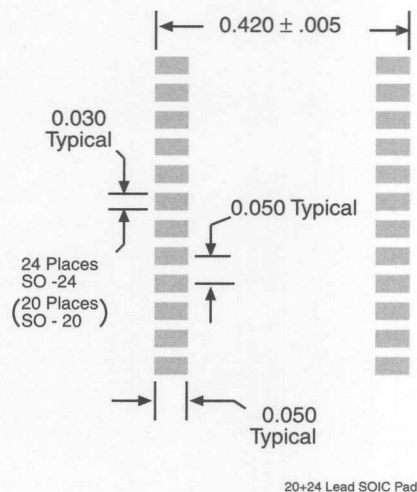
1. Use solder plating boards
2. Screen the solder paste onto the PC board
3. Mount the components onto the PC board
4. Bake for 15 to 20 minutes at 65°C to 90°C
5. Preheat to within 65°C of the solder melting temperature
6. Reflow the solder paste. The solder paste temperature must be 200°C for at least 30 seconds. SMI recommends vapor phase or infrared reflow systems for best performance
7. Clean PC boards

TYPICAL PAD LAYOUTS FOR PC BOARDS

8 Lead SOIC



20 and 24 Lead SOIC





Packaging Information

TABLE 1: PACKAGING INFORMATION

TABLE 2: PACKAGING INFORMATION

TABLE 3: PACKAGING INFORMATION

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TABLE 40: PACKAGING INFORMATION



SECTION 13 **General Ordering Information**

Ordering Tree 13-3



SECTION 2 General Contract Information

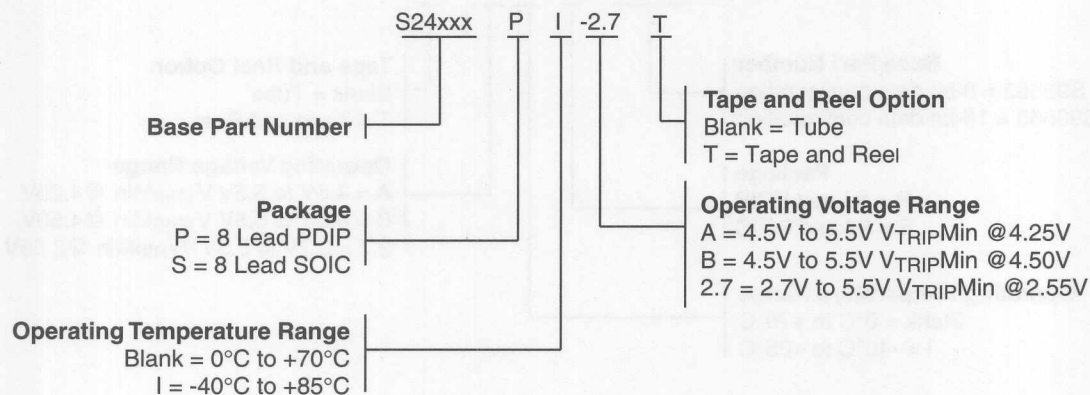
Contract No. _____

Contract Title _____

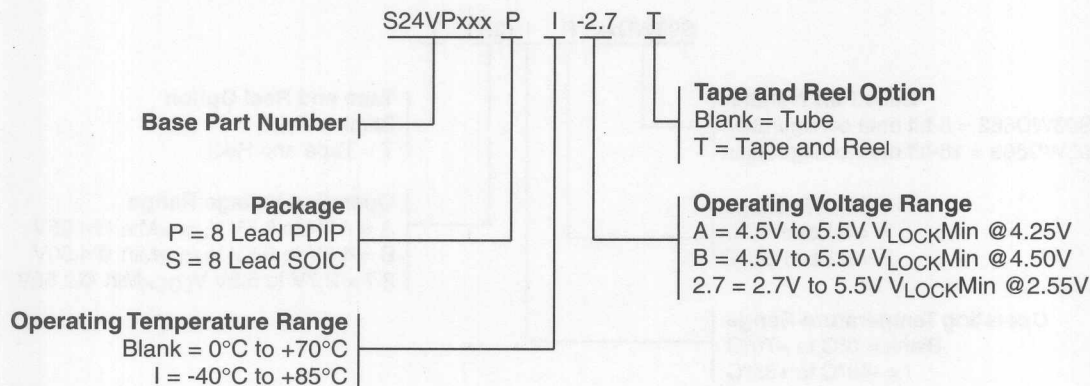
Contract Description _____

ORDERING INFORMATION

Precision Reset Controllers with I²C Memories



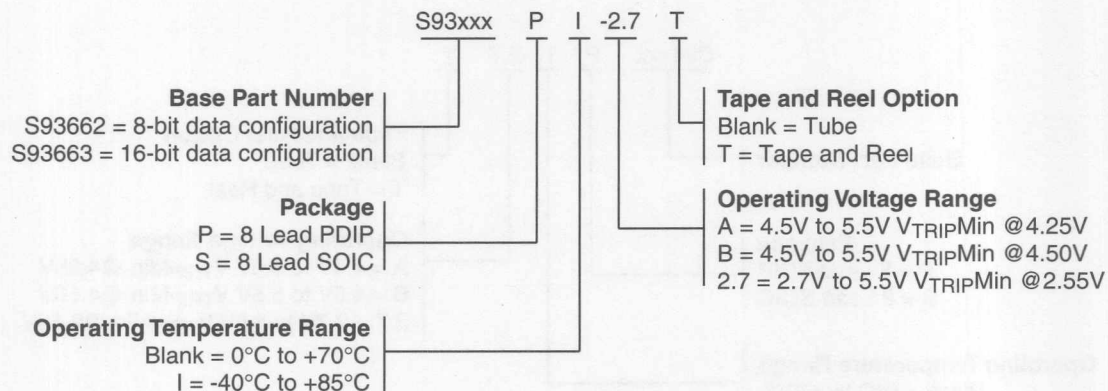
Voltage Protected I²C Memories



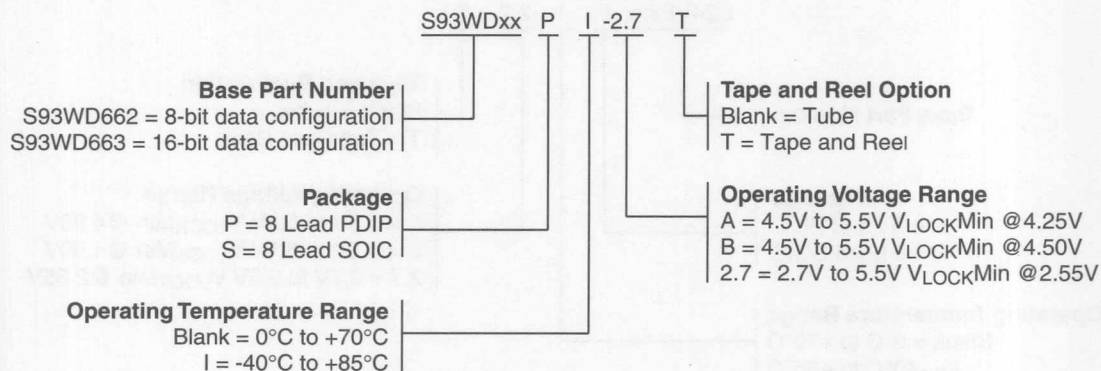


Ordering Information

Precision Reset Controllers with a Microwire Memory



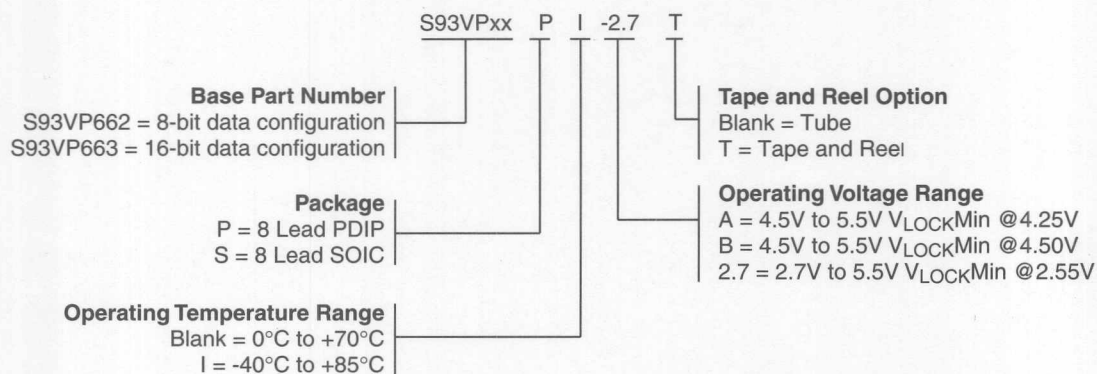
Precision Reset Controller with a Watchdog Timer and Microwire Memory



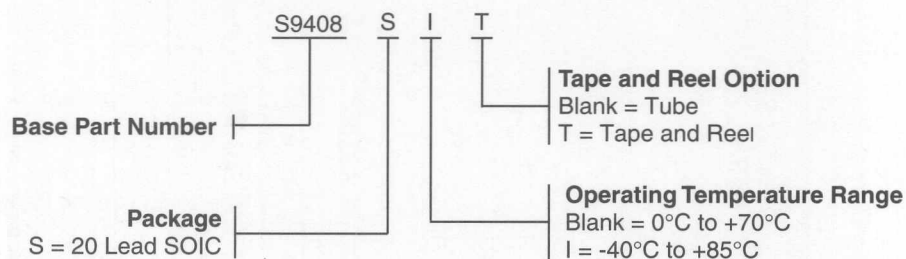


Ordering Information

Voltage Protected Microwire Memory



Nonvolatile DAC





Ordering Information

